

## Excellent Integrated System Limited

Stocking Distributor

Click to view price, real time Inventory, Delivery & Lifecycle Information:

[Alliance Memory, Inc.](#)  
[AS6C8008A-45ZINTR](#)

For any questions, you can email us directly:

[sales@integrated-circuit.com](mailto:sales@integrated-circuit.com)



## AS6C8008A Family

Low Power, 1Mx8 SRAM

---

### Document Title

1M x 8 bit Super Low Power and Low Voltage Full CMOS Static RAM

### Revision History

Revision No.	History	Date	Remark
0.0	-. Initial Draft	Aug. 7 2013	Preliminary



## AS6C8008A Family

### Low Power, 1Mx8 SRAM

#### FEATURES

- Process Technology : 0.15  $\mu$ m Full CMOS
- Organization : 1M x 8 bit
- Power Supply Voltage : 2.7V ~ 3.6V
- Low Data Retention Voltage : 1.5V(Min.)
- Three state output and TTL Compatible
- Package Type : 48-FPBGA, 44-TSOP2

#### GENERAL DESCRIPTION

The AS6C8008A families are fabricated by Alliance Memory's advanced full CMOS process technology. The families support industrial temperature range and Chip Scale Package for user flexibility of system design. The families also supports low data retention voltage for battery back- up operation with low data retention current.

#### PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby ( $I_{SB1}$ , Typ.)	Operating ( $I_{CC1}$ -Max.)	
AS6C8008A-45BIN	Industrial (-40 ~ 85°C)	2.7 ~ 3.6 V	45 ns	2 A <sup>1)</sup>	4 mA	48-FPBGA
AS6C8008A-45ZIN						44-TSOP2

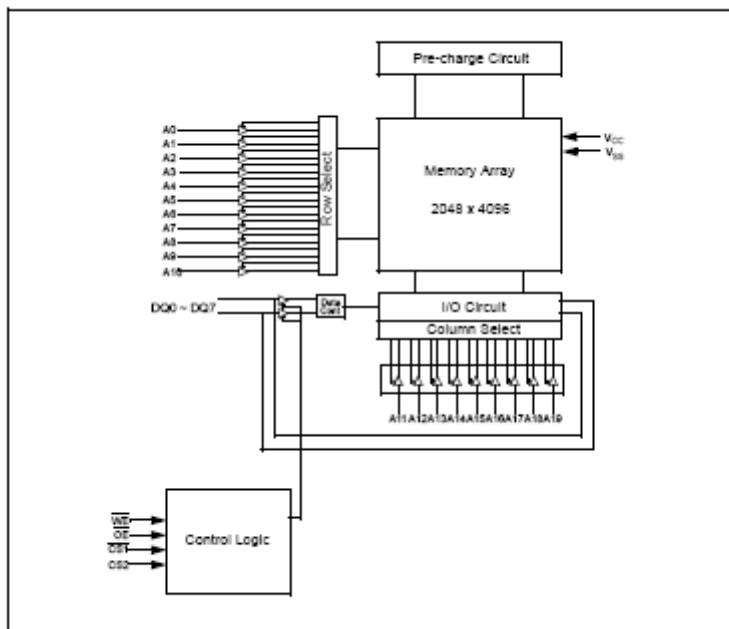
<sup>1)</sup>Typical values are measured at Vcc=3.3V, T<sub>A</sub>=25°C and not 100% tested.



# AS6C8008A Family

## Low Power, 1Mx8 SRAM

### FUNCTIONAL BLOCK DIAGRAM

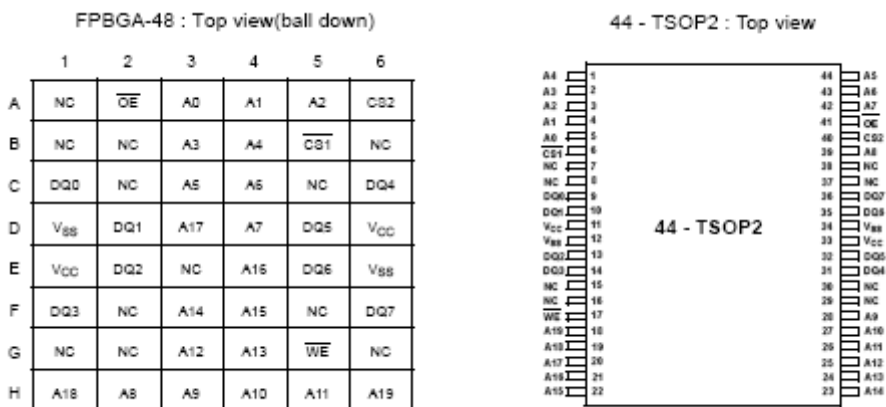




## AS6C8008A Family

### Low Power, 1Mx8 SRAM

#### PIN CONFIGURATIONS



#### PIN DESCRIPTION

Name	Function	Name	Function
$\overline{CS1}$ , $\overline{CS2}$	Chip Select inputs	V <sub>CC</sub>	Power Supply
$\overline{OE}$	Output Enable input	V <sub>SS</sub>	Ground
$\overline{WE}$	Write Enable input	NC	No Connection
A0~A19	Address inputs		
DQ0~DQ7	Data inputs/outputs		



## AS6C8008A Family

### Low Power, 1Mx8 SRAM

#### ABSOLUTE MAXIMUM RATINGS<sup>1)</sup>

Parameter	Symbol	Ratings	Unit
Voltage on Any Pin Relative to Vss	V <sub>IN</sub> , V <sub>OUT</sub>	-0.2 to 4.0	V
Voltage on Vcc supply relative to Vss	V <sub>CC</sub>	-0.2 to 4.0	V
Power Dissipation	P <sub>D</sub>	1.0	W
Operating Temperature	T <sub>A</sub>	-40 to 85	°C

1. Stresses greater than those listed under “nav” may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

#### FUNCTIONAL DESCRIPTION

CS1	CS2	OE	WE	DQ0~7	Mode	Power
H	X	X	X	High-Z	Deselected	Stand by
X	L	X	X	High-Z	Deselected	Stand by
L	H	H	H	High-Z	Output Disabled	Active
L	H	L	H	Data Out	Read	Active
L	H	X	L	Data In	Write	Active

NOTE : X means don't care. (Must be low or high state)



## AS6C8008A Family

Low Power, 1Mx8 SRAM

### RECOMMENDED DC OPERATING CONDITIONS <sup>1)</sup>

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{CC}$	2.7	3.3	3.6	V
Ground	$V_{SS}$	0	0	0	V
Input high voltage	$V_{IH}$	2.2	-	$V_{CC} + 0.2^{2)}$	V
Input low voltage	$V_{IL}$	$-0.2^{3)}$	-	0.6	V

1.  $T_A = -40$  to  $85^\circ\text{C}$ , otherwise specified
2. Overshoot:  $V_{CC} + 2.0$  V in case of pulse width  $\leq 20$ ns
3. Undershoot:  $-2.0$  V in case of pulse width  $\leq 20$ ns
4. Overshoot and undershoot are sampled, not 100% tested.

### CAPACITANCE<sup>1)</sup> (f = 1MHz, $T_A = 25^\circ\text{C}$ )

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	$C_{IN}$	$V_{IN} = 0V$	-	8	pF
Input/Output capacitance	$C_{IO}$	$V_{IO} = 0V$	-	10	pF

1. Capacitance is sampled, not 100% tested



## AS6C8008A Family

### Low Power, 1Mx8 SRAM

#### DC AND OPERATING CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit	
Input leakage current	$I_{LI}$	$V_{IN}=V_{SS}$ to $V_{CC}$	-1	-	1	$\mu A$	
Output leakage current	$I_{LO}$	$\overline{CS1}=V_{IH}$ or $CS2=V_{IL}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ , $V_{IO}=V_{SS}$ to $V_{CC}$	-1	-	1	$\mu A$	
Operating power supply	$I_{CC}$	$I_{IO}=0mA$ , $\overline{CS1}=V_{IL}$ , $CS2=\overline{WE}=V_{IH}$ , $V_{IN}=V_{IH}$ or $V_{IL}$	-	-	2	mA	
Average operating current	$I_{CC1}$	Cycle time=1 s, 100% duty, $I_{IO}=0mA$ , $CS1 \leq 0.2V$ , $CS2 \geq V_{CC}-0.2V$ , $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC}-0.2V$	-	-	4	mA	
	$I_{CC2}$	Cycle time = Min, $I_{IO}=0mA$ , 100% duty, $CS1=V_{IL}$ , $CS2=V_{IH}$ , $V_{IN}=V_{IL}$ or $V_{IH}$	45ns	-	-	45	mA
			70ns	-	-	25	
Output low voltage	$V_{OL}$	$I_{OL} = 2.1mA$	-	-	0.4	V	
Output high voltage	$V_{OH}$	$I_{OH} = -1.0mA$	2.4	-	-	V	
Standby Current (TTL)	$I_{SB}$	$\overline{CS1}=V_{IH}$ , $CS2=V_{IL}$ , Other inputs= $V_{IH}$ or $V_{IL}$	-	-	0.5	mA	
Standby Current (CMOS)	$I_{SB1}$	$\geq V_{CC}-0.2V$ , $CS2 \geq V_{CC}-0.2V$ (CS1 controlled) or $0V \leq CS2 \leq 0.2V$ (CS2 controlled), Other inputs = $0 \sim V_{CC}$ (Typ. condition : $V_{CC}=3.3V$ @ $25^{\circ}C$ ) (Max. condition : $V_{CC}=3.6V$ @ $85^{\circ}C$ )	LF	-	2.1	15	$\mu A$

1. Typical values are measured at  $V_{CC}=3.3V$ ,  $T_A=25^{\circ}C$  and not 100% tested.



### AC OPERATING CONDITIONS

Test Conditions (Test Load and Test Input/Output Reference)

Input Pulse Level : 0.4 to 2.4V

Input Rise and Fall Time : 5ns

Input and Output reference Voltage : 1.5V

Output Load (See right) :  $CL^{(1)} = 100pF + 1\ TTL(70nsec)$

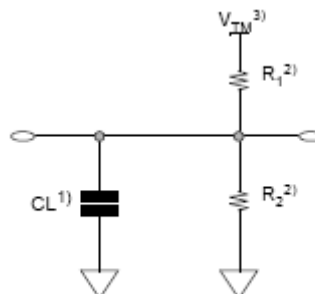
$CL^{(1)} = 30pF + 1\ TTL(45ns/55ns)$

1. Including scope and Jig capacitance

2.  $R_1=3070\Omega$ ,  $R_2=3150\Omega$

3.  $V_{TM}=2.8V$

4.  $CL = 5pF + 1\ TTL$  (measurement with  $t_{LZ}$ ,  $t_{HZ}$ ,  $t_{OLZ}$ ,  $t_{OHZ}$ ,  $t_{WHZ}$ )



**READ CYCLE** ( $V_{CC} = 2.7$  to  $3.6V$ ,  $Gnd = 0V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ )

Parameter	Symbol	45ns		Unit
		Min	Max	
Read cycle time	$t_{RC}$	45	-	ns
Address access time	$t_{AA}$	-	45	ns
Chip select to output	$t_{CO1}$ , $t_{CO2}$	-	45	ns
Output enable to valid output	$t_{OE}$	-	30	ns
Chip select to low-Z output	$t_{LZ1}$ , $t_{LZ2}$	5	-	ns
Output enable to low-Z output	$t_{OLZ}$	5	-	ns
Chip disable to high-Z output	$t_{HZ1}$ , $t_{HZ2}$	0	20	ns
Output disable to high-Z output	$t_{OHZ}$	0	20	ns
Output hold from address change	$t_{OH}$	10	-	ns

Parameter	Symbol	45ns		Unit
		Min	Max	
Write cycle time	$t_{WC}$	45	-	ns
Chip select to end of write	$t_{CW1}$ , $t_{CW2}$	45	-	ns
Address setup time	$t_{AS}$	0	-	ns
Address valid to end of write	$t_{AW}$	45	-	ns
Write pulse width	$t_{WP}$	45	-	ns
Write recovery time	$t_{WR}$	0	-	ns
Write to output high-Z	$t_{WHZ}$	0	20	ns
Data to write time overlap	$t_{DW}$	25		ns
Data hold from write time	$t_{DH}$	0	-	ns
End write to output low-Z	$t_{OW}$	5	-	ns

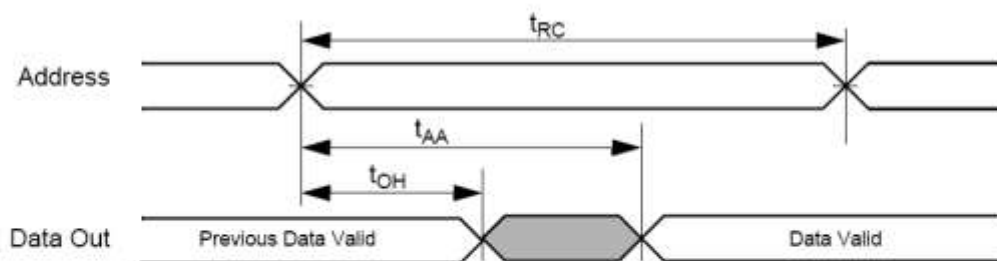


# AS6C8008A Family

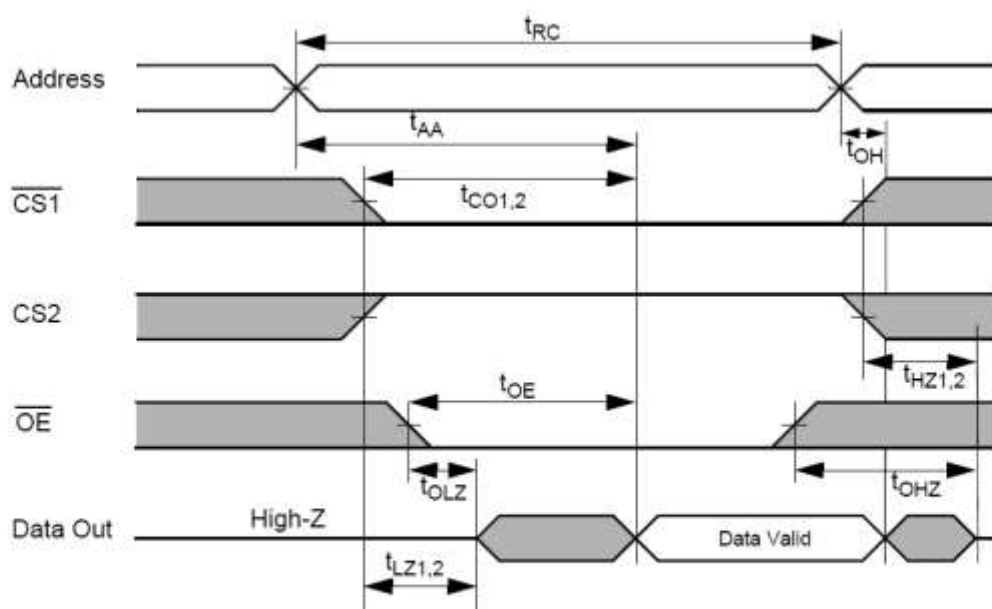
## Low Power, 1Mx8 SRAM

### TIMING DIAGRAMS

**TIMING WAVEFORM OF READ CYCLE(1)** (Address Controlled,  $\overline{CS1}=\overline{OE}=V_{IL}$ ,  $CS2=\overline{WE}=V_{IH}$ )



**TIMING WAVEFORM OF READ CYCLE(2)** ( $\overline{WE} = V_{IH}$ )



**NOTES (READ CYCLE)**

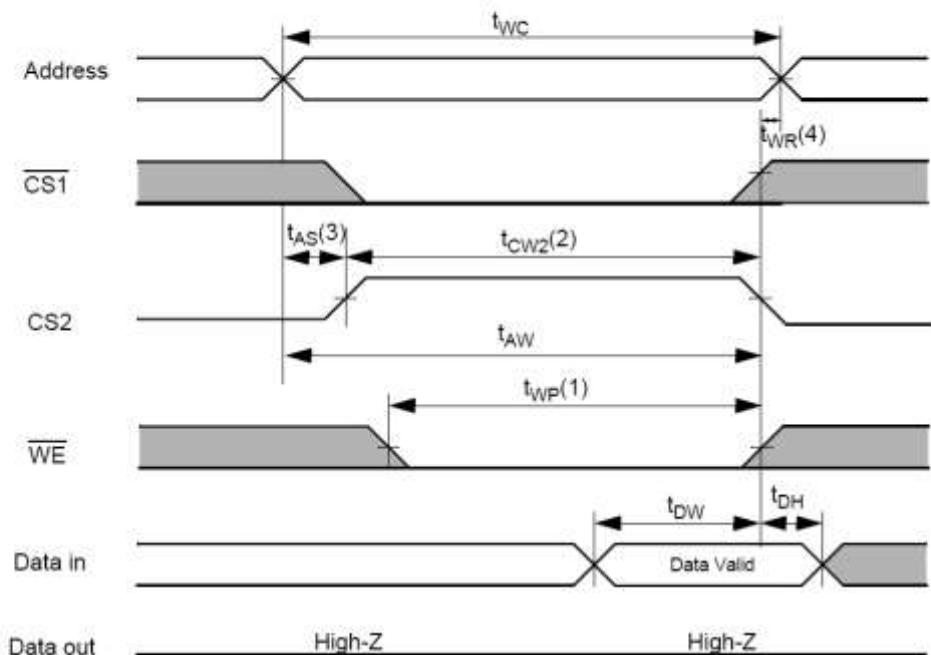
- $t_{HZ1,2}$  and  $t_{OHZ}$  are defined as the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
- At any given temperature and voltage condition,  $t_{HZ1,2}(\text{Max.})$  is less than  $t_{LZ1,2}(\text{Min.})$  both for a given device and from device to device interconnection.



## AS6C8008A Family

### Low Power, 1Mx8 SRAM

#### TIMING WAVEFORM OF WRITE CYCLE(3) (CS2 Controlled)



#### NOTES (WRITE CYCLE)

1. A write occurs during the overlap ( $t_{WP}$ ) of low  $\overline{CS1}$ , a high  $CS2$  and low  $\overline{WE}$ . A write begins at the latest transition among  $\overline{CS1}$  goes low,  $CS2$  goes high and  $\overline{WE}$  goes low. A write ends at the earliest transition among  $\overline{CS1}$  goes high,  $CS2$  goes low and  $\overline{WE}$  goes high. The  $t_{WP}$  is measured from the beginning of write to the end of write.
2.  $t_{CW}$  is measured from the  $\overline{CS1}$  going low or  $CS2$  going high to end of write.
3.  $t_{AS}$  is measured from the address valid to the beginning of write.
4.  $t_{WR}$  is measured from the end of write to the address change.  $t_{WR}$  applied in case a write ends as  $\overline{CS1}$  or  $\overline{WE}$  going high or  $CS2$  going low.



## AS6C8008A Family

### Low Power, 1Mx8 SRAM

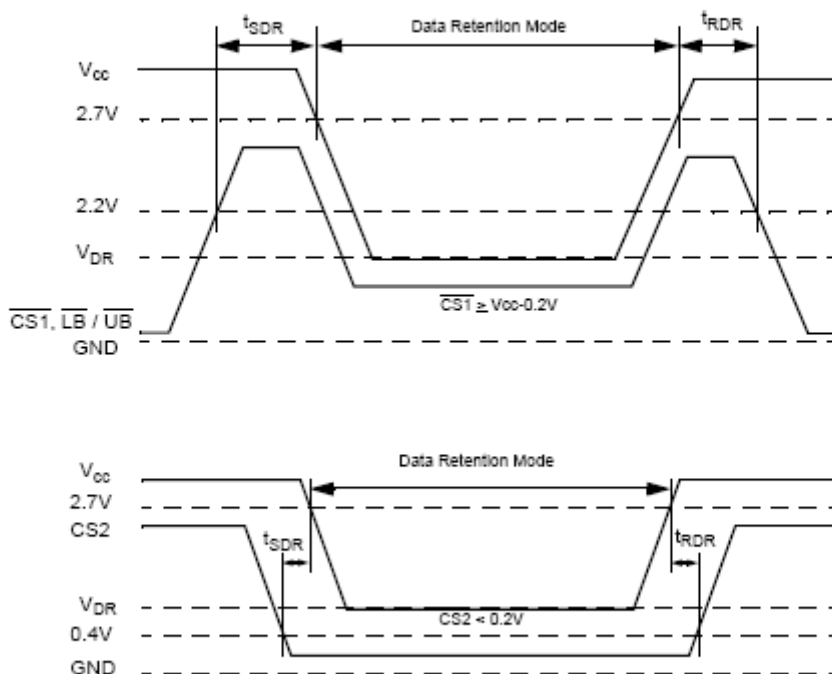
#### DATA RETENTION CHARACTERISTICS

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V <sub>CC</sub> for Data Retention	V <sub>DR</sub>	I <sub>SB1</sub> Test Condition (Chip Disabled) <sup>1)</sup>	1.5	-	3.6	V
Data Retention Current	I <sub>DR</sub>	V <sub>CC</sub> =1.5V, I <sub>SB1</sub> Test Condition (Chip Disabled) <sup>1)</sup>	-	-	4	μA
Chip Deselect to Data Retention Time	t <sub>SDR</sub>	See data retention wave form	0	-	-	ns
Operation Recovery Time	t <sub>RDR</sub>		t <sub>RC</sub>	-	-	

#### NOTES

- See the I<sub>SB1</sub> measurement condition of datasheet page 5.

#### DATA RETENTION WAVE FORM





# AS6C8008A Family

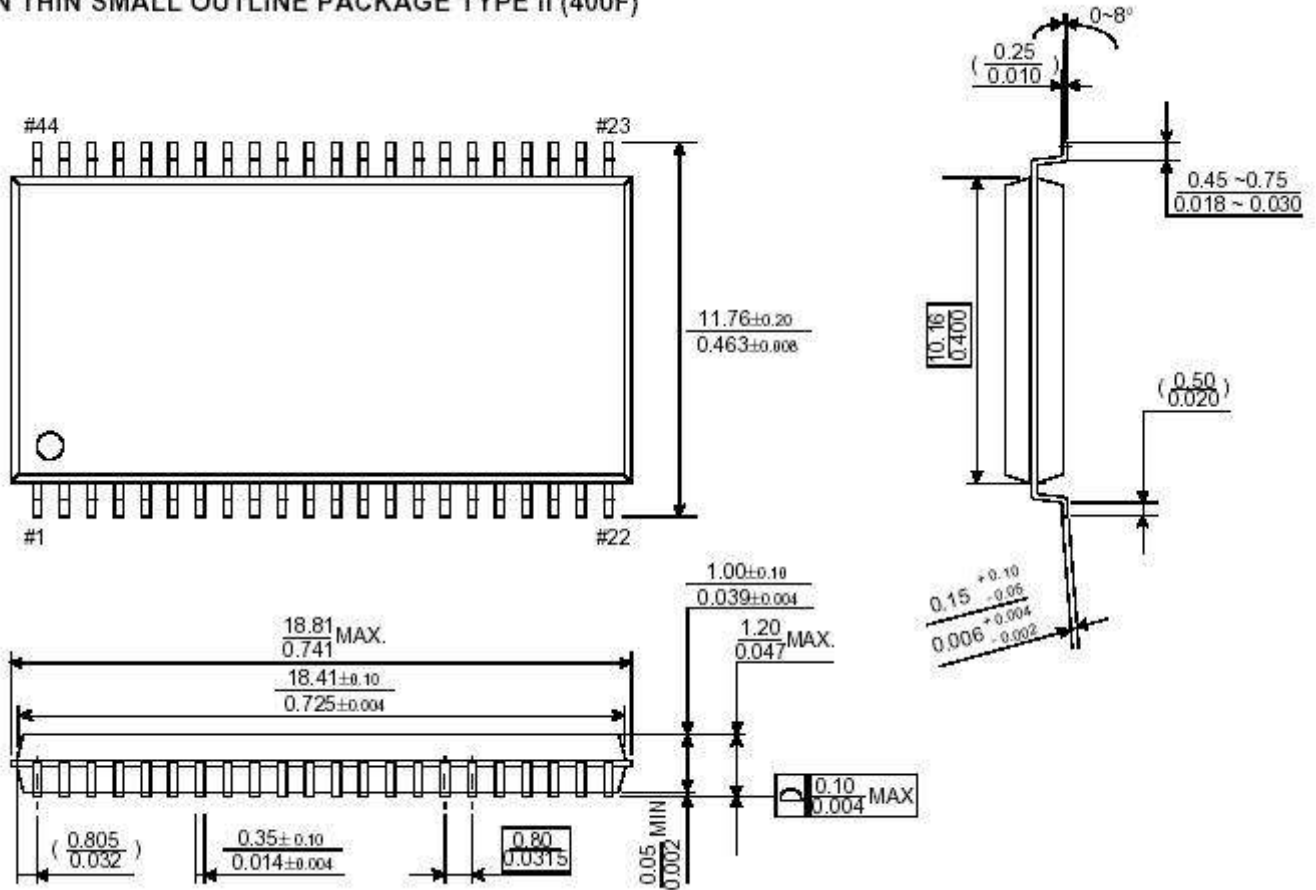
## Low Power, 1Mx8 SRAM

### PACKAGE DIMENSION

44 - TSOP2 (0.8mm pin pitch)

44 PIN THIN SMALL OUTLINE PACKAGE TYPE II (400F)

Unit : millimeters / inches



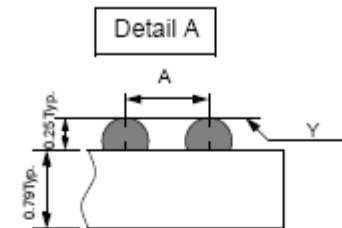
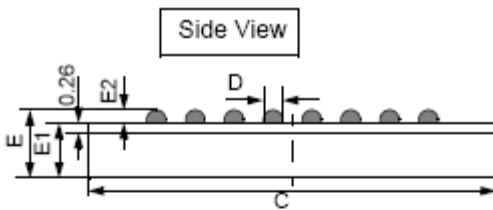
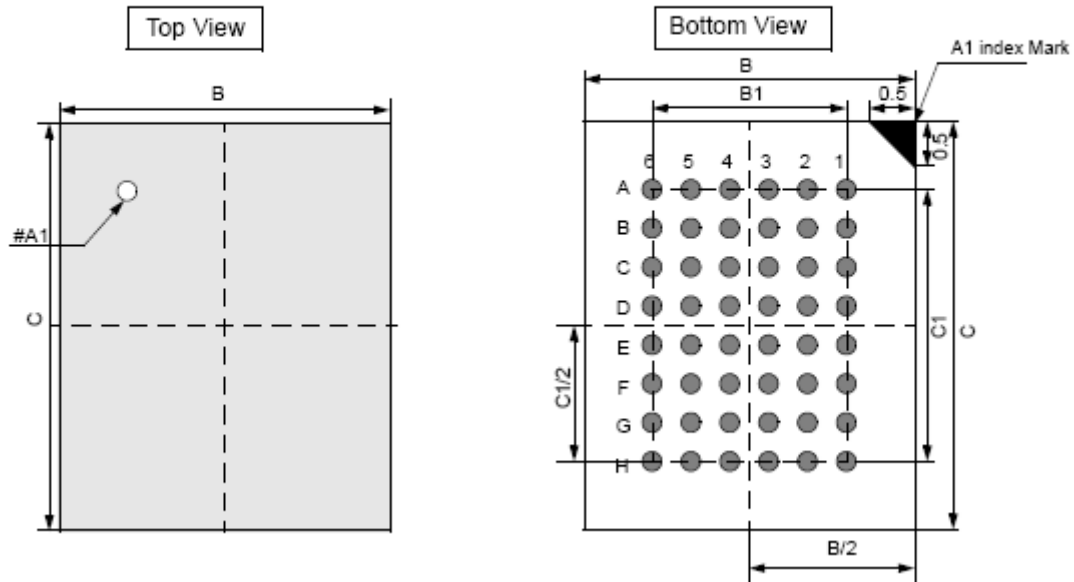
B	7.95	8.00	8.05
B1	-	3.75	-
C	9.95	10.00	10.05
C1	-	5.25	-
D	0.30	0.35	0.40
E	-	-	1.00
E1	-	-	0.70

**NOTES.**

1. Bump counts : 48(8row x 6column)
2. Bump pitch : (x,y)=(0.75x0.75) (typ.)
3. All tolerance are +/-0.050 unless otherwise specified.
4. Typ : Typical
5. Y is coplanarity : 0.08(Max)

48 Ball Fine Pitch BGA (0.75mm ball pitch)

Unit: millimeters



	Min	Typ	Max
A	-	0.75	-
B	7.95	8.00	8.05
B1	-	3.75	-
C	9.95	10.00	10.05
C1	-	5.25	-
D	0.30	0.35	0.40
E	-	-	1.00
E1	-	-	0.70
E2	0.20	0.25	0.30
Y	-	-	0.08

**NOTES.**

1. Bump counts : 48(8row x 6column)
2. Bump pitch : (x,y)=(0.75x0.75) (typ.)
3. All tolerance are +/-0.050 unless otherwise specified.
4. Typ : Typical
5. Y is coplanarity : 0.08(Max)