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RClamp1224S Low Capacitance TVS for ADSL Interfaces

PROTECTION PRODUCTS - RailClamp®

Description

RailClamp® TVS arrays are ultra low capacitance ESD protection devices designed to protect high speed data interfaces. This series has been specifically designed to protect sensitive components which are connected to high-speed data and transmission lines from overvoltage caused by ESD (electrostatic discharge), CDE (Cable Discharge Events), and EFT (electrical fast transients).

These devices integrate low capacitance, surge-rated compensation diodes with high power transient voltage suppressors (TVS). The capacitance of the device is limited to 3pF maximum to ensure correct signal transmission on high-speed lines.

The RClamp®1224S is in a 6-pin SOT-23 package. The leads are finished with lead-free matte tin. They are particularly well suited for applications where board space is at a premium. The RClamp1224S may be used to protect xDSL interfaces, multi-protocol serial transceivers, portable electronics, and wireless systems.

Features

- ◆ Transient protection for high-speed data lines to **IEC 61000-4-2 (ESD) ±15kV (air), ±8kV (contact)**
IEC 61000-4-4 (EFT) 40A (5/50ns)
IEC 61000-4-5 (Lightning) , 15A (8/20µs)
- ◆ Optimized for easy PCB layout
- ◆ Low capacitance: **3pF**
- ◆ Operating voltage: **12V**
- ◆ Low clamping voltage
- ◆ Small Package saves board space
- ◆ Solid-state technology

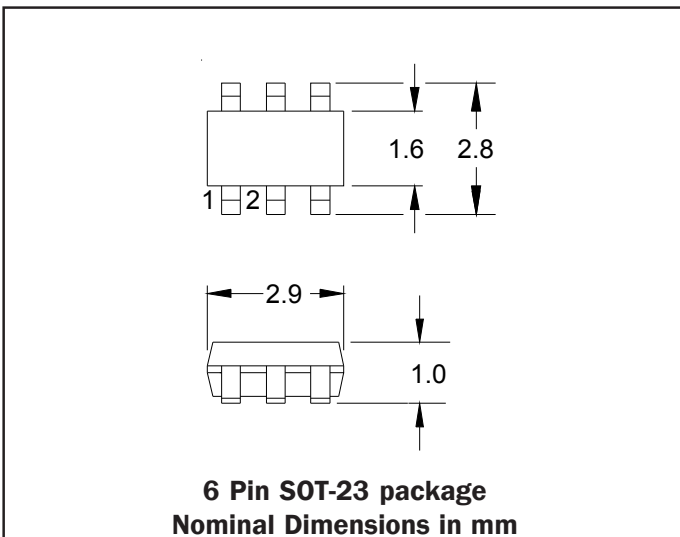
Mechanical Characteristics

- ◆ JEDEC SOT-23 6L package
- ◆ Pb-Free, Halogen Free, RoHS/WEEE Compliant
- ◆ Nominal Dimensions: 2.9 x 2.8mm
- ◆ Molding compound flammability rating: UL 94V-0
- ◆ Marking: Marking Code + Date Code
- ◆ Packaging: Tape and Reel

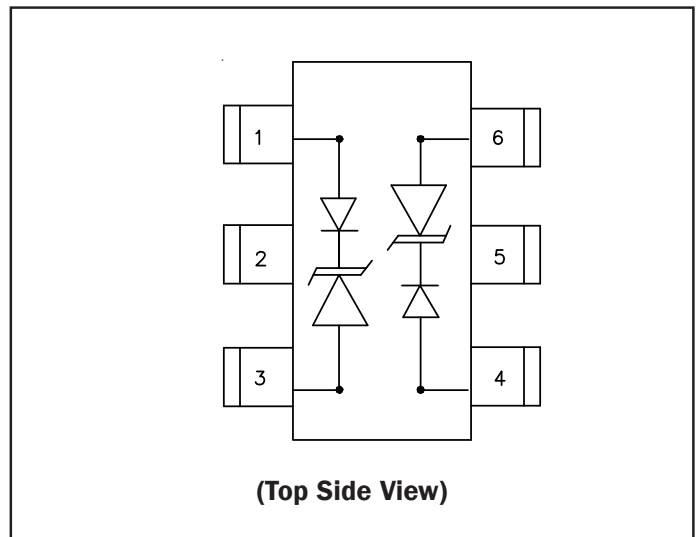
Applications

- ◆ xDSL Interfaces
- ◆ RS-232, RS-422 Interfaces
- ◆ Multi-Protocol Serial Transceivers
- ◆ High-Speed Data Lines
- ◆ WAN/LAN Equipment
- ◆ Carrier Class Equipment
- ◆ Customer Premise Equipment

Package Dimensions



Schematic & Pin Configuration





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Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Power (tp = 8/20μs)	P _{pk}	400	Watts
Peak Pulse Current (tp = 8/20μs)	I _{pp}	15	A
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V _{ESD}	15 8	kV
Operating Temperature	T _j	-40 to +85	°C
Storage Temperature	T _{stg}	-55 to +150	°C

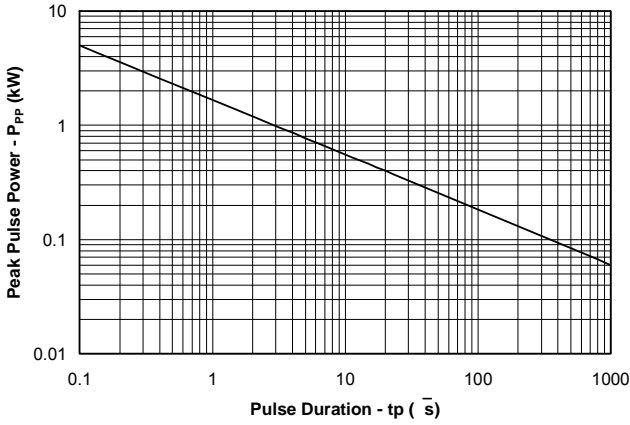
Electrical Characteristics (T=25°C unless otherwise specified)

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V _{RWM}				12	V
Reverse Breakdown Voltage	V _{BR}	I _t = 1mA	13.3			V
Reverse Leakage Current	I _R	V _{RWM} = 12V T = 0 - 85°C		0.01	0.02	μA
Clamping Voltage	V _C	I _{pp} = 1A, t _p = 8/20μs			19	V
Clamping Voltage	V _C	I _{pp} = 15A, t _p = 8/20μs			27	V
Junction Capacitance ¹	C _j	Pin 1 to Pin 3 Pin 4 to Pin 6 V _R = 0V - 12V, f = 1MHz		1.5	3	pF

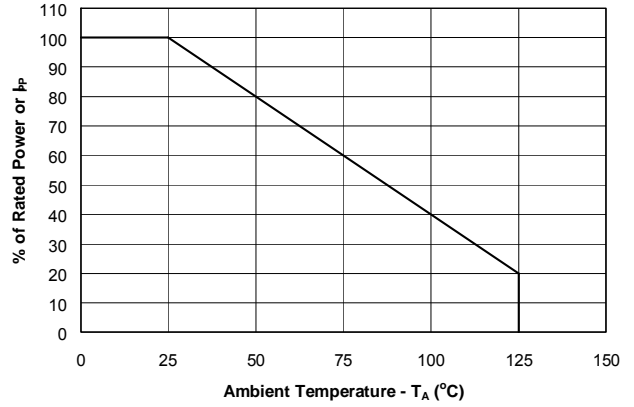
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Typical Characteristics

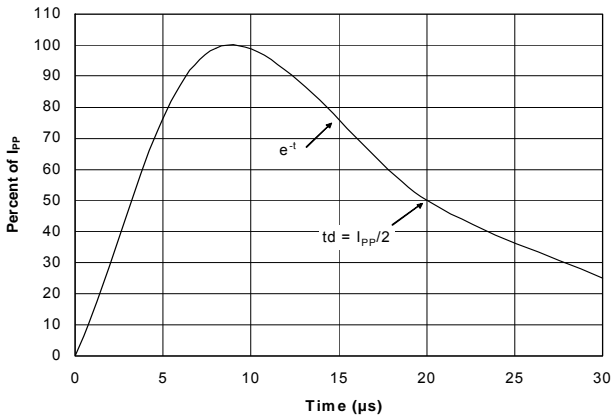
Non-Repetitive Peak Pulse Power vs. Pulse Time



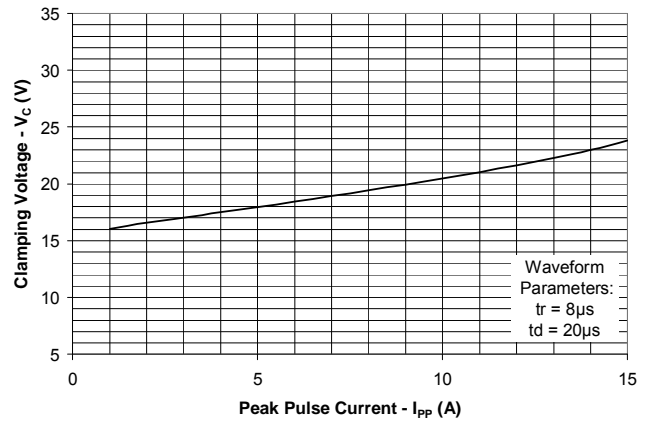
Power Derating Curve



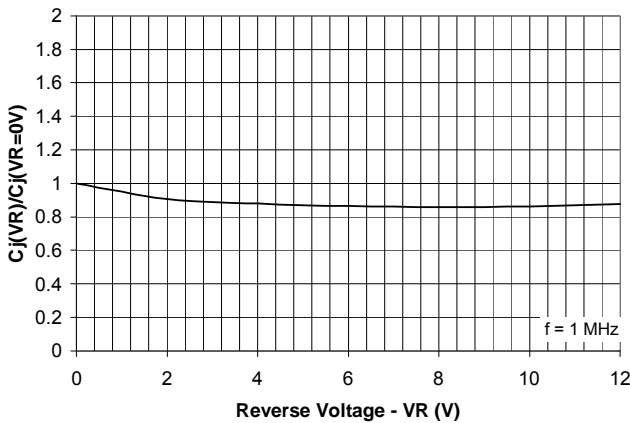
Pulse Waveform



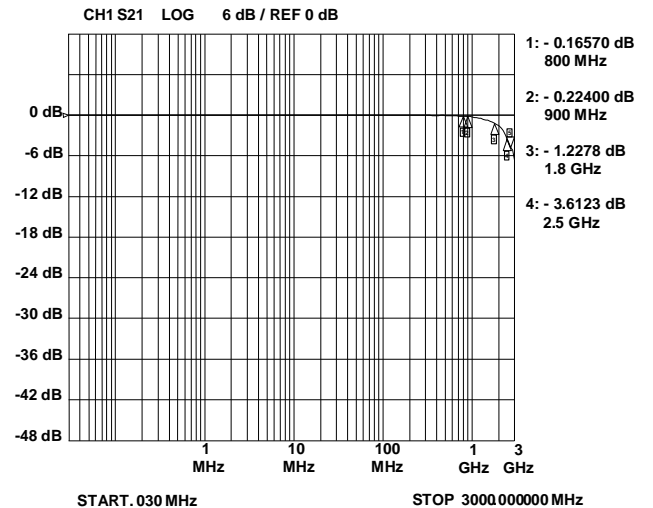
Clamping Voltage vs. Peak Pulse Current



Normalized Junction Capacitance vs. Reverse Voltage (Line-to-Ground)



Typical Insertion Loss S21 (Each Line)



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Applications Information

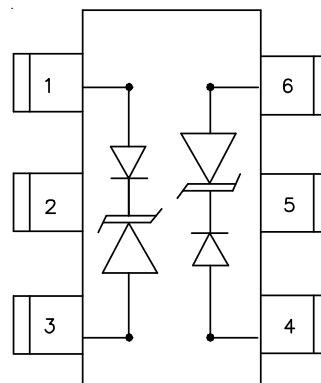
Device Connection for Metallic Protection of High-Speed Data Lines

The RClamp1224S is designed to protect high-speed data lines from transient over-voltages which result from lightning and ESD. The device is designed to protect one line in common mode (Line-to-Ground) or one line pair in metallic (Line-to-Line) mode. For metallic mode protection, the input of line 1 is connected at pin 1 and the output is connected at pin 6. Likewise, the input of line 2 is connected at pin 3 and the output is connected at pin 4. For common mode protection, ground either pins 1 and 6 or pins 3 and 4. The ground connection should be made directly to the ground plane for best results.

Matte Tin Lead Finish

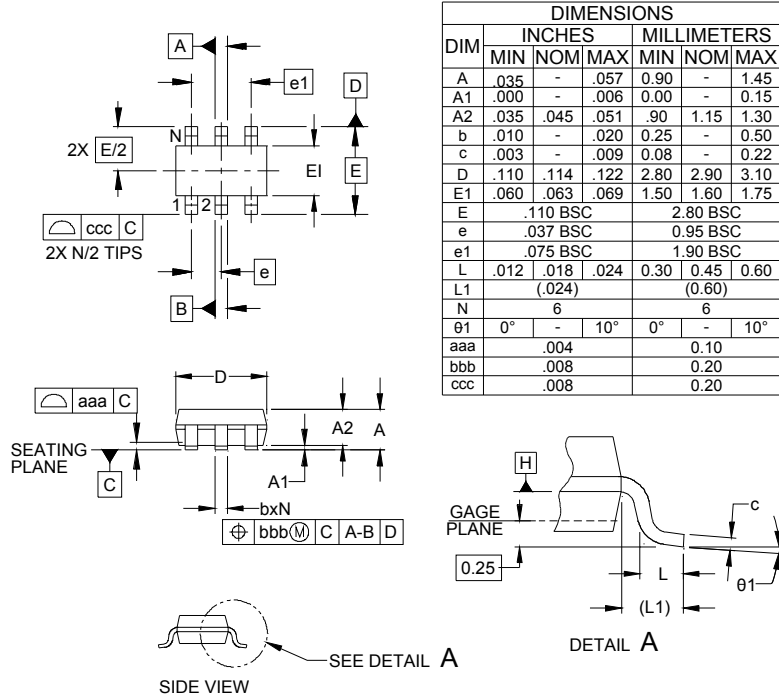
Matte tin has become the industry standard lead-free replacement for SnPb lead finishes. A matte tin finish is composed of 100% tin solder with large grains. Since the solder volume on the leads is small compared to the solder paste volume that is placed on the land pattern of the PCB, the reflow profile will be determined by the requirements of the solder paste. Therefore, these devices are compatible with both lead-free and SnPb assembly techniques. In addition, unlike other lead-free compositions, matte tin does not have any added alloys that can cause degradation of the solder joint.

Pin Configuration (Top Side View)



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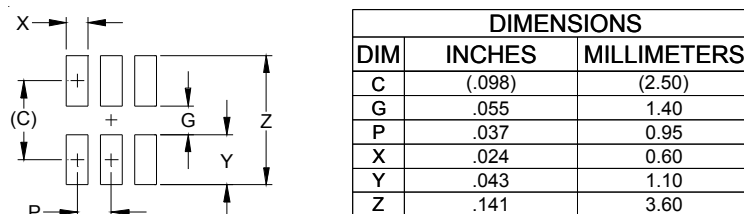
Outline Drawing - SOT-23 6L



NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS **-A-** AND **-B-** TO BE DETERMINED AT DATUM PLANE **-H-**
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

Land Pattern - SOT-23 6L

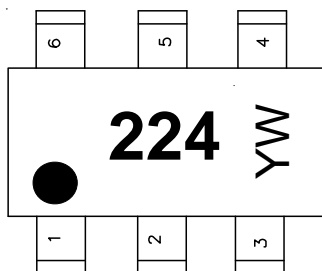


NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

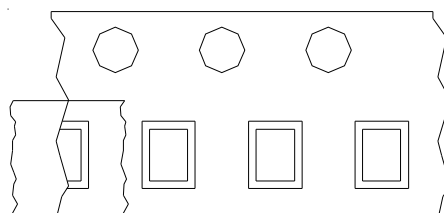
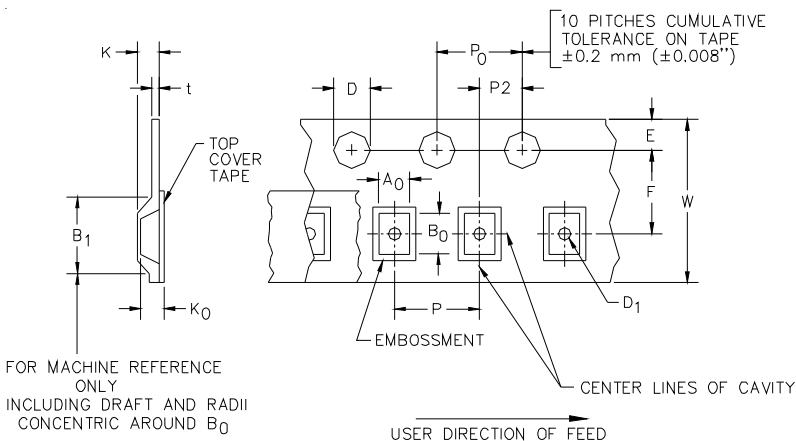
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Marking



YW = 2 - Alphanumeric characters for Date Code

Tape and Reel Specification



Device Orientation in Tape

A0	B0	K0
3.23 +/-0.05 mm	3.17 +/-0.05 mm	1.37 +/-0.05 mm

Tape Width	B ₁ (Max)	D	D1	E	F	K (MAX)	P	P0	P2	T(MAX)	W
8 mm	4.2 mm (.165)	1.5 + 0.1 mm - 0.0 mm	1.0 mm ±0.05	1.750±.10 mm	3.5±0.05 mm	2.4 mm	4.0±0.1 mm	4.0±0.1 mm	2.0±0.05 mm	0.4 mm	8.0 mm + 0.3 mm - 0.1 mm

Contact Information

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