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Maxim Integrated
MAX4551CEE

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Datasheet of MAX4551CEE - IC SW QUAD ANLG ESD SPST 16-QSOP
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19-1391; Rev 0; 10/98

MAXIM

±15kV ESD-Protected, Quad, Low-Voltage, SPST Analog Switches

General Description

The MAX4551/MAX4552/MAX4553 are quad, low-voltage, single-pole/single-throw (SPST) analog switches. Each switch is protected against ±15kV electrostatic discharge (ESD) shocks, without latchup or damage. On-resistance (100Ω max) is matched between switches to 4Ω max, and is flat (8Ω max) over the specified signal range. Each switch can handle Rail-to-Rail® analog signals. The off-leakage current is only 1nA at +25°C and 10nA at +85°C.

The MAX4551 has four normally closed (NC) switches, and the MAX4552 has four normally open (NO) switches. The MAX4553 has two NC and two NO switches.

These CMOS switches can operate with dual power supplies ranging from ±2V to ±6V or a single supply between +2V and +12V. They are fully specified for single +2.7V operation.

All digital inputs have +0.8V and +2.4V logic thresholds, ensuring TTL/CMOS-logic compatibility when using ±5V or a single +5V supply.

Applications

Battery-Operated Equipment
Data Acquisition
Test Equipment
Avionics
Audio Signal Routing
Networking

Features

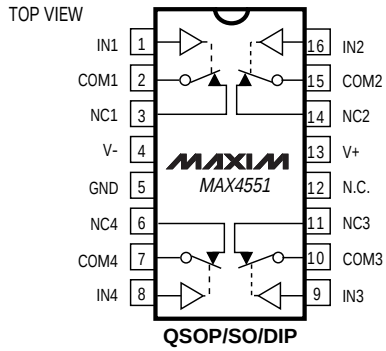
- **±15kV ESD Protection per IEC 1000-4-2**
- **+2V to +12V Single Supply**
  ±2V to ±6V Dual Supplies
- **120Ω Signal Paths with ±5V Supplies**
- **Low Power Consumption: <1µW**
- **4 Separately Controlled SPST Switches**
- **Rail-to-Rail Signal Handling**
- **Pin-Compatible with Industry-Standard DG211/DG212/DG213**
- **TTL/CMOS-Compatible Inputs with Dual ±5V or Single +5V Supply**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX4551CEE	0°C to +70°C	16 QSOP
MAX4551CSE	0°C to +70°C	16 Narrow SO
MAX4551CPE	0°C to +70°C	16 Plastic DIP
MAX4551C/D	0°C to +70°C	Dice*
MAX4551EEE	-40°C to +85°C	16 QSOP
MAX4551ESE	-40°C to +85°C	16 Narrow SO
MAX4551EPE	-40°C to +85°C	16 Plastic DIP

Ordering Information continued at end of data sheet.
**Contact factory for dice specifications.*

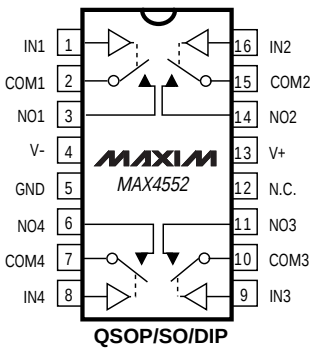
Pin Configurations/Functional Diagrams/Truth Tables



QSOP/SO/DIP

MAX4551	
LOGIC	SWITCH
0	ON
1	OFF

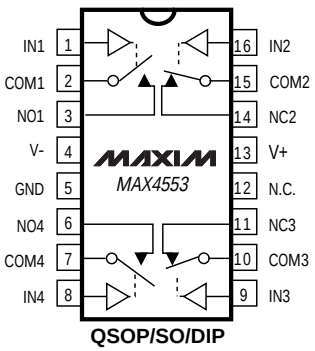
N.C. = NOT CONNECTED



QSOP/SO/DIP

MAX4552	
LOGIC	SWITCH
0	OFF
1	ON

SWITCHES SHOWN FOR LOGIC "0" INPUT



QSOP/SO/DIP

MAX4553		
LOGIC	SWITCHES 1, 4	SWITCHES 2, 3
0	OFF	ON
1	ON	OFF

Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.

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ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to GND
V+ .....-0.3V to +13.0V
V- .....-13.0V to +0.3V
V+ to V- .....-0.3V to +13.0V
All Other Pins (Note 1) .....(V- - 0.3V) to (V+ + 0.3V)
Continuous Current into Any Terminal .....±10mA
Peak Current into Any Terminal
(pulsed at 1ms,10% duty cycle) .....±20mA
ESD per Method 3015.7 (IN_, COM_, V+, V-, GND) .....>2500V
IEC 1000-4-2 (NO_, NC_) .....±15kV

Continuous Power Dissipation (T_A = +70°C)
QSOP (derate 9.52mW/°C above +70°C) 762mW
Narrow SO (derate 8.70mW/°C above +70°C) 696mW
Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
Operating Temperature Ranges
MAX455_C_E .....0°C to +70°C
MAX455_E_E .....-40°C to +85°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Note 1: Signals on NC_, NO_, COM_, or IN_ exceeding V+ or V- are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = +5V, ±10%, V- = -5V, ±10%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range (Note 3)	$V_{COM_}$, $V_{NO_}$, $V_{NC_}$		C, E	V-		V+	V
COM_ to NO_, COM_ to NC_ On-Resistance	R_{ON}	V+ = 5V, V- = -5V, $V_{NO_}$ or $V_{NC_}$ = ±3V, $I_{COM_}$ = 1mA	+25°C		80	120	Ω
			C, E			140	
COM_ to NO_, COM_ to NC_ On-Resistance Match Between Channels (Note 4)	ΔR_{ON}	V+ = 5V, V- = -5V, $V_{NO_}$ or $V_{NC_}$ = ±3V, $I_{COM_}$ = 1mA	+25°C		1	4	Ω
			C, E			5	
COM_ to NO_, COM_ to NC_ On-Resistance Flatness (Note 5)	$R_{FLAT(ON)}$	V+ = 5V, V- = -5V, $V_{NO_}$ or $V_{NC_}$ = +3V, 0, -3V	+25°C		4	8	Ω
			C, E			10	
NO_, NC_ Off-Leakage Current (Note 6)	$I_{NO_(OFF)}$, $I_{NC_(OFF)}$	V+ = 5.5V, V- = -5.5V, $V_{COM_}$ = ∓4.5V, $V_{NO_}$ = ±4.5V	+25°C	-1	0.01	1	nA
			C, E	-10		10	
COM_ Off-Leakage Current (Note 6)	$I_{COM_(OFF)}$	V+ = 5.5V, V- = -5.5V, $V_{COM_}$ = ±4.5V, $V_{NO_}$ = ∓ 4.5V	+25°C	-1	0.01	1	nA
			C, E	-10		10	
COM_ On-Leakage Current (Note 6)	$I_{COM_(ON)}$	V+ = 5.5V, V- = -5.5V, $V_{COM_}$ = ±4.5V	+25°C	-2	0.01	2	nA
			C, E	-20		20	

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ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = +5V, ±10%, V- = -5V, ±10%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP (Note 2)	MAX	UNITS
LOGIC INPUT							
IN_ Input Logic Threshold High	V_{IN_H}		C, E	2.4	1.6		V
IN_ Input Logic Threshold Low	V_{IN_L}		C, E		1.6	0.8	V
IN_ Input Current Logic High or Low	$I_{INH_}$, $I_{INL_}$	$V_{IN_}$ = 0.8V or 2.4V	C, E	-1	0.03	1	µA
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time	t_{ON}	$V_{COM_}$ = ±3V, V+ = 5V, V- = -5V, Figure 1	+25°C		70	110	ns
			C, E			125	
Turn-Off Time	t_{OFF}	$V_{COM_}$ = ±3V, V+ = 5V, V- = -5V, Figure 1	+25°C		50	90	ns
			C, E			100	
Break-Before-Make Time Delay (MAX4553 Only)	t_{BBM}	$V_{COM_}$ = ±3V, V+ = 5V, V- = -5V, Figure 2	+25°C	5	20		ns
Charge Injection (Note 3)	Q	C_L = 1nF, $V_{NO_}$ = 0, R_S = 0, Figure 3	+25°C		2	5	pC
NO_, NC_ Off-Capacitance	$C_{N_(OFF)}$	$V_{NO_}$ = GND, f = 1MHz, Figure 6	+25°C		3.5		pF
COM_ Off-Capacitance	$C_{COM_(OFF)}$	$V_{COM_}$ = GND, f = 1MHz, Figure 6	+25°C		3		pF
COM_ On-Capacitance	$C_{COM_(ON)}$	$V_{COM_}$ = $V_{NO_}$ = GND, f = 1MHz, Figure 7	+25°C		10		pF
Off-Isolation (Note 7)	V_{ISO}	R_L = 50Ω, C_L = 15pF, $V_{N_}$ = $1V_{RMS}$, f = 100kHz, Figure 4	+25°C		< -90		dB
Channel-to-Channel Crosstalk (Note 8)	V_{CT}	R_L = 50Ω, C_L = 15pF, $V_{N_}$ = $1V_{RMS}$, f = 100kHz, Figure 5	+25°C		< -90		dB
POWER SUPPLY							
Power-Supply Range	V+, V-		C, E	±2		±6	V
V+ Supply Current	I+	V+ = 5.5V, all $V_{IN_}$ = 0 or V+	+25°C	-1	0.05	1	µA
			C, E	-1		1	
V- Supply Current	I-	V- = -5.5V	+25°C	-1	0.05	1	µA
			C, E	-1		1	
ESD PROTECTION							
On NC_ and NO_ Pins per IEC 801-2		Contact Discharge IEC 1000-4-2	+25°C		±8		kV
		Air Discharge IEC 1000-4-2	+25°C		±15		
		Human Body Model	+25°C		±15		
All Pins		MIL-STD-883C Method 3015	+25°C		±2.5		kV

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±15kV ESD-Protected, Quad, Low-Voltage, SPST Analog Switches

ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V+ = +5V, ±10%, V- = -5V, ±10%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	$V_{COM_}$, $V_{NO_}$, $V_{NC_}$	(Note 3)	C, E	0		V+	V
COM_ to NO_, COM_ to NC_ On-Resistance	R_{ON}	V+ = 5V, $V_{COM_}$ = 3.5V, $I_{COM_}$ = 1mA	+25°C		115	160	Ω
			C, E			180	
COM_ to NO_, COM_ to NC_ On-Resistance Match Between Channels (Note 4)	ΔR_{ON}	V+ = 5V, $V_{COM_}$ = 3.5V, $I_{COM_}$ = 1mA	+25°C		2	6	Ω
			C, E			8	
NO_, NC_ Off-Leakage Current (Notes 6, 9)	$I_{NO_(OFF)}$, $I_{NC_(OFF)}$	V+ = 5.5V; $V_{COM_}$ = 1V, 4.5V; $V_{N_}$ = 4.5V, 1V	+25°C	-1	0.01	1	nA
			C, E	-10		10	
COM_ Off-Leakage Current (Notes 6, 9)	$I_{COM_(OFF)}$	V+ = 5.5V; $V_{COM_}$ = 1V, 4.5V; $V_{N_}$ = 4.5V, 1V	+25°C	-1	0.01	1	nA
			C, E	-10		10	
COM_ On-Leakage Current (Notes 6, 9)	$I_{COM_(ON)}$	V+ = 5.5V; $V_{COM_}$ = 4.5V, 1V	+25°C	-2	0.01	2	nA
			C, E,	-20		20	
LOGIC INPUT							
IN_ Input Logic Threshold High	V_{IN_H}		C, E	2.4	1.6		V
IN_ Input Logic Threshold Low	V_{IN_L}		C, E		1.6	0.8	V
IN_ Input Current Logic High or Low	$I_{INH_}$, $I_{INL_}$	$V_{IN_}$ = 0.8V or 2.4V	C, E	-1		1	µA
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time	t_{ON}	$V_{COM_}$ = 3V, V+ = 5V, Figure 1	+25°C		100	160	ns
			C, E			170	
Turn-Off Time	t_{OFF}	$V_{COM_}$ = 3V, V+ = 5V, Figure 1	+25°C		80	140	ns
			C, E			150	
Break-Before-Make Time Delay (MAX4553 Only)	t_{BBM}	$V_{COM_}$ = 3V, V+ = 5V, Figure 2	+25°C	5	30		ns
Charge Injection (Note 3)	Q	C_L = 1nF, $V_{NO_}$ = 0, R_S = 0, Figure 3	+25°C		1	5	pC
POWER SUPPLY							
V+ Supply Current	I+	V+ = 5.5V, all $V_{IN_}$ = 0 or V+	+25°C	-1	0.05	1	µA
			C, E	-1		1	
ESD PROTECTION							
On NC_ and NO_ Pins per IEC 801-2		Contact Discharge IEC 1000-4-2	+25°C		±8		kV
		Air Discharge IEC 1000-4-2	+25°C		±15		
		Human Body Model	+25°C		±15		
All Pins		MIL-STD-883C Method 3015	+25°C		±2.5		kV

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ELECTRICAL CHARACTERISTICS—Single +3V Supply

(V+ = +2.7V to +3.6V, V- = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range (Note 3)	$V_{COM_}$, $V_{NO_}$, $V_{NC_}$		C, E	0		V+	V
COM_ to NO_, COM_ to NC_ On-Resistance	R_{ON}	V+ = 2.7V, $V_{COM_}$ = 1.0V, $I_{COM_}$ = 0.1mA	+25°C		200	400	Ω
			C, E			500	
LOGIC INPUT							
IN_ Input Logic Threshold High	V_{IN_H}		C, E	2.0	1.1		V
IN_ Input Logic Threshold Low	V_{IN_L}		C, E		1.1	0.5	V
IN_ Input Current Logic High or Low	$I_{INH_}$, $I_{INL_}$	$V_{IN_}$ = 0.8V or 2.4V	C, E	-1	0.03	1	µA
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time	t_{ON}	$V_{COM_}$ = 1.5V, V+ = 2.7V, Figure 1	+25°C		190	350	ns
			C, E			400	
Turn-Off Time	t_{OFF}	$V_{COM_}$ = 1.5V, V+ = 2.7V, Figure 1	+25°C		160	250	ns
			C, E			300	
Break-Before-Make Time Delay (MAX4553 Only)	t_{BBM}	$V_{COM_}$ = 1.5V, V+ = 3.6V, Figure 2	+25°C	10	50		ns
Charge Injection	Q	C_L = 1nF, $V_{NO_}$ = 0, R_S = 0, Figure 3	+25°C		1	5	pC
POWER SUPPLY							
V+ Supply Current	I+	V+ = 3.6V, all $V_{IN_}$ = 0 or V+	+25°C	-1	0.05	1	µA
			C, E	-1		1	
ESD PROTECTION							
On NC_ and NO_ Pins per IEC 801-2		Contact Discharge IEC 1000-4-2	+25°C		±8		kV
		Air Discharge IEC 1000-4-2	+25°C		±15		
		Human Body Model	+25°C		±15		
All Pins		MIL-STD-883C Method 3015	+25°C		±2.5		kV

Note 2: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.
Note 3: Guaranteed by design.
Note 4: $\Delta R_{ON} = \Delta R_{ON(MAX)} - \Delta R_{ON(MIN)}$.
Note 5: Resistance flatness is defined as the difference between the maximum and minimum on-resistance values, as measured over the specified analog signal range.
Note 6: Leakage parameters are 100% tested at maximum rated temperature, and guaranteed by correlation at T_A = +25°C.
Note 7: Off-isolation = 20log10 [$V_{COM_}$ / ($V_{NC_}$ or $V_{NO_}$)], $V_{COM_}$ = output, $V_{NC_}$ or $V_{NO_}$ = input to off switch.
Note 8: Between any two switches.
Note 9: Leakage testing for single-supply operation is guaranteed by testing with dual supplies.

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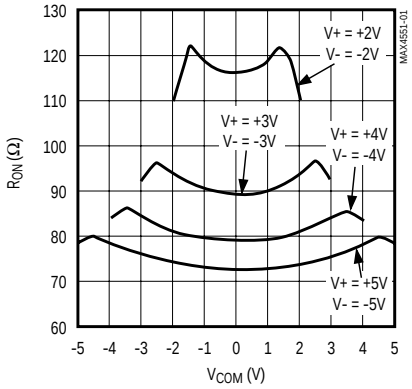
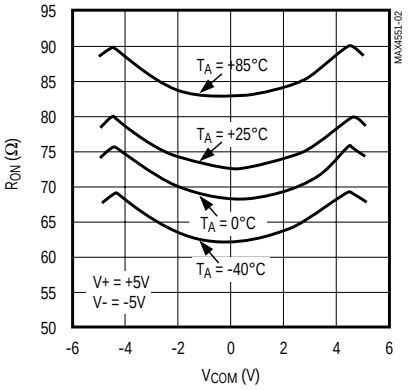
Typical Operating Characteristics

(V+ = +5V, V- = -5V, GND = 0, T_A = +25°C, unless otherwise noted.)

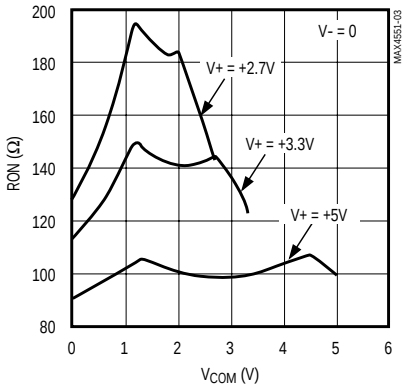
ON-RESISTANCE vs. V_{COM} (DUAL SUPPLIES)



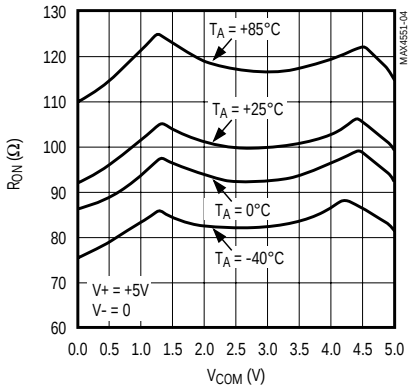
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE (DUAL SUPPLIES)



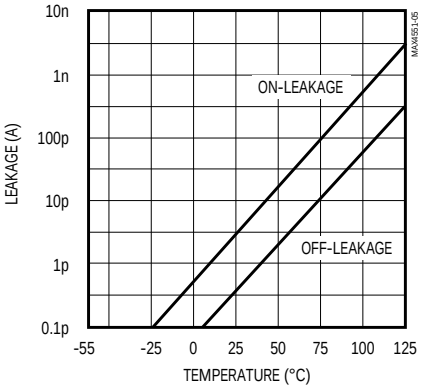
ON-RESISTANCE vs. V_{COM} (SINGLE SUPPLY)



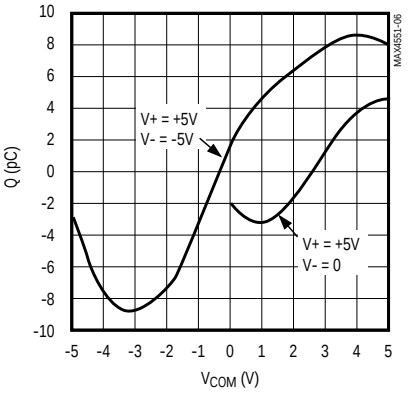
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE (SINGLE SUPPLY)



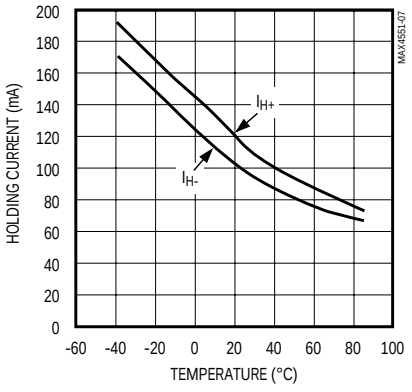
ON- AND OFF-LEAKAGE CURRENT vs. TEMPERATURE



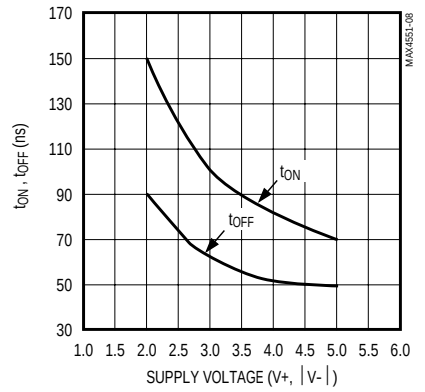
CHARGE INJECTION vs. V_{COM}



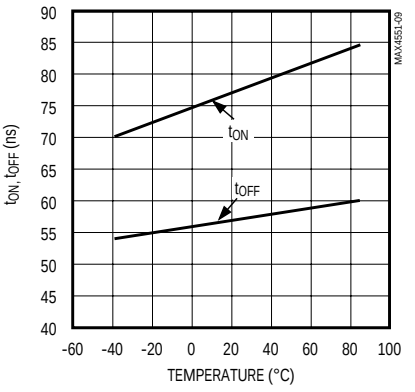
SCR HOLDING CURRENT vs. TEMPERATURE



TURN-ON/TURN-OFF TIME vs. SUPPLY VOLTAGE



TURN-ON/TURN-OFF TIME vs. TEMPERATURE



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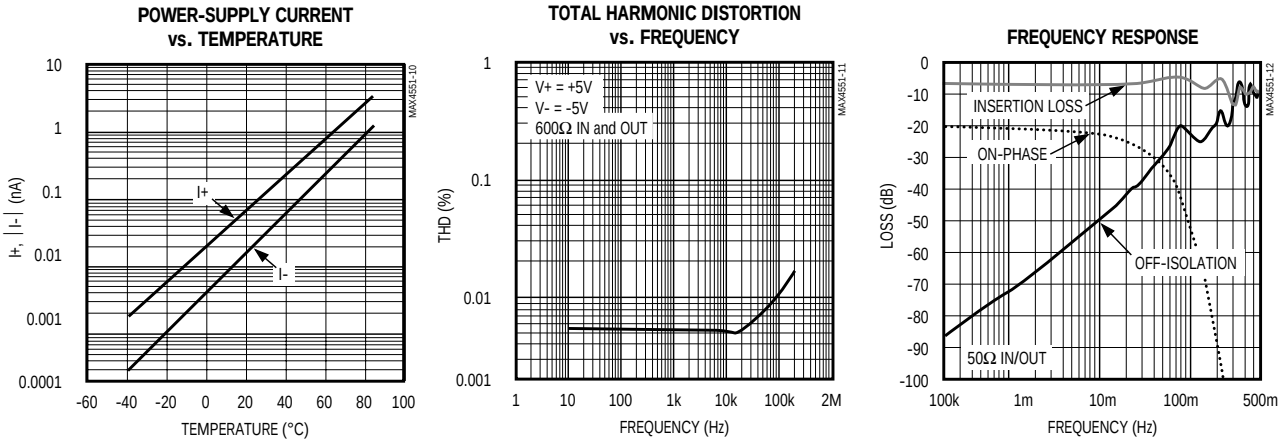
Typical Operating Characteristics (continued)

(V+ = +5V, V- = -5V, GND = 0, T_A = +25°C, unless otherwise noted.)



Pin Description

PIN			NAME	FUNCTION
MAX4551	MAX4552	MAX4553		
1, 16, 9, 8	1, 16, 9, 8	1, 16, 9, 8	IN1–IN4	Logic-Control Digital Inputs
2, 15, 10, 7	2, 15, 10, 7	2, 15, 10, 7	COM1–COM4	Analog Switch Common* Terminals
3, 14, 11, 6	—	—	NC1–NC4	Analog Switch Normally Closed Terminals
—	3, 14, 11, 6	—	NO1–NO4	Analog Switch Normally Open Terminals
—	—	3, 6	NO1, NO4	Analog Switch Normally Open Terminals
—	—	14, 11	NC2, NC3	Analog Switch Normally Closed Terminals
4	4	4	V-	Negative Analog Supply-Voltage Input. Connect to GND for single-supply operation.
5	5	5	GND	Ground. Connect to digital ground. (Analog signals have no ground reference; they are limited to V+ and V-.)
12	12	12	N.C.	No Connection. Not internally connected.
13	13	13	V+	Positive Analog and Digital Supply Voltage Input. Internally connected to substrate.

**NO_ (or NC_) and COM_ pins are identical and interchangeable. Either may be considered as an input or output; signals pass equally well in either direction.*

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±15kV ESD-Protected, Quad, Low-Voltage, SPST Analog Switches

Applications Information

MAX4551/MAX4552/MAX4553 ±15kV ESD Protection

The MAX4551/MAX4552/MAX4553 are ±15kV ESD-protected according to IEC 1000-4-2 at their NC/NO pins. To accomplish this, bidirectional SCRs are included on-chip between these pins and the GND pin. In normal operation, these SCRs are off and have negligible effect on the performance of the switches. When there is an ESD strike at these pins, however, the voltages at these pins go Beyond-the-Rails™ and cause the corresponding SCR(s) to turn on in a few nanoseconds and bypass the surge safely to ground. This method is superior to using diode clamps to the supplies because unless the supplies are very carefully decoupled through low ESR capacitors, the ESD current through the diode clamp could cause a significant spike in the supplies. This may damage or compromise the reliability of any other chip powered by those same supplies.

In the MAX4551/MAX4552/MAX4553, there are diodes to the supplies in addition to the SCRs at the NC/NO pins, but there is a resistance in series with these diodes to limit the current into the supplies during an ESD strike. The diodes are present to protect these pins from overvoltages that are not as a result of ESD strikes like those that may occur due to improper power-supply sequencing.

Once the SCR turns on because of an ESD strike, it continues to be on until the current through it falls below its “holding current.” The holding current is typically 110mA in the positive direction (current flowing into the NC/NO pin) and 95mA in the negative direction at room temperature (see SCR Holding Current vs. Temperature in the *Typical Operating Characteristics*). The system should be designed such that any sources connected to these pins are current limited to a value below these to make sure the SCR turns off when the ESD event gets over to resume normal operation. Also, keep in mind that the holding current varies significantly with temperature. At +85°C, which represents the worst case, the holding currents drop to 70mA and 65mA in the positive and negative directions respectively. Since these are typical numbers, to get guaranteed turn-off of the SCRs under all conditions, the sources connected to these pins should be current limited to not more than half these values. When the SCR is latched, the voltage across it is about ±3V, depending on the polarity of the pin current. The supply voltages do not affect the holding currents appreciably. The sources connected to the COM side of the switches do not need to be current limited since the switches are made to turn off internally when the corresponding SCR(s) get latched.

Even though most of the ESD current flows to GND through the SCRs, a small portion of it goes into the supplies. Therefore, it is a good idea to bypass the supply pins with 100nF capacitors directly to the ground plane.

ESD protection can be tested in various ways. Transmitter outputs and receiver inputs are characterized for protection to the following:

- ±15kV using the Human Body Model
- ±8kV using the Contact Discharge method specified in IEC 1000-4-2 (formerly IEC 801-2)
- ±15kV using the Air-Gap Discharge method specified in IEC 1000-4-2 (formerly IEC 801-2).

ESD Test Conditions

Contact Maxim for a reliability report that documents test setup, methodology, and results.

Human Body Model

Figure 8 shows the Human Body Model, and Figure 9 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

IEC 1000-4-2

The IEC 1000-4-2 standard covers ESD testing and performance of finished equipment; it does not specifically refer to integrated circuits. The MAX4551/MAX4552/MAX4553 enable the design of equipment that meets Level 4 (the highest level) of IEC 1000-4-2, without additional ESD protection components.

The major difference between tests done using the Human Body Model and IEC 1000-4-2 is higher peak current in IEC 1000-4-2. Because series resistance is lower in the IEC 1000-4-2 ESD test model (Figure 10), the ESD withstand voltage measured to this standard is generally lower than that measured using the Human Body Model. Figure 11 shows the current waveform for the ±8kV IEC 1000-4-2 Level 4 ESD Contact Discharge test.

The Air-Gap test involves approaching the device with a charged probe. The Contact Discharge method connects the probe to the device before the probe is energized.

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Power-Supply Considerations

Overview

The MAX4551/MAX4552/MAX4553 construction is typical of most CMOS analog switches. They have three supply pins: V+, V-, and GND. V+ and V- are used to drive the internal CMOS switches, and they set the limits of the analog voltage on any switch. Reverse ESD-protection diodes are internally connected between each analog-signal pin and both V+ and V-. If any analog signal exceeds V+ or V-, one of these diodes conducts. During normal operation these reverse-biased ESD diodes leak, forming the only current drawn from V+ or V-.

Virtually all the analog leakage current is through the ESD diodes. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or V- and the analog signal. This means their leakages vary as the signal varies. The *difference* in the two diode leakages from the signal path to the V+ and V- pins constitutes the analog-signal-path leakage current. All analog leakage current flows to the supply terminals, not to the other switch terminal. This explains how both sides of a given switch can show leakage currents of the same or opposite polarity.

The analog signal paths consist of an N-channel and P-channel MOSFET with their sources and drains paralleled, and their gates driven out of phase to V+ and V- by the logic-level translators.

V+ and GND power the internal logic and logic-level translators, and set the input logic thresholds. The logic-level translators convert the logic levels to switched V+ and V- signals, to drive the gates of the analog switches. This drive signal is the only connection between the logic supplies and the analog supplies. V+ and V- have ESD-protection diodes to GND. The logic-level inputs and output have ESD protection to V+ and to GND.

Increasing V- has no effect on the logic-level thresholds, but it does increase the drive to the P-channel switches, reducing their on-resistance. V- also sets the negative limit of the analog signal voltage.

The logic-level thresholds are CMOS/TTL compatible when V+ = +5V. The threshold increases slightly as V+ is raised, and when V+ reaches +12V, the level threshold is about 3.1V. This is above the TTL output high-level minimum of 2.8V, but still compatible with CMOS outputs.

Bipolar Supplies

The MAX4551/MAX4552/MAX4553 operate with bipolar supplies between ±2V and ±6V. The V+ and V- supplies need not be symmetrical, but their sum cannot exceed the absolute maximum rating of 13.0V. **Do not connect the MAX4551/MAX4552/MAX4553 V+ to +3V, and then connect the logic-level-input pins to TTL logic-level signals. TTL logic-level outputs in excess of the absolute maximum ratings can damage the part and/or external circuits.**

Caution: The absolute maximum V+ to V- differential voltage is 13.0V. Typical ±6V or 12V supplies with ±10% tolerances can be as high as 13.2V. This voltage can damage the MAX4551/MAX4552/MAX4553. Even ±5% tolerance supplies may have overshoot or noise spikes that exceed 13.0V.

Single Supply

The MAX4551/MAX4552/MAX4553 operate from a single supply between +2V and +12V when V- is connected to GND. All of the bipolar precautions must be observed.

High-Frequency Performance

In 50Ω systems, signal response is reasonably flat up to 50MHz (see *Typical Operating Characteristics*). Above 20MHz, the on-response has several minor peaks that are highly layout-dependent. The problem with high-frequency operation is not turning the switch on, but turning it off. The off-state switch acts like a capacitor and passes higher frequencies with less attenuation. At 10MHz, off-isolation is about -52dB in 50Ω systems, becoming worse (approximately 20dB per decade) as frequency increases. Higher circuit impedances also make off-isolation worse. Adjacent channel attenuation is about 3dB above that of a bare IC socket, and is due entirely to capacitive coupling.

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Test Circuits/Timing Diagrams

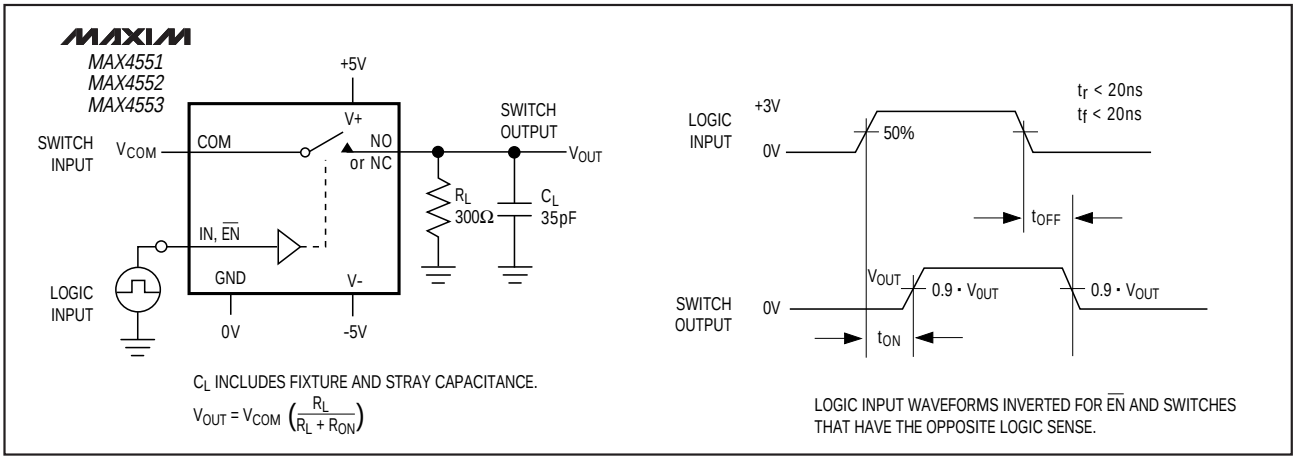

Figure 1. Switching Time

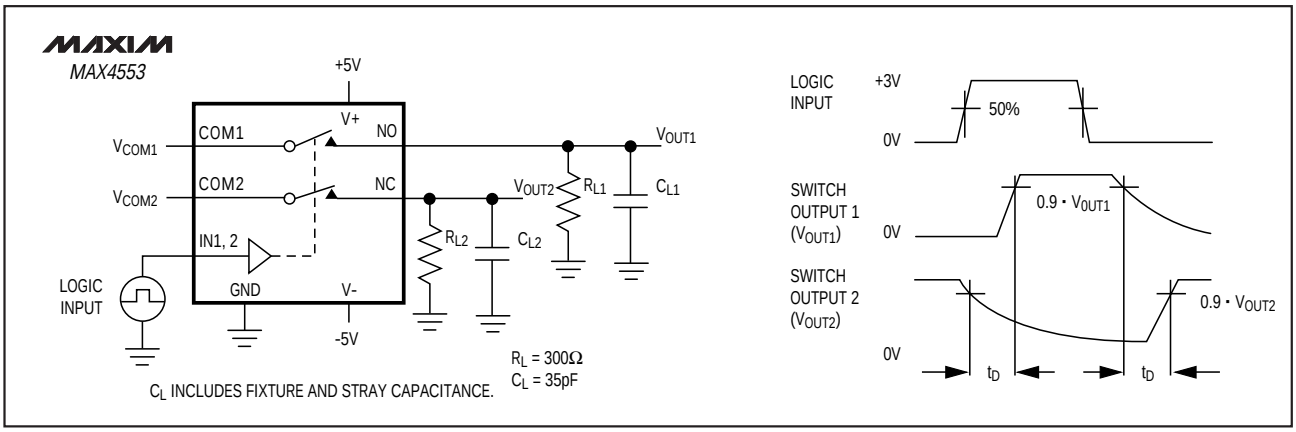

Figure 2. Break-Before-Make Interval (MAX4553 only)

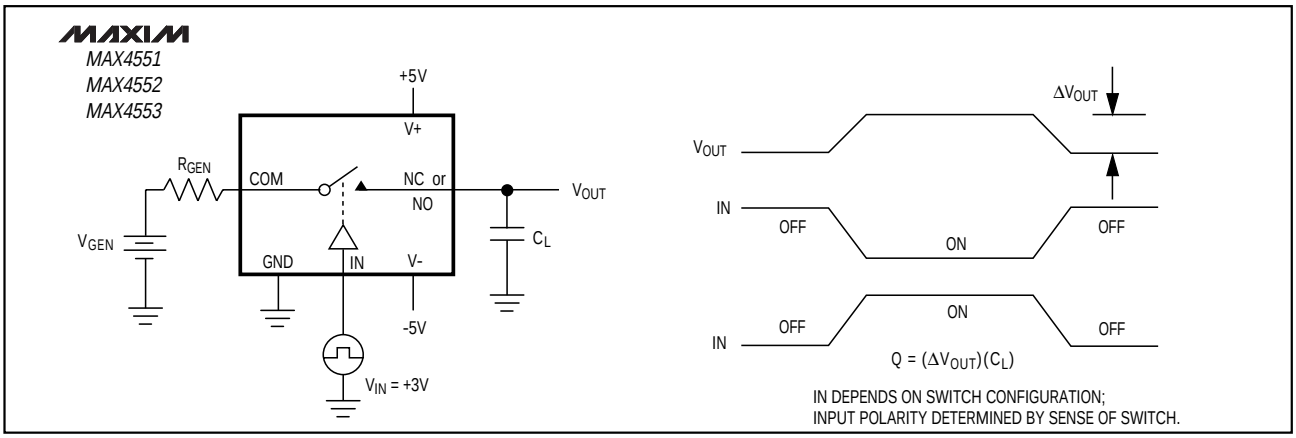

Figure 3. Charge Injection

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Test Circuits/Timing Diagrams (continued)

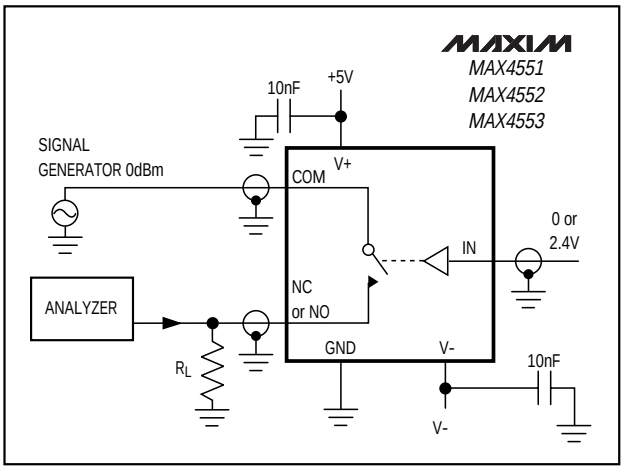

Figure 4. Off-Isolation

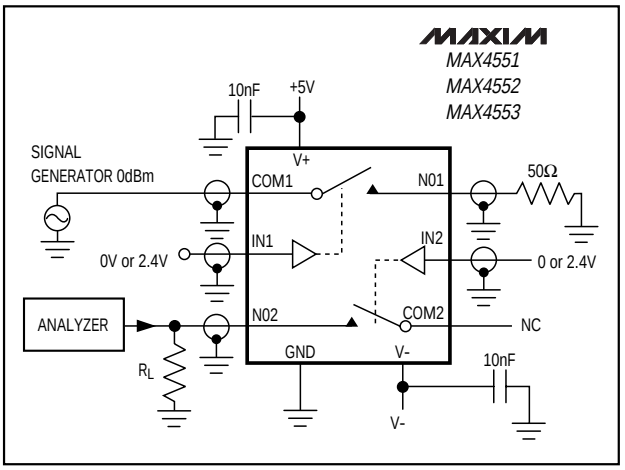

Figure 5. Crosstalk

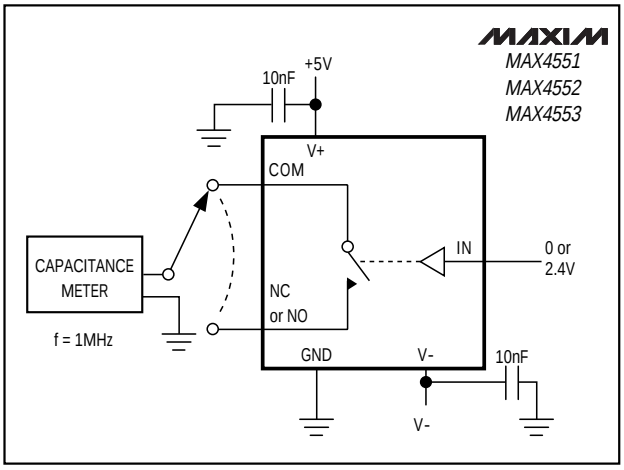

Figure 6. Channel Off-Capacitance

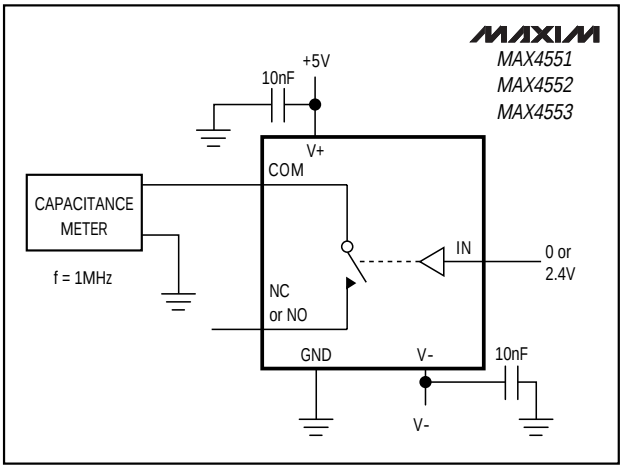

Figure 7. Channel On-Capacitance

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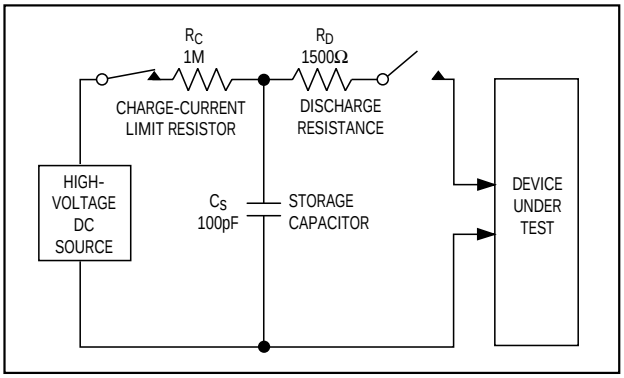

Figure 8. Human Body ESD Test Model

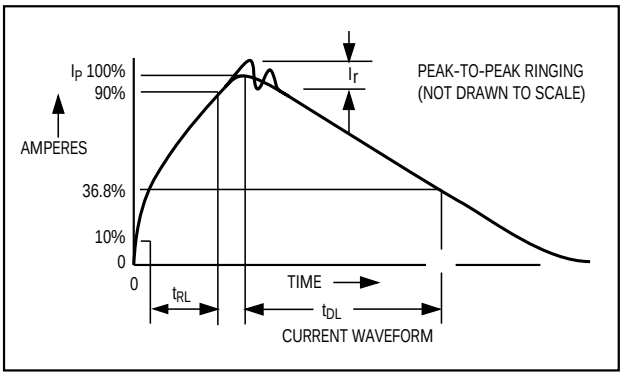

Figure 9. Human Body Model Current Waveform

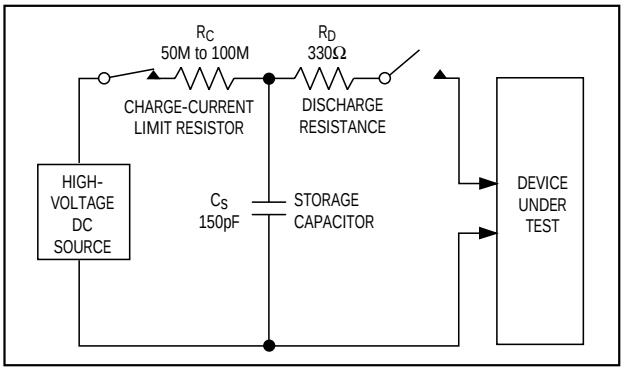

Figure 10. IEC 1000-4-2 ESD Test Model

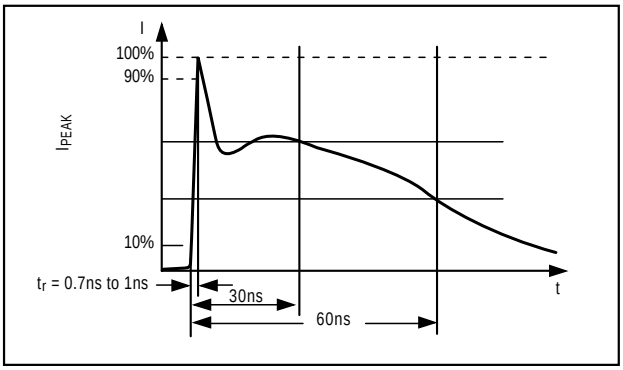

Figure 11. IEC 1000-4-2 ESD Generator Current Waveform

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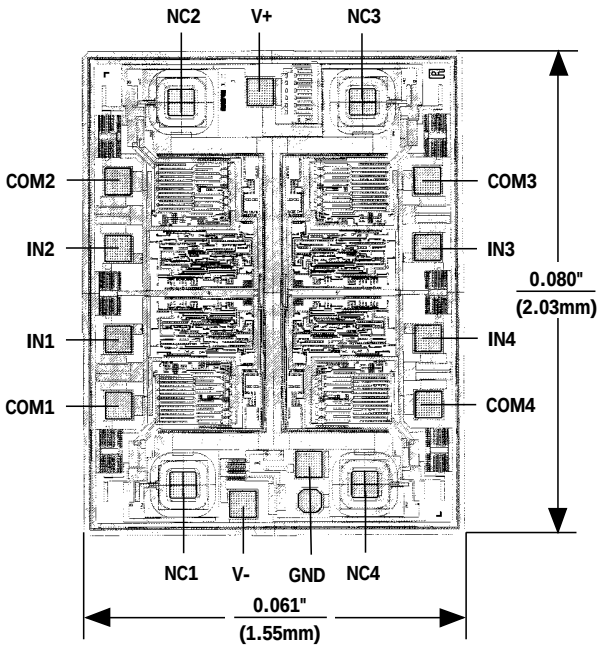
Chip Topographies

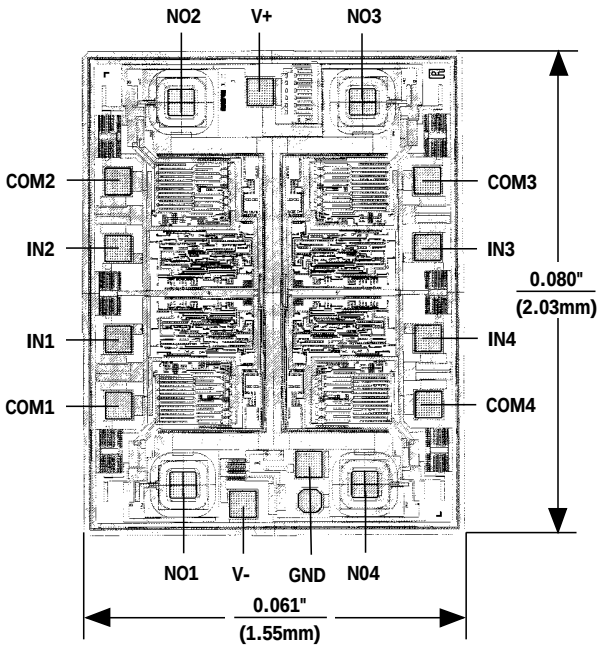
MAX4551



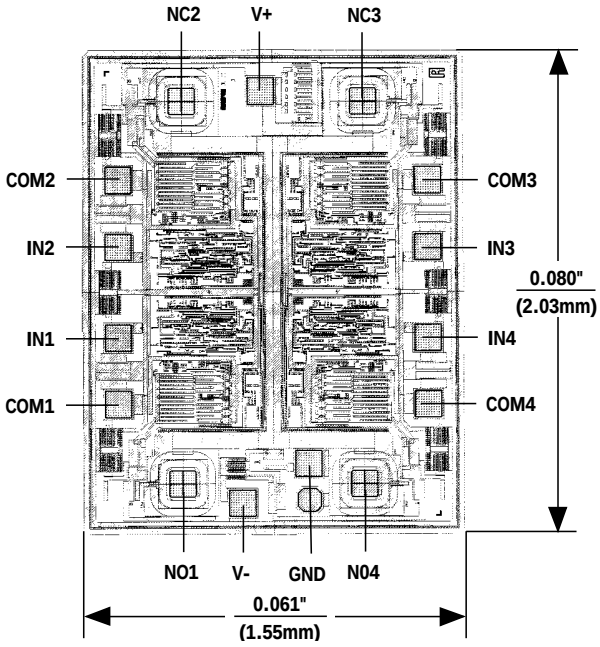
TRANSISTOR COUNT: 126

SUBSTRATE CONNECTED TO GND

MAX4552



MAX4553



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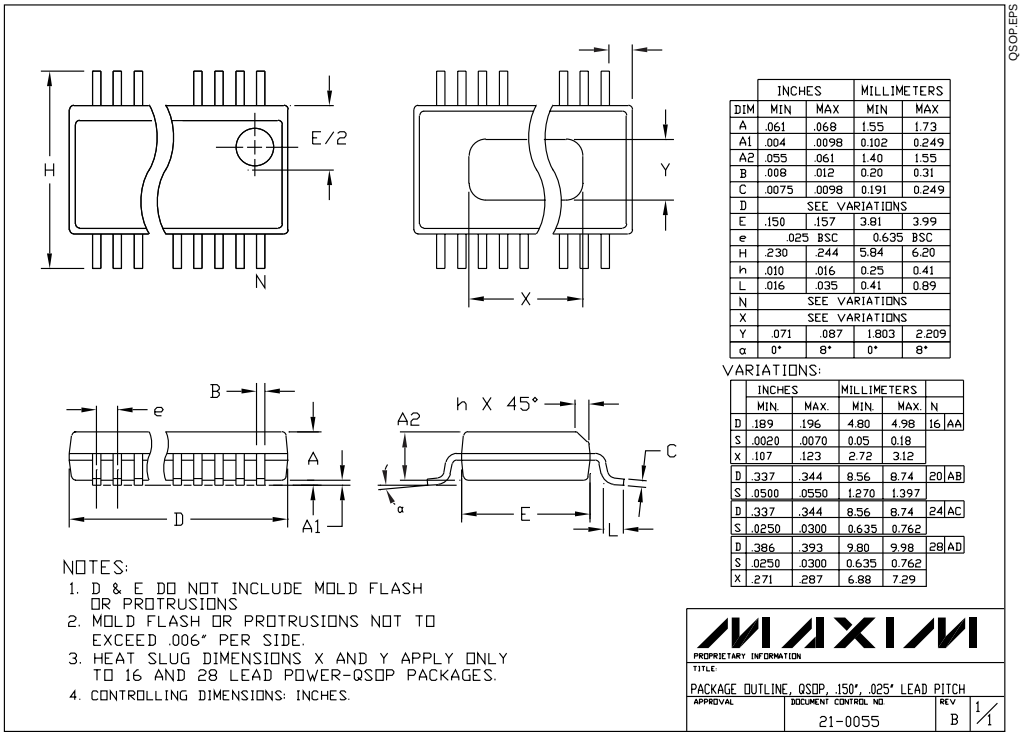
Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX4552CEE	0°C to +70°C	16 QSOP
MAX4552CSE	0°C to +70°C	16 Narrow SO
MAX4552CPE	0°C to +70°C	16 Plastic DIP
MAX4552C/D	0°C to +70°C	Dice*
MAX4552EEE	-40°C to +85°C	16 QSOP
MAX4552ESE	-40°C to +85°C	16 Narrow SO
MAX4552EPE	-40°C to +85°C	16 Plastic DIP
MAX4553CEE	0°C to +70°C	16 QSOP
MAX4553CSE	0°C to +70°C	16 Narrow SO
MAX4553CPE	0°C to +70°C	16 Plastic DIP
MAX4553C/D	0°C to +70°C	Dice*
MAX4553EEE	-40°C to +85°C	16 QSOP
MAX4553ESE	-40°C to +85°C	16 Narrow SO
MAX4553EPE	-40°C to +85°C	16 Plastic DIP

**Contact factory for dice specifications.*

Package Information



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.31
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
X	SEE VARIATIONS			
Y	.071	.087	1.803	2.209
α	0°	8°	0°	8°

VARIATIONS:

	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	N	
D	.189	.196	4.80	4.98	16	AA
S	.0020	.0070	0.05	0.18		
X	.107	.123	2.72	3.12		
D	.337	.344	8.56	8.74	20	AB
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AC
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AD
S	.0250	.0300	0.635	0.762		
X	.271	.287	6.88	7.29		

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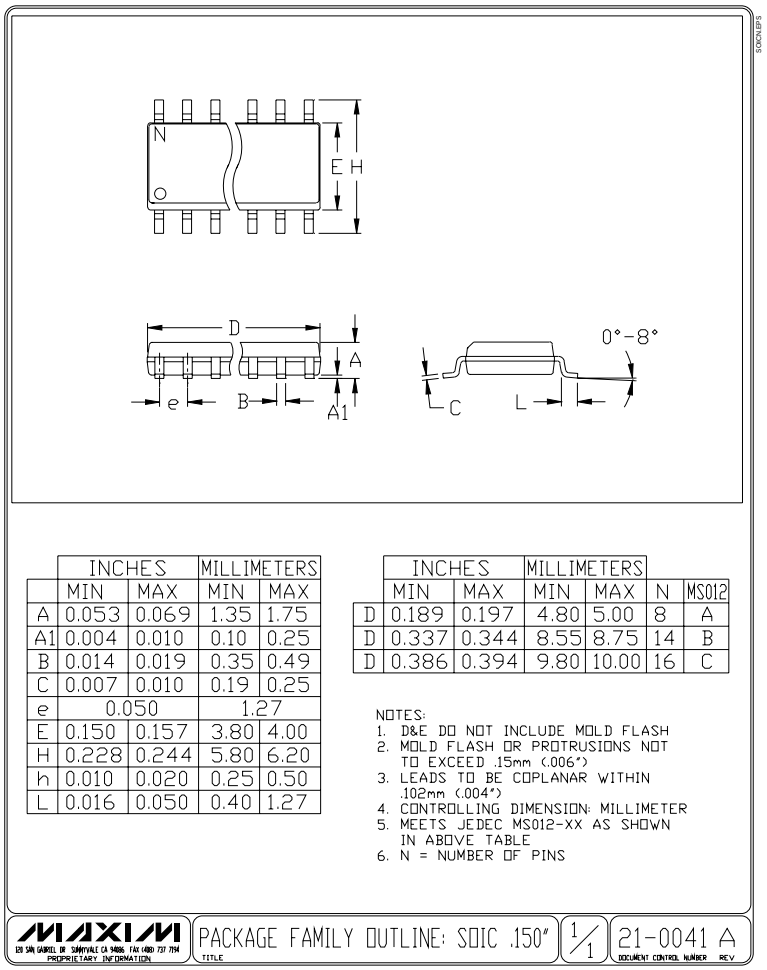
Package Information (continued)



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050		1.27	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	A
D	0.337	0.344	8.55	8.75	14	B
D	0.386	0.394	9.80	10.00	16	C

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MS012-XX AS SHOWN IN ABOVE TABLE
6. N = NUMBER OF PINS

MAXIM — PACKAGE FAMILY OUTLINE: SOIC .150" — 1/1 — 21-0041 A

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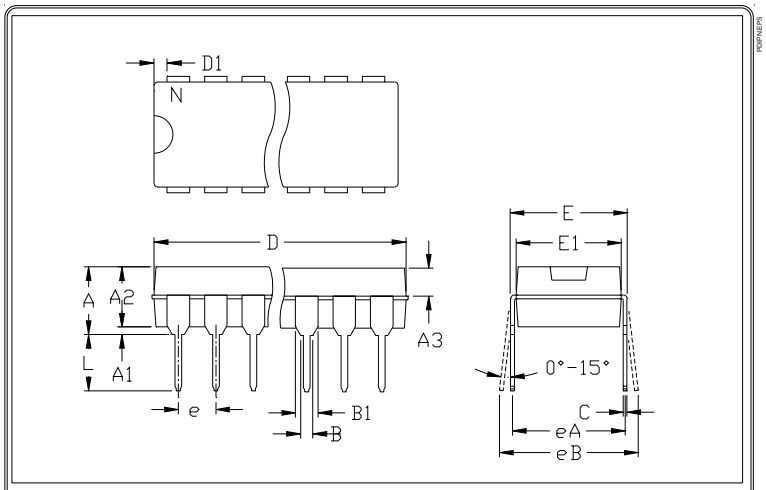
Package Information (continued)



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.200	---	5.08
A1	0.015	---	0.38	---
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100	---	2.54	---
eA	0.300	---	7.62	---
eB	---	0.400	---	10.16
L	0.115	0.150	2.92	3.81

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS001
D	0.348	0.390	8.84	9.91	8	AB
D	0.735	0.765	18.67	19.43	14	AC
D	0.745	0.765	18.92	19.43	16	AA
D	0.885	0.915	22.48	23.24	18	AD
D	1.015	1.045	25.78	26.54	20	AE
D	1.14	1.265	28.96	32.13	24	AF
D	1.360	1.380	34.54	35.05	28	*5

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS001-XX AS SHOWN IN ABOVE TABLE
5. SIMILIAR TO JEDEC MO-058AB
6. N = NUMBER OF PINS

MAXIM 120 SAN GABRIEL DR SUNNYVALE CA 94086 FAX (408) 737 7194 PROPRIETARY INFORMATION | TITLE: PACKAGE FAMILY OUTLINE: PDIP .300" | 1/1 | DOCUMENT CONTROL NUMBER: 21-0043 A REV.

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