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BTA425Y-800BT

3Q Hi-Com Triac

23 June 2014

Product data sheet

1. General description

Planar passivated high commutation three quadrant triac in a SOT78D (TO-220AB) internally insulated plastic package intended for use in circuits where high static and dynamic dV/dt and high dI/dt can occur. This "series BT" triac will commute the full RMS current at the maximum rated junction temperature ($T_{j(max)} = 150\text{ }^{\circ}\text{C}$) without the aid of a snubber. It is used in applications where "high junction operating temperature capability" is required.

2. Features and benefits

- 3Q technology for improved noise immunity
- 2500 V RMS isolation voltage capability
- High commutation capability with maximum false trigger immunity
- High immunity to false turn-on by dV/dt
- High junction operating temperature capability
- High voltage capability
- High current capability
- Least sensitive gate for highest noise immunity
- Internally insulated package
- Internally isolated mounting base
- Planar passivated for voltage ruggedness and reliability
- Triggering in three quadrants only

3. Applications

- Applications subject to high temperature
- Heating controls
- High power motor control
- High power switching

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	-	800	V
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25\text{ }^{\circ}\text{C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5	-	-	250	A
T_j	junction temperature		-	-	150	$^{\circ}\text{C}$



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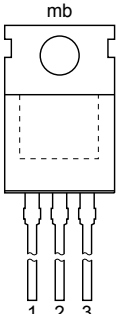

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 101\text{ }^{\circ}\text{C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	-	25	A
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 7	-	-	50	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 7	-	-	50	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 7	-	-	50	mA
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 536\text{ V}$; $T_j = 150\text{ }^{\circ}\text{C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit	2000	-	-	V/ μs
dI_{com}/dt	rate of change of commutating current	$V_D = 400\text{ V}$; $T_j = 150\text{ }^{\circ}\text{C}$; $I_{T(RMS)} = 25\text{ A}$; $dV_{com}/dt = 20\text{ V}/\mu\text{s}$; (snubberless condition); gate open circuit	15	-	-	A/ms

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T1	main terminal 1	 <p>TO-220AB (SOT78D)</p>	 <p>sym051</p>
2	T2	main terminal 2		
3	G	gate		
mb	n.c.	mounting base; isolated		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BTA425Y-800BT	TO-220AB	plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220	SOT78D

7. Marking

Table 4. Marking codes

Type number	Marking code
BTA425Y-800BT	BTA425Y-800BT

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	800	V
$I_{\text{T(RMS)}}$	RMS on-state current	full sine wave; $T_{\text{mb}} \leq 101\text{ °C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	25	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{\text{j(init)}} = 25\text{ °C}$; $t_{\text{p}} = 20\text{ ms}$; Fig. 4 ; Fig. 5	-	250	A
		full sine wave; $T_{\text{j(init)}} = 25\text{ °C}$; $t_{\text{p}} = 16.7\text{ ms}$	-	275	A
I^2t	I^2t for fusing	$t_{\text{p}} = 10\text{ ms}$; sine-wave pulse	-	312.5	A^2s
di_{T}/dt	rate of rise of on-state current	$I_{\text{T}} = 30\text{ A}$; $I_{\text{G}} = 0.2\text{ A}$; $di_{\text{G}}/dt = 0.2\text{ A}/\mu\text{s}$	-	100	$\text{A}/\mu\text{s}$
I_{GM}	peak gate current		-	2	A
P_{GM}	peak gate power		-	5	W
$P_{\text{G(AV)}}$	average gate power	over any 20 ms period	-	0.5	W
T_{stg}	storage temperature		-40	150	$^{\circ}\text{C}$
T_{j}	junction temperature		-	150	$^{\circ}\text{C}$

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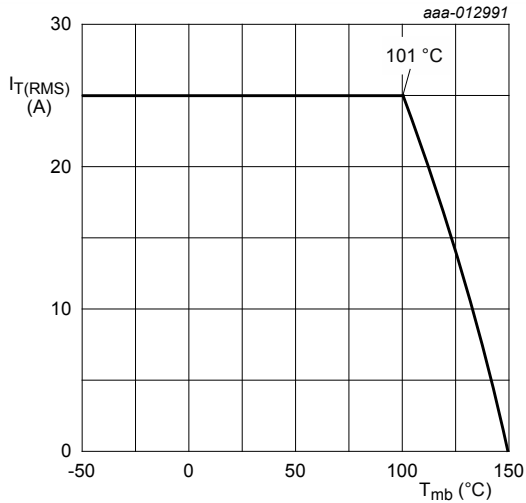
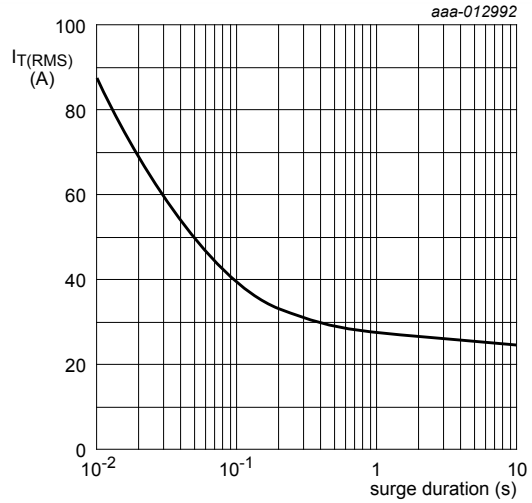
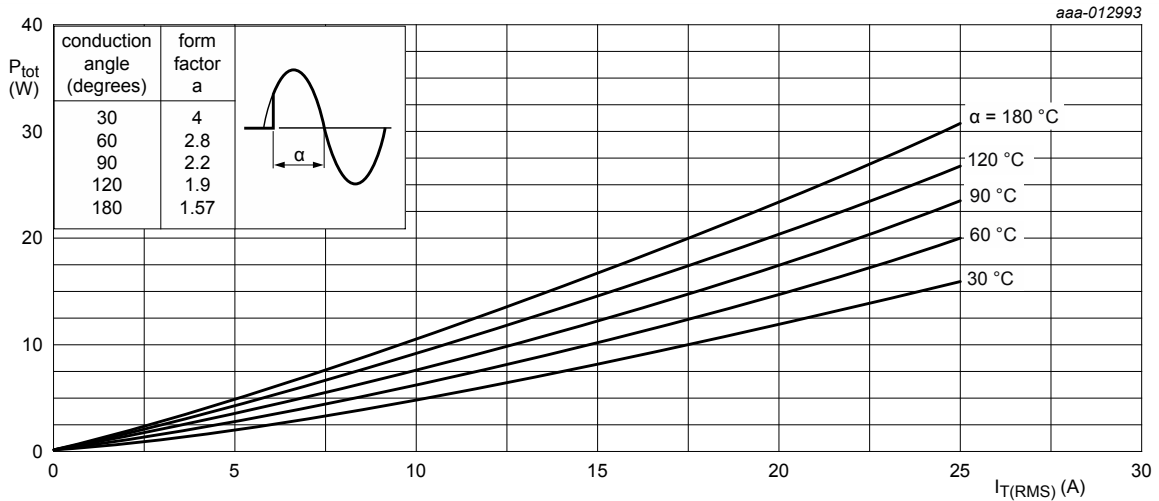


Fig. 1. RMS on-state current as a function of mounting base temperature; maximum values



f = 50 Hz; T_{mb} = 101 °C

Fig. 2. RMS on-state current as a function of surge duration; maximum values



α = conduction angle
 a = form factor = $I_{T(RMS)} / I_{T(AV)}$

Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

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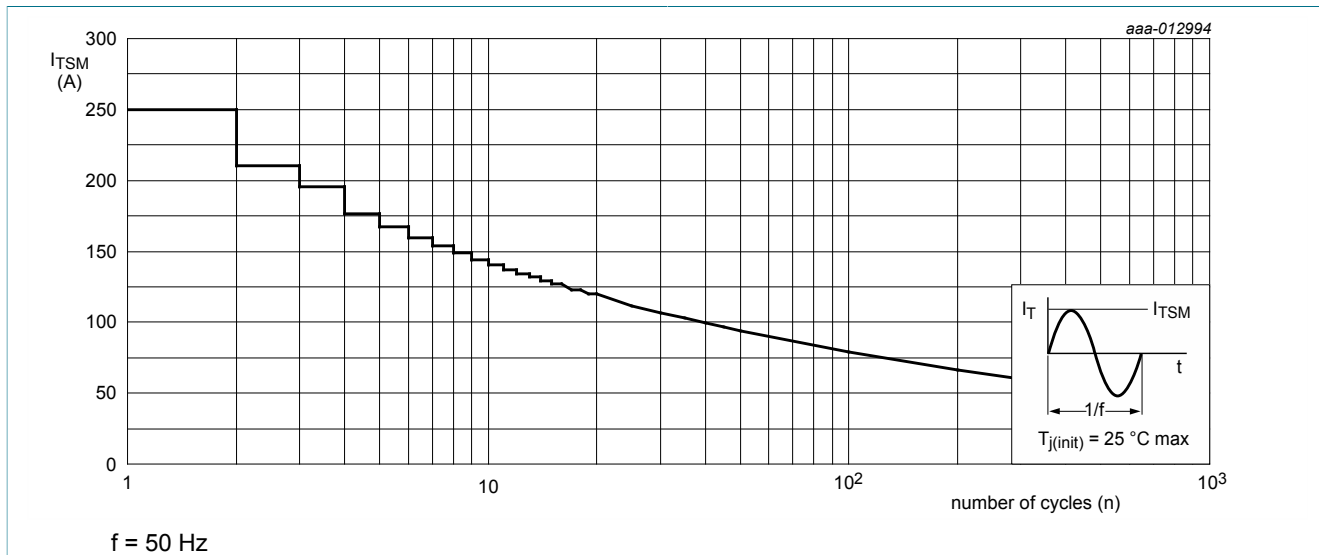


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

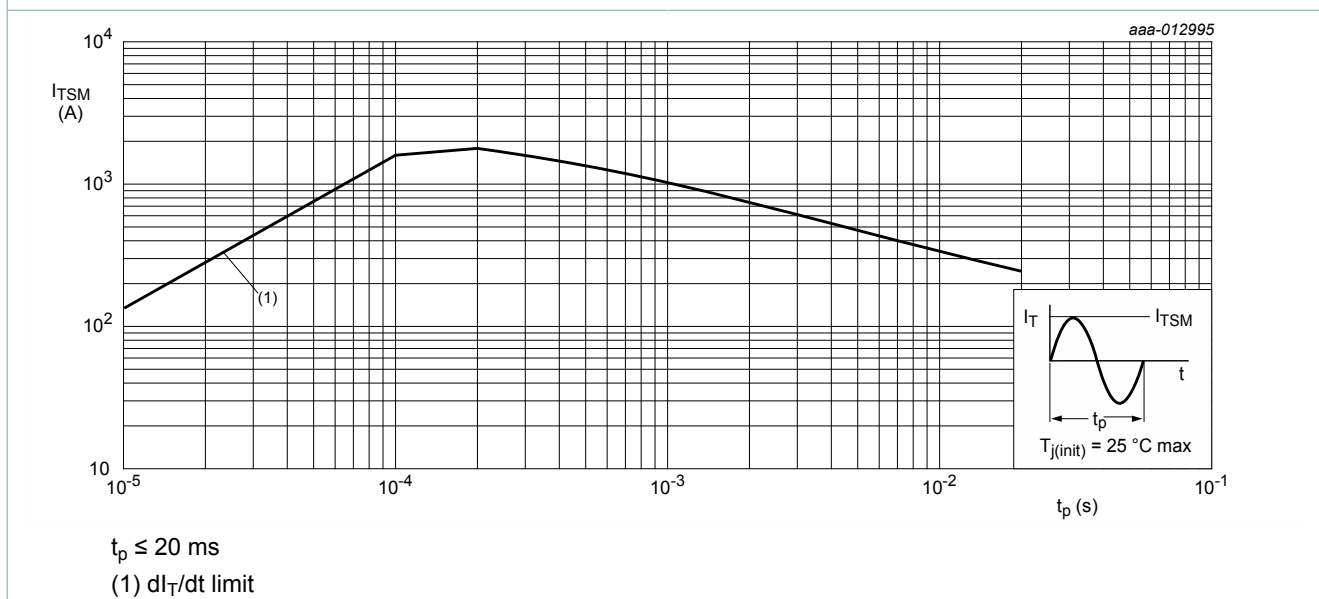


Fig. 5. Non-repetitive peak on-state current as a function of pulse duration; maximum values

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	full cycle; Fig. 6	-	-	1.7	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	-	60	-	K/W

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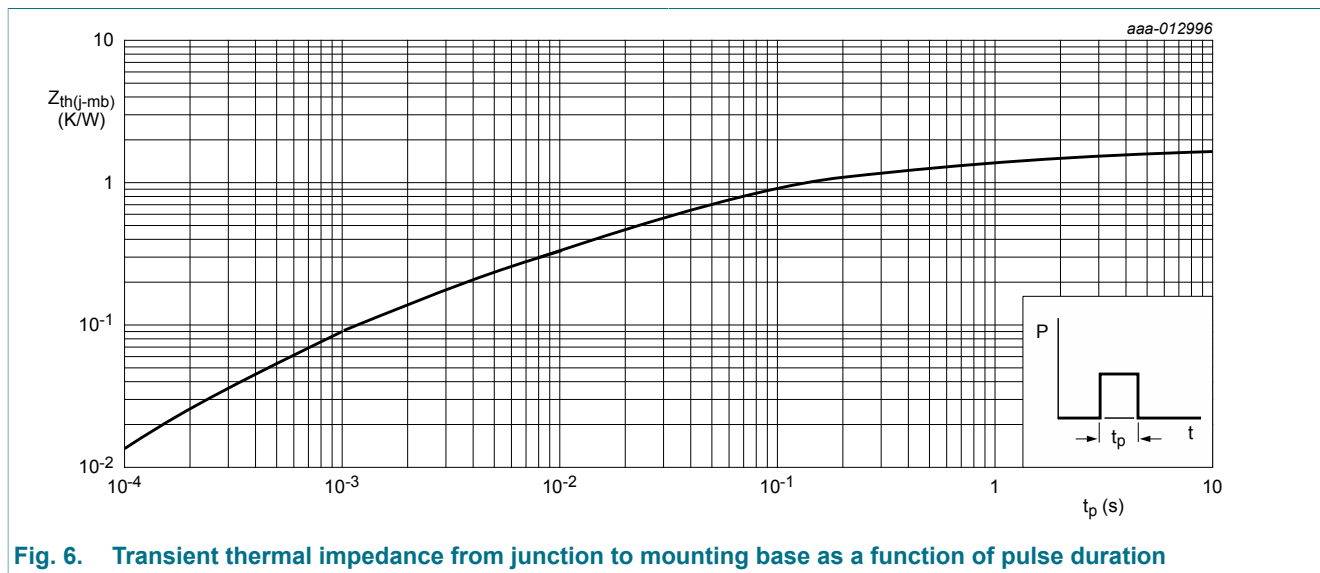


Fig. 6. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Isolation characteristics

Table 7. Isolation characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{isol(RMS)}$	RMS isolation voltage	from all terminals to external heatsink; sinusoidal waveform; clean and dust free; $50\text{ Hz} \leq f \leq 60\text{ Hz}$; $RH \leq 65\%$; $T_{mb} = 25\text{ }^\circ\text{C}$	-	-	2500	V
C_{isol}	isolation capacitance	from main terminal 2 to external heatsink; $f = 1\text{ MHz}$; $T_{mb} = 25\text{ }^\circ\text{C}$	-	10	-	pF

11. Characteristics

Table 8. Characteristics

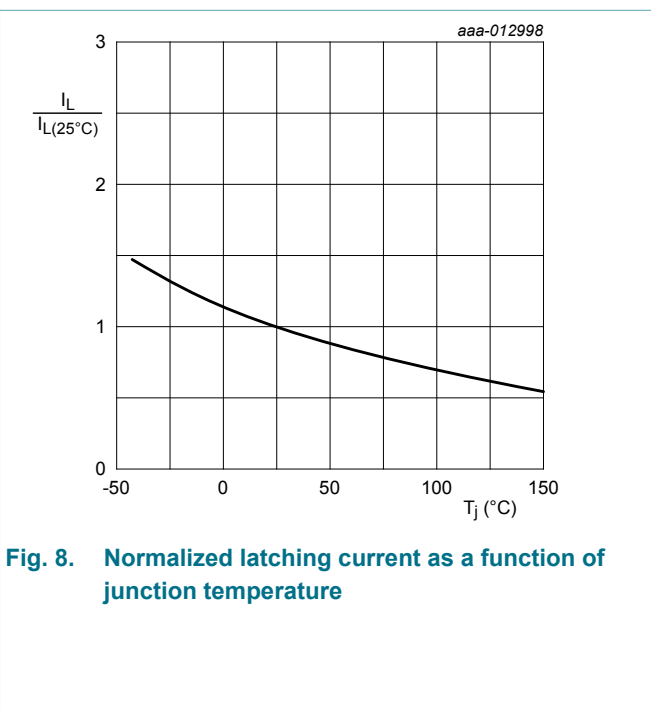
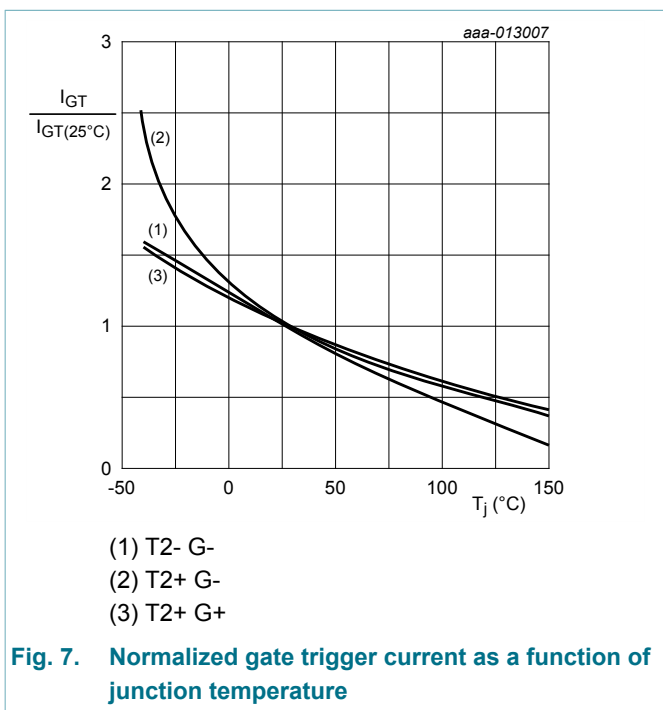
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ }^\circ\text{C}$; Fig. 7	-	-	50	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 7	-	-	50	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 7	-	-	50	mA
I_L	latching current	$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ }^\circ\text{C}$; Fig. 8	-	-	80	mA
		$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 8	-	-	100	mA

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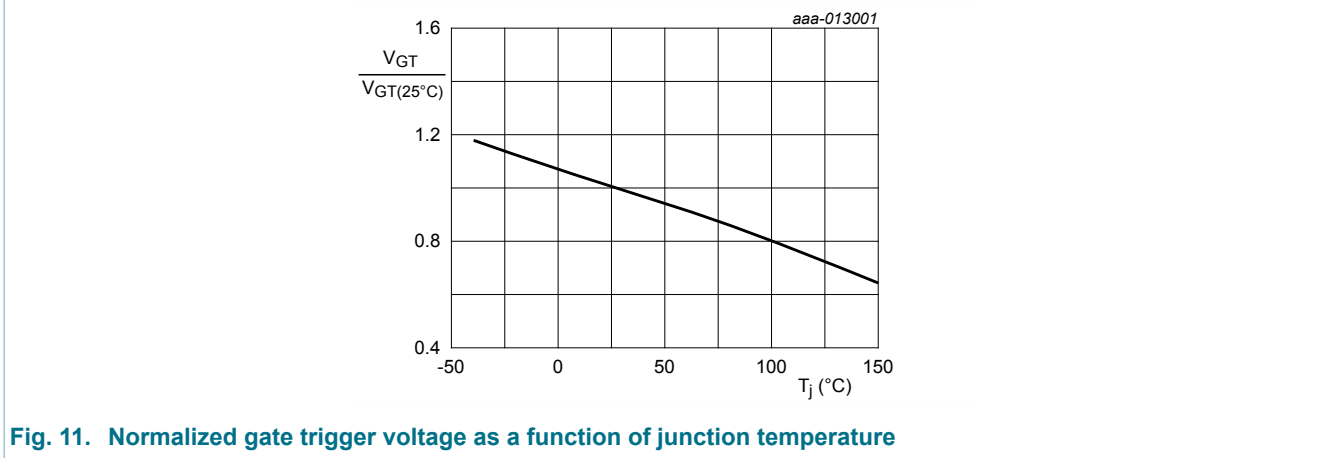
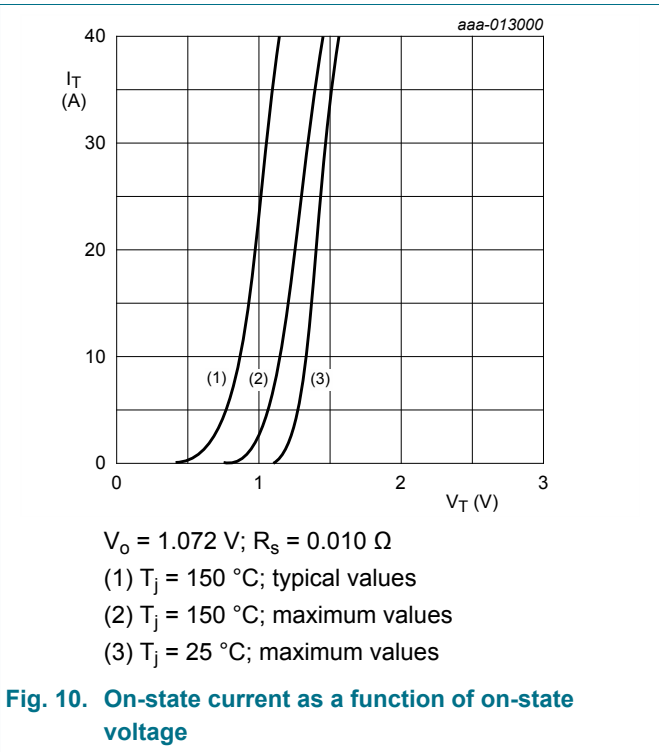
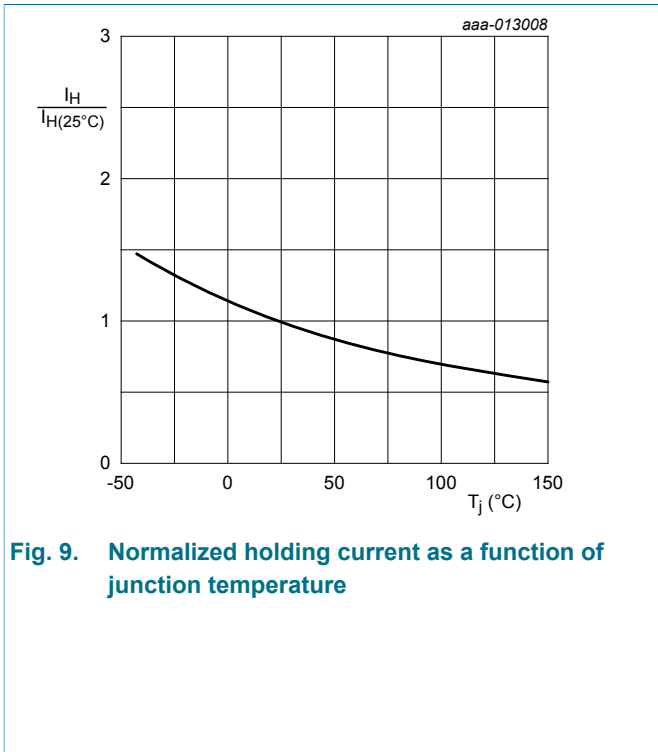
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		$V_D = 12\text{ V}; I_G = 0.1\text{ A}; T_2\text{- G-}; T_j = 25\text{ }^\circ\text{C};$ Fig. 8	-	-	80	mA
I_H	holding current	$V_D = 12\text{ V}; T_j = 25\text{ }^\circ\text{C};$ Fig. 9	-	-	75	mA
V_T	on-state voltage	$I_T = 35\text{ A}; T_j = 25\text{ }^\circ\text{C};$ Fig. 10	-	1.2	1.5	V
V_{GT}	gate trigger voltage	$V_D = 12\text{ V}; T_j = 25\text{ }^\circ\text{C};$ Fig. 11	-	0.9	1.3	V
		$V_D = 400\text{ V}; T_j = 150\text{ }^\circ\text{C};$ Fig. 11	0.2	0.45	-	V
I_D	off-state current	$V_D = 800\text{ V}; T_j = 150\text{ }^\circ\text{C}$	-	0.4	2	mA
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 536\text{ V}; T_j = 150\text{ }^\circ\text{C}; (V_{DM} = 67\% \text{ of } V_{DRM});$ exponential waveform; gate open circuit	2000	-	-	V/ μ s
dI_{com}/dt	rate of change of commutating current	$V_D = 400\text{ V}; T_j = 150\text{ }^\circ\text{C}; I_{T(RMS)} = 25\text{ A};$ $dV_{com}/dt = 20\text{ V}/\mu\text{s};$ (snubberless condition); gate open circuit	15	-	-	A/ms



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12. Package outline

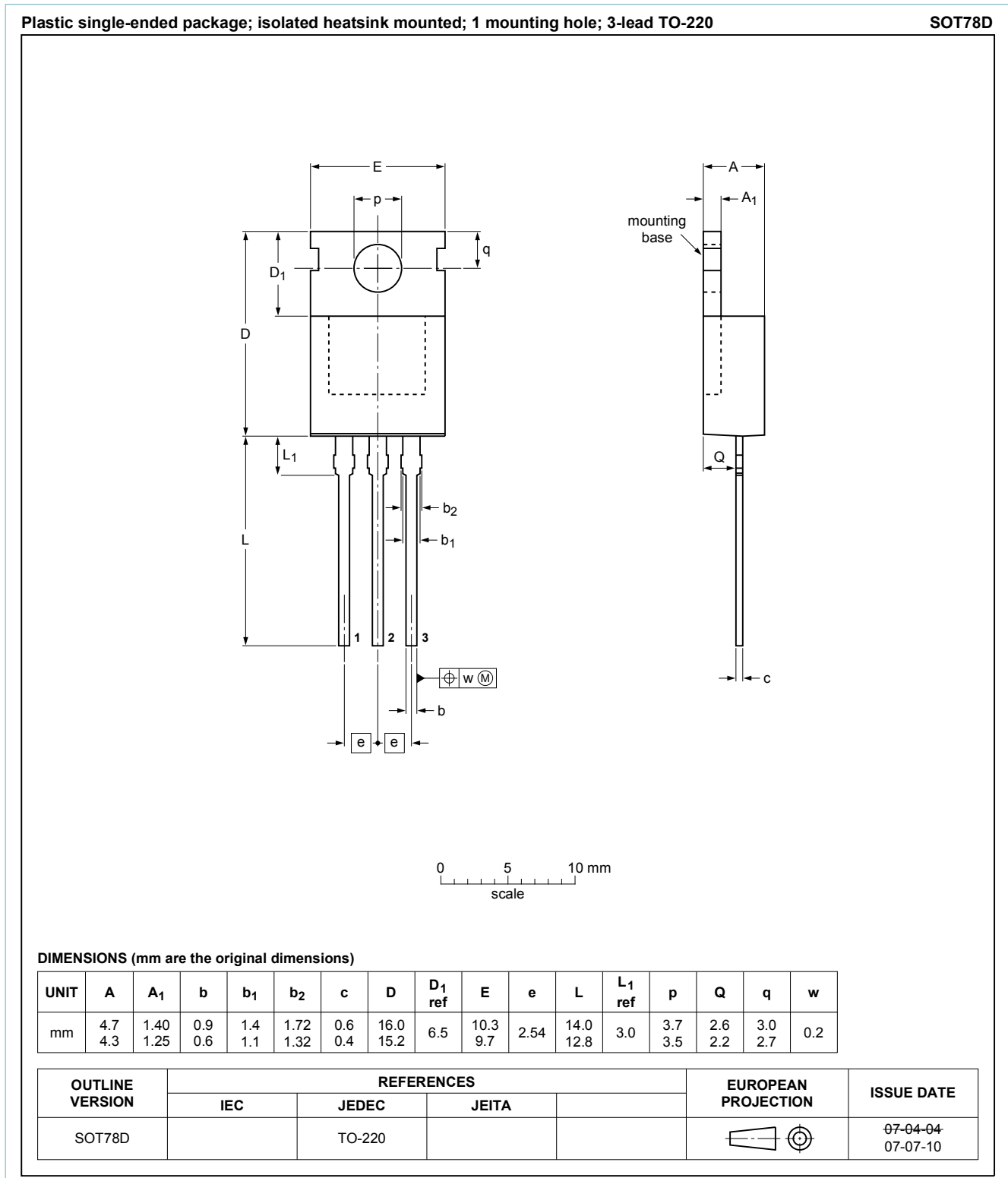


Fig. 12. Package outline TO-220AB (SOT78D)

13. Legal information

13.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
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