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A6861KLPTR-T

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Automotive 3-Phase Isolator MOSFET Driver

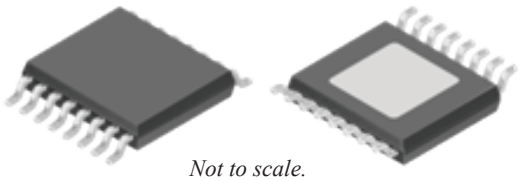
FEATURES AND BENEFITS

- 3 floating N-channel MOSFET drives
- Maintains VGS with 100 kΩ gate-source resistors
- Integrated charge pump controller
- 4.5 V-50 V Supply voltage operating range
- Independent TTL input for each phase
- 150°C ambient (165°C junction) continuous
- A^2-SIL™ Product – device features for safety critical systems

APPLICATIONS

- 3-phase safety disconnect systems
- Electric power steering (EPS)
- Electric braking
- 3-phase Solid State Relay driver

Package: 16-Lead TSSOP with exposed thermal pad (suffix LP)



Not to scale.

DESCRIPTION

The A6861 is an N-channel power MOSFET driver capable of controlling MOSFETs connected as a 3-phase solid state relay in phase-isolation applications. The A6861 is intended for automotive systems that must meet ASIL requirements. In safety critical applications motor isolation is a critical safety requirement which is currently addressed with discrete circuitry or relays. Allegro A^2-SIL™ products include specific features that compliment proper system design, allowing users to achieve up to ASIL-D system rating.

The A6861 has three independent floating gate drive outputs to maintain the power MOSFETs in the on state over the full supply range with high phase-voltage slew rates. An integrated charge pump regulator provides the above battery supply voltage necessary to maintain the power MOSFETs in the on state continuously when the phase voltage is equal to the battery voltage. The charge pump will maintain sufficient gate drive (>7.5 V) for battery voltages down to 4.5 V with 100 kΩ gate-source resistors.

The three gate drives can be independently controlled by a logic level control input. In typical applications the MOSFETs will be switched on within 8 µs and will switch off within 1 µs.

An undervoltage monitor checks that the pumped supply voltage is high enough to ensure that the MOSFETs are maintained in a safe conducting state.

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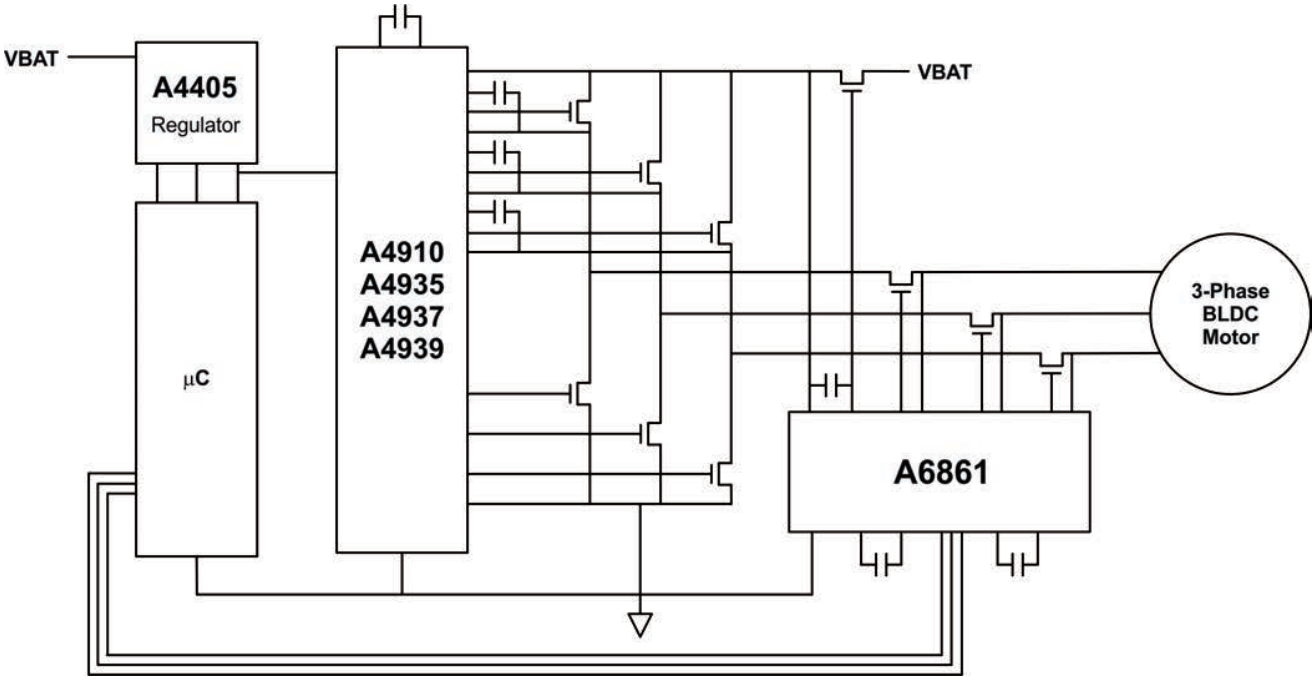


Typical Application Diagram

Description (continued)

The A6861 is supplied in a 16-lead TSSOP (LP), with exposed pad for enhanced thermal dissipation. They are lead (Pb) free, with 100% matte tin leadframe plating.

Selection Guide

Part Number	Packing	Package
A6861KLPTR-T	13-in. reel, 4000 pieces/reel	16-Lead TSSOPwith exposed thermal pad, 4.4 X 5 mm case

SPECIFICATIONS

Absolute Maximum Ratings[1]

Characteristic	Symbol	Notes	Rating	Units
Load Voltage Supply	V_{BB}		–0.3 to 50	V
Terminal VCP	V_{CP}		V_{BB} – 0.3 to V_{BB} + 12	V
Terminal CP1	V_{CP1}		V_{BB} – 12 to V_{BB} + 0.3	V
Terminal CP2	V_{CP2}		V_{BB} – 0.3 to V_{CP4} + 0.3	V
Terminal CP3	V_{CP3}		V_{BB} – 12 to V_{BB} + 0.3	V
Terminal CP4	V_{CP4}		V_{CP2} – 0.3 to V_{CP} + 0.3	V
Terminal ENU, ENV, ENW	V_I		–0.3 to 50	V
Terminal GU, GV, GW	V_{GX}		V_{SX} – 0.3 to V_{SX} + 12	V
Terminal SU, SV, SW	V_{SX}		– 6 to V_{BB} + 5	V
Operating Ambient Temperature	T_A	Limited by power dissipation	–40 to 150	ºC
Maximum ContinuousJunction Temperature	$T_{J(max)}$		165	ºC
Transient Junction Temperature	T_{Jt}	Over temperature event not exceeding 10s, lifetime duration not exceeding 10hours, guaranteed by design characterization.	175	ºC
Storage Temperature	T_{stg}		–55 to 150	ºC

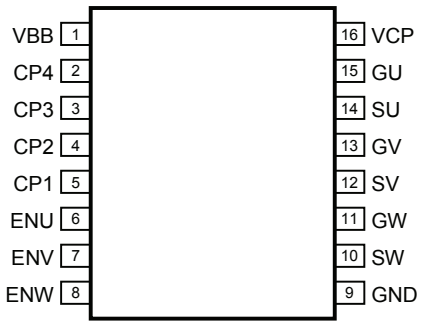
[1]With respect to GND. Ratings apply when no other circuit operating constraints are present.

THERMAL CHARACTERISTICS may require derating at maximum conditions, see application information

Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance (Junction to Ambient)	$R_{\theta JA}$	4-layer PCB based on JEDEC standard	34	ºC/W
		1-layer PCB with copper limited to solder pads	43	ºC/W
Package Thermal Resistance (Junction to Pad)	$R_{\theta JP}$		2	ºC/W

*Additional thermal data available on the Allegro Web site.

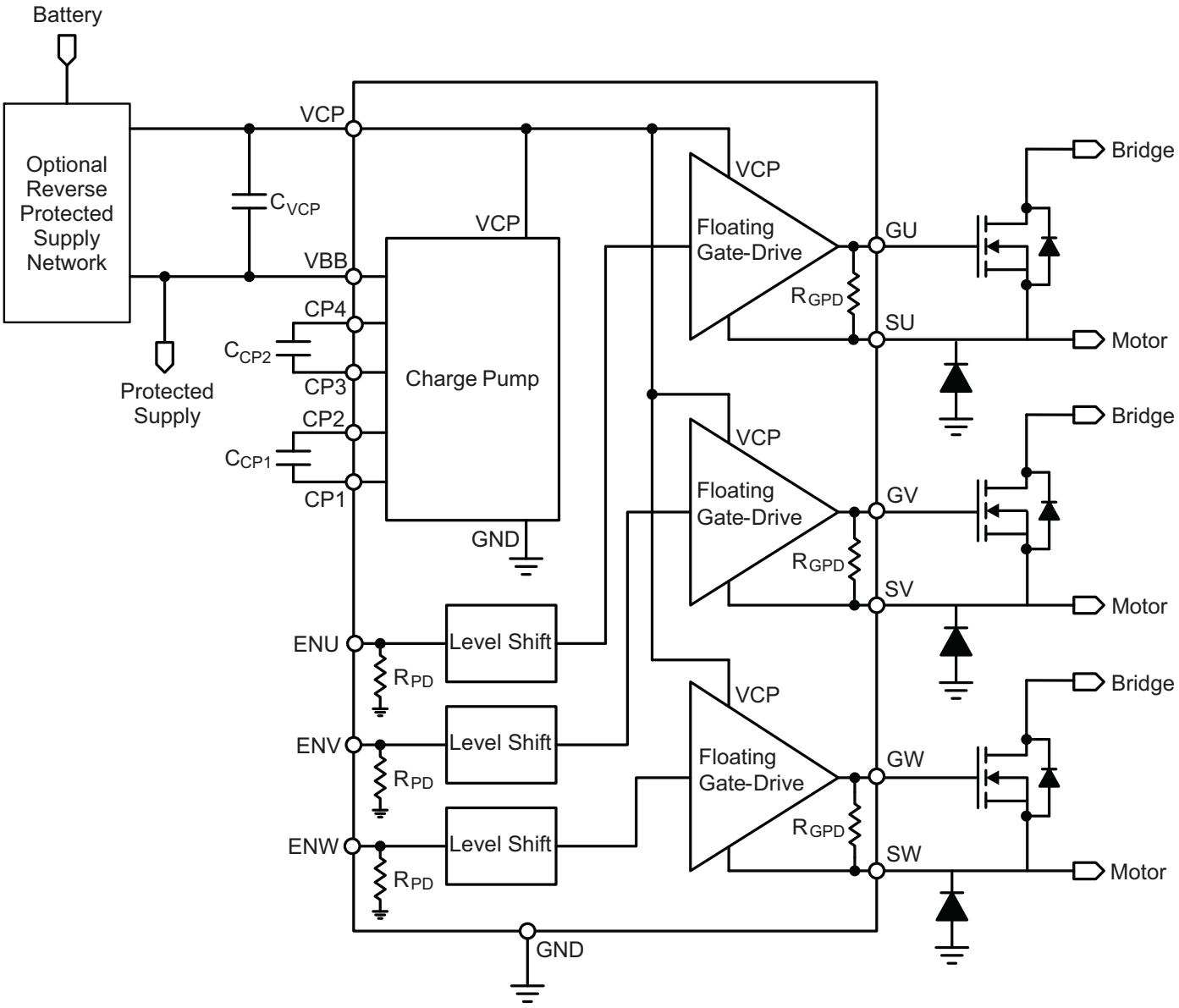
Pin-out Diagram and Terminal List Table



Package LP, 16-Pin TSSOP Pin-out Diagram

Terminal List Table

Name	Number	Description
VBB	1	Main Power Supply
CP4	2	Pump Capacitor Connection
CP3	3	Pump Capacitor Connection
CP2	4	Pump Capacitor Connection
CP1	5	Pump Capacitor Connection
ENU	6	U phase Enable Input
ENV	7	V phase Enable Input
ENW	8	W phase Enable Input
GND	9	Ground
SW	10	W Phase MOSFET Source Reference
GW	11	W Phase MOSFET Gate Drive
SV	12	V Phase MOSFET Source Reference
GV	13	V Phase MOSFET Gate Drive
SU	14	U Phase MOSFET Source Reference
GU	15	U Phase MOSFET Gate Drive
VCP	16	Pump Supply
Tab		Exposed Tab - Connect to GND



Functional Block Diagram

ELECTRICAL CHARACTERISTICS at T_J = -40 to +150°C, V_{BB} 6 V to 50 V (unless noted otherwise)

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Supply						
VBB Functional Operating Range[1]	V_{BB}	Operating. Outputs active.	4.5	–	50	V
		Operating. Outputs disabled	4	–	50	V
		No unsafe states.	0	–	50	V
VBB Quiescent Current	I_{BBQ}	Gate drive active, V_{BB} = 12 V, Sx = GND.	–	10	13.5	mA
	I_{BBS}	Gate drive disabled, V_{BB} = 12 V	–	5.5	8	mA
VCP Output voltage w.r.t. V_{BB}	V_{CP}	V_{BB} > 9V, I_{VCP} > -1 mA[2]	9	10	11	V
		6 V < V_{BB} ≤ 9 V, I_{VCP} > -1 mA[2]	8	10	11	V
		4.5 V < V_{BB} ≤ 6 V, I_{VCP} > - 800 µA[2]	7.5	9.5	–	V
VCP Static Load Resistance	R_{CP}	Between VCP and VBB (using ±1% tolerance resistor)	100	–	–	kΩ
Gate Output Drive						
Turn-on Time	t_r	C_{LOAD} = 10 nF, 20% to 80%	–	5	–	µs
Turn-off Time	t_r	C_{LOAD} = 10 nF, 80% to 20%	–	0.5	–	µs
Propagation Delay – Turn On[3]	t_{PON}	C_{LOAD} = 10 nF, ENx high to Gx 20%	–	–	3	µs
Propagation Delay – Turn Off[3]	t_{POFF}	C_{LOAD} = 10 nF, ENx low to Gx 80%	–	–	1.5	µs
Turn-on Pulse Current	I_{GXP}		–	14	–	mA
Turn-on Pulse Time	t_{GXP}		–	12.5	–	µs
On Hold Current	I_{GXH}		–	400	–	µA
Pull-down On Resistance	$R_{DS(on)DN}$	T_J = 25°C, I_{Gx}= 10 mA	–	5	–	Ω
		T_J = 150°C, I_{Gx} = 10 mA	–	10	–	Ω
Gx Output high voltage w.r.t. SX, or VBB if SX>VBB	V_{GH}	V_{BB} > 9 V	8.5	10	12	V
		6 V < V_{BB} ≤ 9 V	8	10	12	V
		4.5 V < V_{BB} ≤ 6 V	7.5	9.5	–	V
Gate Drive Static Load Resistance	R_{GS}	Between Gx and Sx (using ±1% tolerance resistor)	100	–	–	kΩ
Gx Output Voltage Low	V_{GL}	-10 µA < I_{Gx} < 10 µA	–	–	V_{SX} +0.3	V
Gx Passive Pull-down	R_{GPD}	V_{Gx} - V_{Sx} < 0.3 V	–	950	–	kΩ
Logic Inputs & Outputs						
Input Low Voltage	V_{IL}		–	–	0.8	V
Input High Voltage	V_{IH}		2.0	–	–	V
Input Hysteresis	V_{Ihys}		150	300	–	mV
Input Pull-down Resistor	R_{PD}		30	50	70	kΩ
Diagnostics & Protection						
VCP Undervoltage Start-up Blank Timer	t_{CPON}		–	100	–	µs
VCP Undervoltage Lockout	V_{CPON}	V_{CP} w.r.t. V_{BB}. V_{CP} rising	6.2	6.7	7.2	V
	V_{CPOFF}	V_{CP} w.r.t. V_{BB}. V_{CP} falling	6.0	6.5	7.0	V

[1] Function is correct but parameters are not guaranteed below the general limits (6-50V).
[2] For input and output current specifications, negative current is defined as coming out of (sourcing) the specified device terminal.
[3] Refer to Figure 1.

FUNCTIONAL DESCRIPTION

The A6861 is an N-channel power MOSFET driver capable of controlling MOSFETs connected as a 3-phase solid state relay in phase-isolation applications. It has three independent floating gate drive outputs to maintain the power MOSFETs in the ON state over the full supply range when the phase outputs are PWM switched with high phase-voltage slew rates.

A charge pump regulator provides the above battery supply voltage necessary to maintain the power MOSFETs in the ON state continuously when the phase voltage is equal to the battery voltage. Voltage regulation is based on the difference between VBB and VCP.

The charge pump will maintain sufficient gate drive (>7.5 V) for battery voltages down to 4.5 V. It is also able to provide the current taken by gate-source resistors as low as 100 kΩ should they be required, between the source and gate of the power MOSFETS.

The voltage generated by the charge pump can also be used to power circuitry to control the gate-source voltage for a MOSFET connected to the main supply to provide reverse battery protection.

The three gate drives can be controlled independently by three logic level enable inputs. In typical applications the MOSFETs will be switched on within 8 µs and will switch off within 1 µs.

An undervoltage monitor checks that the pumped supply voltage is high enough to ensure that the MOSFETs are maintained in a safe conducting state

Input & Output Terminal Functions

VBB: Main power supply. The main power supply should be connected to VBB through a reverse voltage protection circuit.

GND: Main power supply return. Connect to supply ground.

VCP: Pumped gate drive voltage. Can be used to turn on a MOSFET connected to the main supply to provide reverse battery protection. Connect a 1 µF ceramic capacitor between VCP and VBB.

CP1, CP2: Pump capacitor connections. Connect a 330 nF ceramic capacitor between CP1 and CP2.

CP3, CP4: Pump capacitor connections. Connect a 330 nF ceramic capacitor between CP3 and CP4.

ENU, ENV, ENW: Logic level enable inputs to control the gate drive outputs.

GU, GV, GW: Floating, gate-drive outputs for external n-channel MOSFETs.

SU, SV, SW: Load phase connections. These terminals are the reference connections for the floating gate-drive outputs.

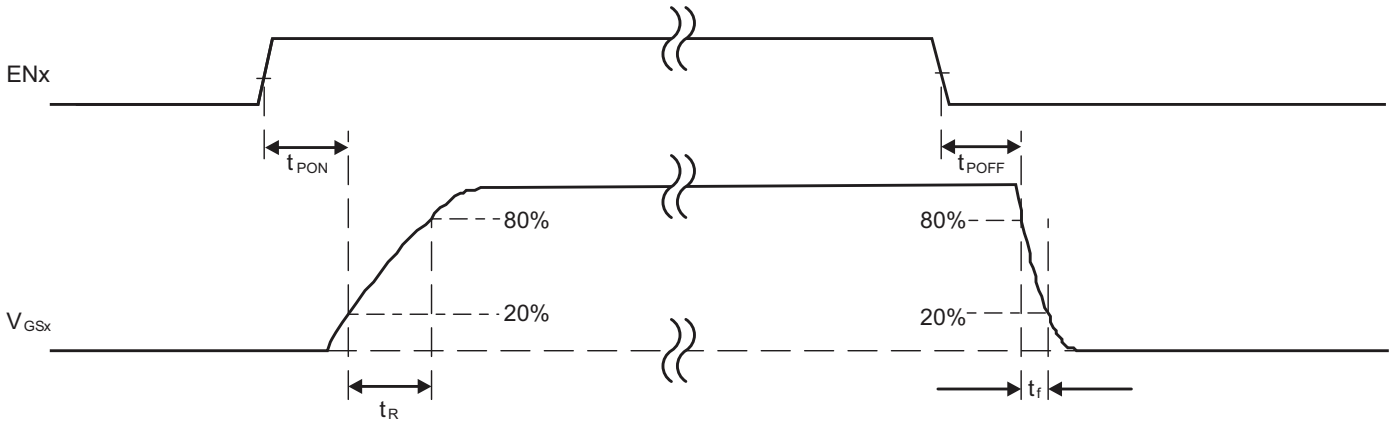


Figure 1: Enable Inputs to V_{GS} Timing

Power Supplies

A single reverse polarity protected power supply voltage is required. It is recommended that the VBB supply is decoupled to GND by ceramic capacitors mounted close to the device pins. Decoupling capacitors are not required for correct operation but will assist in reducing switching noise conducted to the supply from the charge pump switching circuits.

The A6861 will operate within specified parameters with V_{BB} from 6 V to 50 V and will function correctly with a supply down to 4.5 V. This provides a very rugged solution for use in the harsh automotive environment and permits use in start-stop systems.

There are no unsafe device states, even at low supply voltage. As the supply voltage rises from 0 V, the gate drive outputs are maintained in the off state until the gate voltage is sufficiently high to ensure conduction and the outputs are enabled.

Pump Regulator

The gate drivers are powered by a regulated charge pump, which provides the voltage above VBB to ensure that the MOSFETs are fully enhanced with low on-resistance when the source of the MOSFET is at the same voltage as V_{BB}.

Voltage regulation is based on the difference between the VBB and VCP pins.

The pumped voltage, V_{CP}, is available at the VCP terminal and is limited to 12 V maximum with respect to V_{BB}. This removes the need for external clamp diodes on the power MOSFETs to limit the gate source voltage.

It also allows the VCP terminal to be used to power circuitry to control a MOSFET connected to the main supply to provide reverse battery protection.

To provide the continuous low level current required when gate-source resistors are connected to the external MOSFETs, a pump storage capacitor, typically 1 µF, has to be connected between the VCP and VBB terminals. Pump capacitors, typically 330 nF, have to be connected between the CP1 and CP2 terminals and between the CP3 and CP4 terminals to provide sufficient charge transfer, especially at low supply voltage.

Gate Drives

The A6861 is designed to drive external, low on-resistance, power N-channel MOSFETs when used in a phase isolation application. The gate drive outputs and the V_{CP} supply will turn the MOSFETs on in typically 8 µs and will maintain the on-state during transients on the source of the MOSFETs. The gate drive outputs will turn the MOSFETs off in typically 1 µs and will hold them in the off-state during transients on the source. An internal resistor, R_{GPD}, between the Gx and Sx pins plus an integrated hold-off circuit, will ensure that the gate-source voltage of the MOSFET is held close to 0 V even with the power disconnected. This can remove the need for additional gate-source resistors on the isolation MOSFETs. In any case, if gate-source resistors are mandatory for the application then the pump regulator can provide sufficient current to maintain the MOSFET in the on state with a gate-source resistor of as low as 100 kΩ.

The floating gate-drive outputs for external N-channel MOSFETs are provided on pins GU, GV, and GW. Gx=1 (or “high”) means that the upper half of the driver is turned on and current will be sourced to the gate of the MOSFET in the phase isolation circuit, turning it on. Gx=0 (or “low”) means that the lower half of the driver is turned on and will sink current from the external MOSFET’s gate to the respective Sx terminal, turning it off.

The reference points for the floating drives are the load phase connections, SU, SV, and SW. The discharge current from the floating MOSFET gate capacitance flows through these connections.

In some applications it may be necessary to provide a current recirculation path when the motor load is isolated. This will be necessary in situations where the motor driver does not reduce the load current to zero before the isolation MOSFETs are turned off.

The recirculation path can be provided by connecting a suitably rated power diode to the “motor” side of the isolation MOSFETs and GND. See the Functional Block Diagram for more details. Only three diodes are required since the source to drain diodes in the isolation and bridge MOSFETs provide a recirculation path to the Battery connection.

Logic Control Inputs

Three TTL level digital inputs, ENU, ENV, & ENW, provide independent control for each gate drive. The three enable inputs directly control their respective gate drive outputs. When an enable input is high the corresponding gate drive output will be on.

These inputs have nominal hysteresis of 300 mV to improve noise performance and can be shorted to V_{BB} without damage.

Supply Monitor

The A6861 includes undervoltage detection on the charge pump output. If the voltage at the charge pump output, V_{CP}, drops below the falling undervoltage threshold, V_{CPOFF}, then the gate drive outputs will be held in the off state. They will remain in that state until V_{CP} rises above the rising undervoltage threshold V_{CPON}.

Input and Output Structures

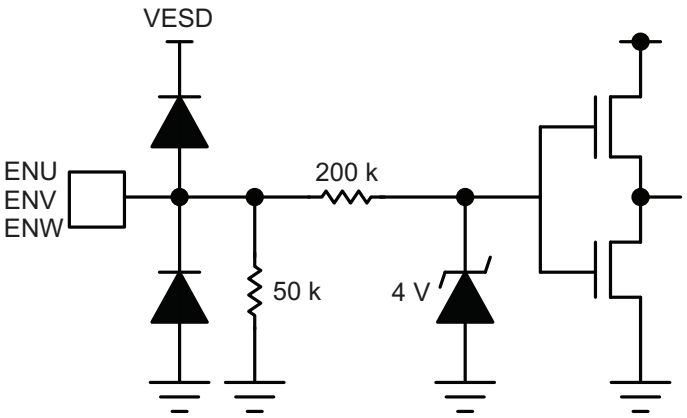


Figure 2: ENU, ENV, ENW Inputs

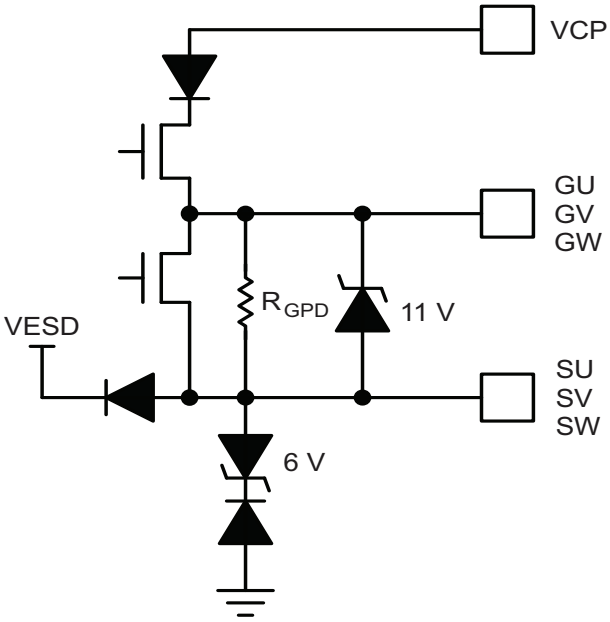


Figure 3: Drive Outputs

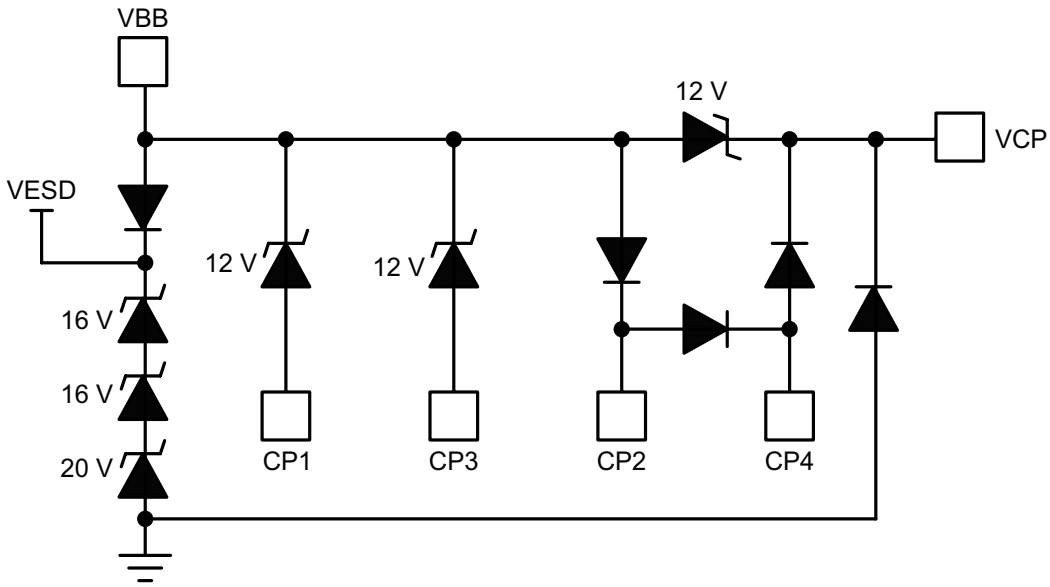


Figure 4: Supplies

Battery Voltage Reversal Protection

The charge pump output voltage may be used to drive a reverse-connected battery protection circuit as illustrated in Figure 5.

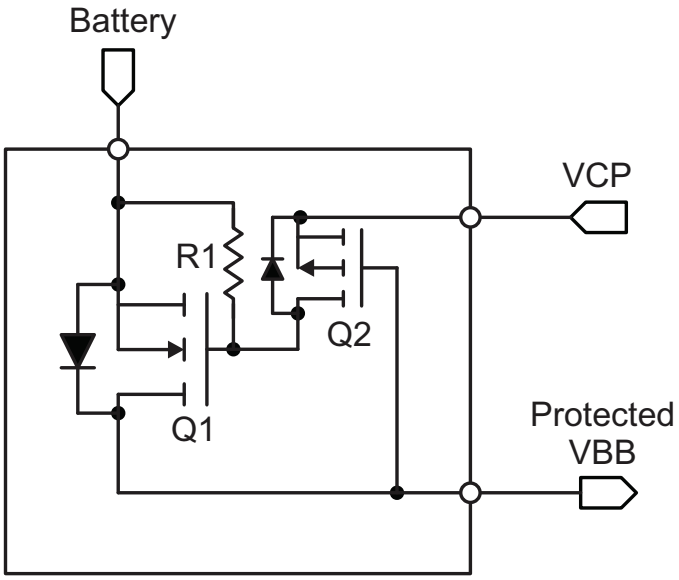


Figure 5: Indicative Reverse Voltage Protection Scheme

Transistor Q1 is an n-channel power MOSFET selected to create a low voltage drop at the full current rated for the motor drive system. It is connected with source and drain pins reversed from the normal biased condition. During power up the initial system current is supplied to VBB through the forward biased parasitic source to drain diode until V_{CP} has exceeded the threshold voltage of Q1 and turned it on.

When the battery voltage is reversed the voltage between VBB and VCP is zero, the gate source voltage on Q1 is zero and its source to drain diode becomes reverse biased. In this condition Q1 blocks current flow to VBB and the voltage between VBB and GND remains at Zero.

Transistor Q2 is a normally connected p channel, small signal MOSFET used to control the gate of Q1 in the normal and reversed battery voltage condition. Both Q1 and Q2 must be correctly rated for the full peak reversed battery voltage.

Resistor R1 is used to control the gate to source voltage of Q1 and is powered from the V_{CP} supply. To reduce the current drain from VCP the value of R1 should be a minimum defined for R_{CP}, 100 k.

PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference MO-153 ABT)
Dimensions in millimeters. NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

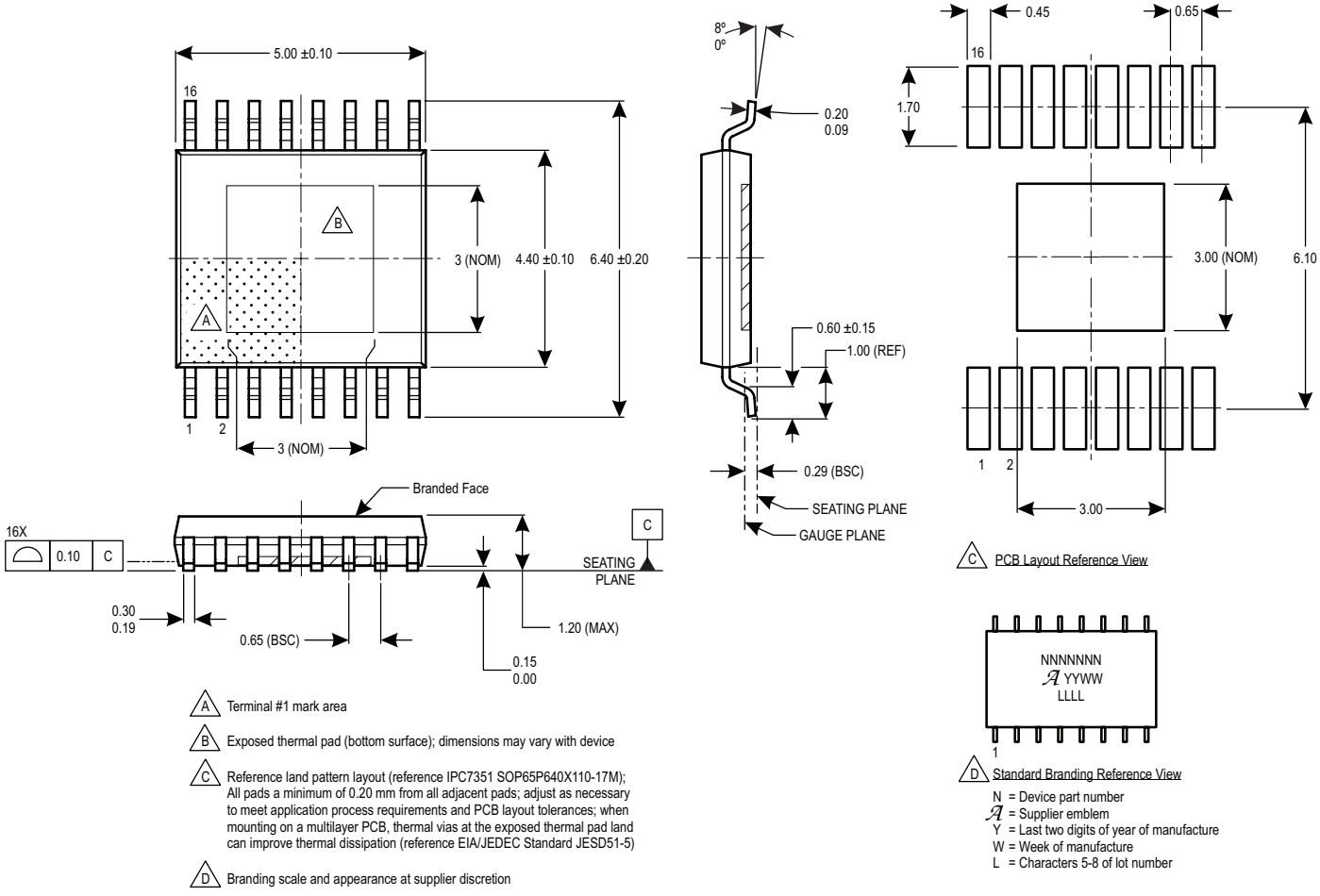


Figure 6: LP Package, 16-Lead TSSOP with Exposed Pad

Revision	Date	Change
–	February 26, 2014	Initial Release
1	August 25, 2014	Various text edits throughout; reformatted document
2	May 28, 2015	Corrected typo on Package Outline Drawing
3	July 20, 2016	Updated test conditions for R_{CP} and R_{GS} (page 5)