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# Automotive 3-Phase Isolator MOSFET Driver

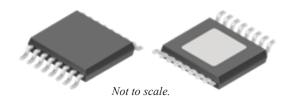
#### **FEATURES AND BENEFITS**

- 3 floating N-channel MOSFET drives
- Maintains VGS with 100 k $\Omega$  gate-source resistors
- Integrated charge pump controller
- 4.5 V-50 V Supply voltage operating range
- Independent TTL input for each phase
- 150°C ambient (165°C junction) continuous
- A<sup>2</sup>-SIL<sup>TM</sup> Product device features for safety critical systems

#### **APPLICATIONS**

- 3-phase safety disconnect systems
- Electric power steering (EPS)
- Electric braking
- 3-phase Solid State Relay driver

# Package: 16-Lead TSSOP with exposed thermal pad (suffix LP)



#### **DESCRIPTION**

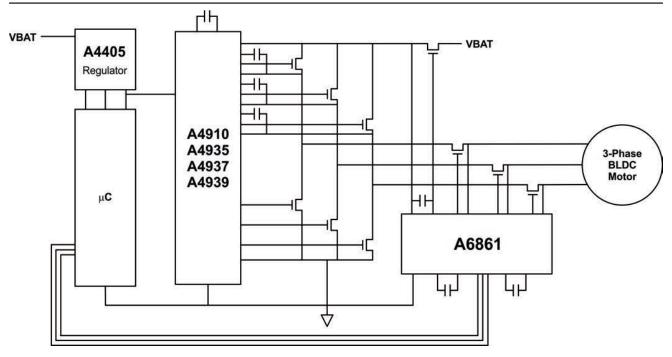
The A6861 is an N-channel power MOSFET driver capable of controlling MOSFETs connected as a 3-phase solid state relay in phase-isolation applications. The A6861 is intended for automotive systems that must meet ASIL requirements. In safety critical applications motor isolation is a critical safety requirement which is currently addressed with discrete circuitry or relays. Allegro A<sup>2-</sup>SIL<sup>TM</sup> products include specific features that compliment proper system design, allowing users to achieve up to ASIL-D system rating.

The A6861 has three independent floating gate drive outputs to maintain the power MOSFETs in the on state over the full supply range with high phase-voltage slew rates. An integrated charge pump regulator provides the above battery supply voltage necessary to maintain the power MOSFETs in the on state continuously when the phase voltage is equal to the battery voltage. The charge pump will maintain sufficient gate drive (>7.5 V) for battery voltages down to 4.5 V with  $100 \, \mathrm{k}\Omega$  gate-source resistors.

The three gate drives can be independently controlled by a logic level control input. In typical applications the MOSFETs will be switched on within 8  $\mu$ s and will switch off within 1  $\mu$ s.

An undervoltage monitor checks that the pumped supply voltage is high enough to ensure that the MOSFETs are maintained in a safe conducting state.

Continued on the next page...



**Typical Application Diagram** 



# Automotive 3-Phase Isolator MOSFET Driver

### **Description (continued)**

The A6861 is supplied in a 16-lead TSSOP (LP), with exposed pad for enhanced thermal dissipation. They are lead (Pb) free, with 100% matte tin leadframe plating.

#### **Selection Guide**

Part Number	Packing	Package
A6861KLPTR-T	13-in. reel, 4000 pieces/reel	16-Lead TSSOPwith exposed thermal pad, 4.4 X 5 mm case

#### **SPECIFICATIONS**

#### Absolute Maximum Ratings<sup>1</sup>

Characteristic	Symbol	Notes	Rating	Units
Load Voltage Supply	V <sub>BB</sub>		-0.3 to 50	V
Terminal VCP	$V_{CP}$		V <sub>BB</sub> – 0.3 to V <sub>BB</sub> + 12	V
Terminal CP1	V <sub>CP1</sub>		V <sub>BB</sub> – 12 to V <sub>BB</sub> + 0.3	V
Terminal CP2	$V_{CP2}$		$V_{BB} - 0.3 \text{ to}$ $V_{CP4} + 0.3$	V
Terminal CP3	$V_{CP3}$		V <sub>BB</sub> – 12 to V <sub>BB</sub> + 0.3	V
Terminal CP4	$V_{CP4}$		$V_{CP2} - 0.3 \text{ to}$ $V_{CP} + 0.3$	V
Terminal ENU, ENV, ENW	$V_{I}$		-0.3 to 50	V
Terminal GU, GV, GW	$V_{GX}$		$V_{SX} - 0.3 \text{ to} $ $V_{SX} + 12$	V
Terminal SU, SV, SW	$V_{SX}$		– 6 to V <sub>BB</sub> + 5	V
Operating Ambient Temperature	T <sub>A</sub>	Limited by power dissipation	-40 to 150	°C
Maximum ContinuousJunction Temperature	T <sub>J(max)</sub>		165	°C
Transient Junction Temperature	Over temperature event not exceeding 10s, lifetime duration not exceeding 10hours, guaranteed by design characterization.		175	°C
Storage Temperature	T <sub>stg</sub>		-55 to 150	°C

<sup>&</sup>lt;sup>1</sup>With respect to GND. Ratings apply when no other circuit operating constraints are present.

#### THERMAL CHARACTERISTICS may require derating at maximum conditions, see application information

The time to the term of the production of the time to					
Characteristic	Symbol	Test Conditions*	Value	Units	
Package Thermal Resistance	$R_{\theta JA}$	4-layer PCB based on JEDEC standard	34	°C/W	
(Junction to Ambient)	I VOJA	1-layer PCB with copper limited to solder pads	43	°C/W	
Package Thermal Resistance (Junction to Pad)	$R_{\theta JP}$		2	°C/W	

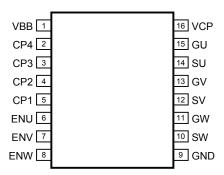
<sup>\*</sup>Additional thermal data available on the Allegro Web site.





# Automotive 3-Phase Isolator MOSFET Driver

### **Pin-out Diagram and Terminal List Table**



Package LP, 16-Pin TSSOP Pin-out Diagram

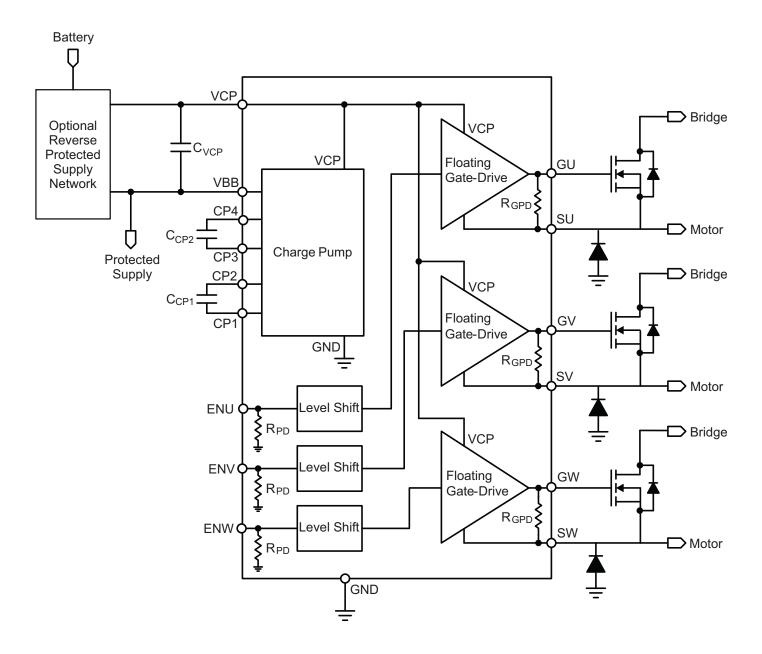
#### **Terminal List Table**

Name	Number	Description
VBB	1	Main Power Supply
CP4	2	Pump Capacitor Connection
CP3	3	Pump Capacitor Connection
CP2	4	Pump Capacitor Connection
CP1	5	Pump Capacitor Connection
ENU	6	U phase Enable Input
ENV	7	V phase Enable Input
ENW	8	W phase Enable Input
GND	9	Ground
SW	10	W Phase MOSFET Source Reference
GW	11	W Phase MOSFET Gate Drive
SV	12	V Phase MOSFET Source Reference
GV	13	V Phase MOSFET Gate Drive
SU	14	U Phase MOSFET Source Reference
GU	15	U Phase MOSFET Gate Drive
VCP	16	Pump Supply
Tab		Exposed Tab - Connect to GND





# Automotive 3-Phase Isolator MOSFET Driver



**Functional Block Diagram** 





# Automotive 3-Phase Isolator MOSFET Driver

### ELECTRICAL CHARACTERISTICS at $T_J$ = -40 to +150°C, $V_{BB}$ 6 V to 50 V (unless noted otherwise)

VBB Functional Operating Range <sup>1</sup>   VBB   Operating, Outputs active.   4.5   −   50   V	Characteristics	Symbol	Test Conditions	Min.	Тур.	Max.	Units
VBB Functional Operating Range¹         VBB         Operating. Outputs disabled         4         −         50         V           VBB Quiescent Current         IBBQ         Sx = GND.         −         10         13.5         mA           VBB Quiescent Current         IBBS         Gate drive active, VBB = 12 V, Sx = GND.         −         5.5         8         mA           VCP Quiptut voltage w.r.t. VBB         VCP         6 V < VBS ≥ 9V, Iv <sub>CP</sub> > -1 mAI <sup>23</sup> 8         10         11         V           VCP Static Load Resistance         RCP         Between VCP and VBB (using ±1% tolerance resistor)         100         −         −         kΩ           Gate Output Drive           Turn-on Time         t,         C <sub>LOAD</sub> = 10 nF, 20% to 80%         −         5         −         µs           Turn-on Time         t,         C <sub>LOAD</sub> = 10 nF, 20% to 80%         −         5         −         µs           Turn-on Time         t,         C <sub>LOAD</sub> = 10 nF, 20% to 80%         −         5         −         µs           Turn-on Time         t,         C <sub>LOAD</sub> = 10 nF, ENx light to Gx 20%         −         0         -         µs           Turn-on Disc Current         IcoAD         IcoAD </td <td>Supply</td> <td>-1</td> <td></td> <td>1</td> <td></td> <td></td> <td></td>	Supply	-1		1			
No unsafe states   0   −   50   V			Operating. Outputs active.	4.5	_	50	V
No unsafe states   0	VBB Functional Operating Range <sup>1</sup>	Vpp	Operating. Outputs disabled	4	_	50	V
SBS   SX = GND.			No unsafe states.	0	_	50	V
$V_{CP} \   \text{Output voltage w.r.t. } V_{BB} \   \begin{array}{c} V_{CP} \\ V_{CP} \   & V_{CP}$	VBB Quiescent Current	I <sub>BBQ</sub>		_	10	13.5	mA
$V_{CP} \   \text{Output voltage w.r.t.} \   V_{BB} \   \begin{array}{ c c c c c c c c c c c c c c c c c c c$		I <sub>BBS</sub>	Gate drive disabled, V <sub>BB</sub> = 12 V	_	5.5	8	mA
4.5 V \ V \ V \ B \ S \ S \ V, \ V \ V \ D \ S \ S \ S \ V, \ V \ D \ S \ S \ S \ V, \ V \ D \ S \ S \ S \ V, \ V \ D \ S \ S \ S \ V, \ V \ D \ S \ S \ S \ V, \ V \ D \ S \ S \ S \ V, \ V \ D \ D \ S \ D \ D \ D \ D \ D \ D \ D			V <sub>BB</sub> > 9V, I <sub>VCP</sub> > -1 mA <sup>[2]</sup>	9	10	11	V
Set	VCP Output voltage w.r.t. V <sub>BB</sub>	V <sub>CP</sub>	6 V < V <sub>BB</sub> ≤ 9 V, I <sub>VCP</sub> > -1 mA <sup>[2]</sup>	8	10	11	V
Fesistor   Fesisto			$4.5 \text{ V} < \text{V}_{BB} \le 6 \text{ V}, \text{I}_{VCP} > -800  \mu\text{A}^{[2]}$	7.5	9.5	_	V
Turn-on Time	VCP Static Load Resistance	R <sub>CP</sub>		100	-	-	kΩ
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Gate Output Drive				•		
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Turn-on Time	t <sub>r</sub>	C <sub>LOAD</sub> = 10 nF, 20% to 80%	_	5	_	μs
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Turn-off Time		-	_	0.5	_	μs
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Propagation Delay – Turn On <sup>3</sup>	t <sub>PON</sub>	C <sub>LOAD</sub> = 10 nF, ENx high to Gx 20%	_	-	3	μs
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Propagation Delay – Turn Off <sup>3</sup>	t <sub>POFF</sub>	C <sub>LOAD</sub> = 10 nF, ENx low to Gx 80%	_	-	1.5	μs
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Turn-on Pulse Current	I <sub>GXP</sub>		_	14	-	mA
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Turn-on Pulse Time	t <sub>GXP</sub>		_	12.5	-	μs
$ Pull-down \ On \ Resistance \  \   R_{DS(on)DN} \  \   \frac{T_{J} = 25^{\circ}C, \ I_{Gx} = 10 \ mA}{T_{J} = 150^{\circ}C, \ I_{Gx} = 10 \ mA} \  \   - \  \   10 \  \   - \  \   \Omega}{T_{J} = 150^{\circ}C, \ I_{Gx} = 10 \ mA} \  \   - \  \   10 \  \   - \  \   \Omega}  \  \   \\ Gx \ Output \ high \ voltage \  \   w.r.t. \ SX, \ or \ VBB \ if \ SX>VBB \  \   V_{GH} \  \   \frac{V_{BB}}{6} \lor V \  \   8 \  \   10 \  \   12 \  \   V \  \   \\ \frac{V_{BB}}{6} \lor V \  \   V_{BB} \le 9 \  \   V \  \   8 \  \   10 \  \   12 \  \   V \  \   \\ \frac{G_{CH}}{4.5 \ V \lor V_{BB}} \le 6 \  \   V \  \             $	On Hold Current	<del></del>		_	400	_	μA
	Dull davis On Desistance		T <sub>J</sub> = 25°C, I <sub>Gx</sub> = 10 mA	_	5	_	Ω
$V_{GH} = \begin{cases} \text{SX Output high voltage} \\ \text{w.r.t. SX, or VBB if SX>VBB} \end{cases} \qquad V_{GH} = \begin{cases} 6 \ \text{V} < V_{BB} \leq 9 \ \text{V} \\ 4.5 \ \text{V} < V_{BB} \leq 6 \ \text{V} \end{cases} \qquad 7.5 \qquad 9.5 \qquad - \qquad \text{V} \\ \text{Gate Drive Static Load Resistance} = \begin{cases} R_{GS} \\ \text{Between Gx and Sx (using $\pm 1\% tolerance resistor)} \end{cases} \qquad 100 \qquad - \qquad - \qquad k\Omega \\ \text{GX Output Voltage Low} \qquad V_{GL} \qquad -10 \ \mu\text{A} < I_{Gx} < 10 \ \mu\text{A} \qquad - \qquad - \qquad V_{Sx} + 0.3 \ \text{V} \\ \text{GX Passive Pull-down} \qquad R_{GPD} \qquad V_{Gx} - V_{Sx} < 0.3 \ \text{V} \qquad - \qquad 950 \qquad - \qquad k\Omega \\ \text{Logic Inputs & Outputs} \end{cases} \qquad 0.8 \qquad V_{IL} \qquad - \qquad - \qquad 0.8 \qquad V_{Input High Voltage} \qquad V_{IL} \qquad - \qquad - \qquad V_{Input High Voltage} \qquad V_{IH} \qquad 2.0 \qquad - \qquad - \qquad V_{Input Hysteresis} \qquad V_{Input Hysteresis} \qquad V_{Input Pull-down Resistor} \qquad R_{PD} \qquad 30 \qquad 50 \qquad 70 \qquad k\Omega \\ \text{Diagnostics & Protection} \qquad VCP Undervoltage Start-up Blank} \qquad 100 \qquad - \qquad 100 \qquad$	Pull-down On Resistance		$T_J = 150$ °C, $I_{Gx} = 10$ mA	_	10	_	Ω
w.r.t. SX, or VBB if SX>VBB		V <sub>GH</sub>	V <sub>BB</sub> > 9 V	8.5	10	12	V
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$			6 V < V <sub>BB</sub> ≤ 9 V	8	10	12	V
Gx Output Voltage Low $V_{GL}$ -10 $\mu$ A < $I_{Gx}$ < 10 $\mu$ A $-$ - $V_{SX}$ +0.3 $V$ Gx Passive Pull-down $R_{GPD}$ $V_{Gx}$ - $V_{Sx}$ < 0.3 $V$ - 950 - $K\Omega$ Logic Inputs & Outputs Input Low Voltage $V_{IL}$ 0.8 $V_{IL}$ Input High Voltage $V_{IH}$ $V_{IL}$ 2.0 $V_{IL}$ Input Hysteresis $V_{Ihys}$ 150 300 - $V_{IL}$ Input Pull-down Resistor $V_{Ihys}$ 150 300 - $V_{IL}$ Input Pull-down Resistor $V_{IL}$ 30 50 70 $V_{IL}$ $V_{IL}$ 30 50 70 $V_{IL}$ $V_{IL}$ 30 50 70 $V_{IL}$ $V_{IL}$ $V_{IL}$ 30 50 70 $V_{IL}$ $V_{IL}$ $V_{IL}$ 30 50 70 $V_{IL}$	w.r.t. SX, or VBB if SX>VBB			7.5	9.5	_	V
Gx Output Voltage Low $V_{GL}$ $-10  \mu A < I_{Gx} < 10  \mu A$ $  V_{SX} + 0.3$ $V$ Gx Passive Pull-down $R_{GPD}$ $V_{Gx} - V_{Sx} < 0.3  V$ $-$ 950 $ k\Omega$ Logic Inputs & Outputs  Input Low Voltage $V_{IL}$ $ -$ 0.8 $V$ Input High Voltage $V_{IH}$ $  V_{IN}$ $  V_{IN}$ Input Hysteresis $V_{IN}$ $  V_{IN}$ Input Pull-down Resistor $V_{IN}$	Gate Drive Static Load Resistance	R <sub>GS</sub>	Between Gx and Sx (using ±1% tolerance resistor)	100	_	_	kΩ
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Gx Output Voltage Low	V <sub>GL</sub>	-10 μA < I <sub>Gx</sub> < 10 μA	-	_	V <sub>SX</sub> +0.3	V
Logic Inputs & Outputs           Input Low Voltage         V <sub>IL</sub> -         -         0.8         V           Input High Voltage         V <sub>IH</sub> 2.0         -         -         V           Input Hysteresis         V <sub>Inys</sub> 150         300         -         mV           Input Pull-down Resistor         R <sub>PD</sub> 30         50         70         kΩ           Diagnostics & Protection           VCP Undervoltage Start-up Blank         -         100         -         Us	Gx Passive Pull-down	R <sub>GPD</sub>	$V_{Gx} - V_{Sx} < 0.3 \text{ V}$	_	950	_	kΩ
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Logic Inputs & Outputs	1					
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Input Low Voltage	V <sub>IL</sub>		_	_	0.8	V
Input Pull-down Resistor R <sub>PD</sub> 30 50 70 kΩ  Diagnostics & Protection  VCP Undervoltage Start-up Blank to the start of the	Input High Voltage	V <sub>IH</sub>		2.0	-	_	V
Input Pull-down Resistor R <sub>PD</sub> 30 50 70 kΩ  Diagnostics & Protection  VCP Undervoltage Start-up Blank 100 - 100 - 100	Input Hysteresis	V <sub>Ihys</sub>		150	300	_	mV
VCP Undervoltage Start-up Blank	Input Pull-down Resistor	<del>-</del>		30	50	70	kΩ
	Diagnostics & Protection	1					
Timer   Story     The story	VCP Undervoltage Start-up Blank Timer	t <sub>CPON</sub>		_	100	_	μs
VCP Undervoltage Legkout V <sub>CPON</sub> V <sub>CP</sub> w.r.t. V <sub>BB.</sub> V <sub>CP</sub> rising 6.2 6.7 7.2 V	VCP Undervoltage Lockout	V <sub>CPON</sub>	V <sub>CP</sub> w.r.t. V <sub>BB.</sub> V <sub>CP</sub> rising	6.2	6.7	7.2	V
VCP Undervoltage Lockout V <sub>CPOFF</sub> V <sub>CP</sub> w.r.t. V <sub>BB.</sub> V <sub>CP</sub> falling 6.0 6.5 7.0 V	VCP Undervoltage Lockout		V <sub>CP</sub> w.r.t. V <sub>BB.</sub> V <sub>CP</sub> falling	6.0	6.5	7.0	V

<sup>&</sup>lt;sup>1</sup> Function is correct but parameters are not guaranteed below the general limits (6-50V).



<sup>&</sup>lt;sup>2</sup> For input and output current specifications, negative current is defined as coming out of (sourcing) the specified device terminal.

<sup>&</sup>lt;sup>3</sup> Refer to Figure 1.

### Automotive 3-Phase Isolator MOSFET Driver

#### **FUNCTIONAL DESCRIPTION**

The A6861 is an N-channel power MOSFET driver capable of controlling MOSFETs connected as a 3-phase solid state relay in phase-isolation applications. It has three independent floating gate drive outputs to maintain the power MOSFETs in the ON state over the full supply range when the phase outputs are PWM switched with high phase-voltage slew rates.

A charge pump regulator provides the above battery supply voltage necessary to maintain the power MOSFETs in the ON state continuously when the phase voltage is equal to the battery voltage. Voltage regulation is based on the difference between VBB and VCP.

The charge pump will maintain sufficient gate drive (>7.5 V) for battery voltages down to 4.5 V. It is also able to provide the current taken by gate-source resistors as low as 100 k $\Omega$  should they be required, between the source and gate of the power MOSFETS.

The voltage generated by the charge pump can also be used to power circuitry to control the gate-source voltage for a MOSFET connected to the main supply to provide reverse battery protection

The three gate drives can be controlled independently by three logic level enable inputs. In typical applications the MOSFETs will be switched on within 8  $\mu$ s and will switch off within 1  $\mu$ s.

An undervoltage monitor checks that the pumped supply voltage is high enough to ensure that the MOSFETs are maintained in a safe conducting state

#### **Input & Output Terminal Functions**

**VBB:** Main power supply. The main power supply should be connected to VBB through a reverse voltage protection circuit.

**GND:** Main power supply return. Connect to supply ground.

**VCP:** Pumped gate drive voltage. Can be used to turn on a MOSFET connected to the main supply to provide reverse battery protection. Connect a 1  $\mu$ F ceramic capacitor between VCP and VBB.

**CP1**, **CP2**: Pump capacitor connections. Connect a 330 nF ceramic capacitor between CP1 and CP2.

**CP3**, **CP4**: Pump capacitor connections. Connect a 330 nF ceramic capacitor between CP3 and CP4.

**ENU, ENV, ENW:** Logic level enable inputs to control the gate drive outputs.

**GU, GV, GW:** Floating, gate-drive outputs for external n-channel MOSFETs.

**SU, SV, SW:** Load phase connections. These terminals are the reference connections for the floating gate-drive outputs.

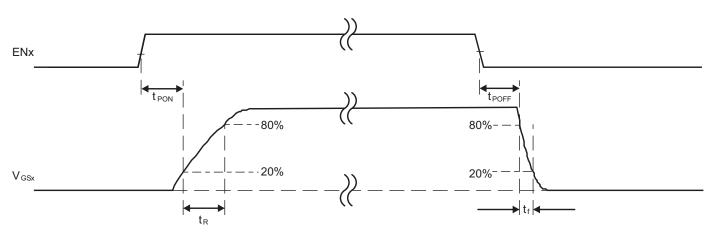


Figure 1: Enable Inputs to V<sub>GS</sub> Timing





# Automotive 3-Phase Isolator MOSFET Driver

#### **Power Supplies**

A single reverse polarity protected power supply voltage is required. It is recommended that the VBB supply is decoupled to GND by ceramic capacitors mounted close to the device pins. Decoupling capacitors are not required for correct operation but will assist in reducing switching noise conducted to the supply from the charge pump switching circuits.

The A6861 will operate within specified parameters with  $V_{\rm BB}$  from 6 V to 50 V and will function correctly with a supply down to 4.5 V. This provides a very rugged solution for use in the harsh automotive environment and permits use in start-stop systems.

There are no unsafe device states, even at low supply voltage. As the supply voltage rises from 0 V, the gate drive outputs are maintained in the off state until the gate voltage is sufficiently high to ensure conduction and the outputs are enabled.

#### **Pump Regulator**

The gate drivers are powered by a regulated charge pump, which provides the voltage above VBB to ensure that the MOSFETs are fully enhanced with low on-resistance when the source of the MOSFET is at the same voltage as  $V_{\rm BB}$ .

Voltage regulation is based on the difference between the VBB and VCP pins.

The pumped voltage,  $V_{CP}$ , is available at the VCP terminal and is limited to 12 V maximum with respect to  $V_{BB}$ . This removes the need for external clamp diodes on the power MOSFETs to limit the gate source voltage.

It also allows the VCP terminal to be used to power circuitry to control a MOSFET connected to the main supply to provide reverse battery protection.

To provide the continuous low level current required when gate-source resistors are connected to the external MOSFETs, a pump storage capacitor, typically 1  $\mu F$ , has to be connected between the VCP and VBB terminals. Pump capacitors, typically 330 nF, have to be connected between the CP1 and CP2 terminals and between the CP3 and CP4 terminals to provide sufficient charge transfer, especially at low supply voltage.

#### **Gate Drives**

The A6861 is designed to drive external, low on-resistance, power N-channel MOSFETs when used in a phase isolation application. The gate drive outputs and the  $V_{CP}$  supply will turn

the MOSFETs on in typically 8  $\mu$ s and will maintain the on-state during transients on the source of the MOSFETs. The gate drive outputs will turn the MOSFETs off in typically 1  $\mu$ s and will hold them in the off-state during transients on the source. An internal resistor,  $R_{GPD}$ , between the Gx and Sx pins plus an integrated hold-off circuit, will ensure that the gate-source voltage of the MOSFET is held close to 0 V even with the power disconnected. This can remove the need for additional gate-source resistors on the isolation MOSFETs. In any case, if gate-source resistors are mandatory for the application then the pump regulator can provide sufficient current to maintain the MOSFET in the on state with a gate-source resistor of as low as  $100 \ k\Omega$ .

The floating gate-drive outputs for external N-channel MOSFETs are provided on pins GU, GV, and GW. Gx=1 (or "high") means that the upper half of the driver is turned on and current will be sourced to the gate of the MOSFET in the phase isolation circuit, turning it on. Gx=0 (or "low") means that the lower half of the driver is turned on and will sink current from the external MOSFET's gate to the respective Sx terminal, turning it off.

The reference points for the floating drives are the load phase connections, SU, SV, and SW. The discharge current from the floating MOSFET gate capacitance flows through these connections.

In some applications it may be necessary to provide a current recirculation path when the motor load is isolated. This will be necessary in situations where the motor driver does not reduce the load current to zero before the isolation MOSFETs are turned off.

The recirculation path can be provided by connecting a suitably rated power diode to the "motor" side of the isolation MOSFETs and GND. See the Functional Block Diagram for more details. Only three diodes are required since the source to drain diodes in the isolation and bridge MOSFETs provide a recirculation path to the Battery connection.

#### **Logic Control Inputs**

Three TTL level digital inputs, ENU, ENV, & ENW, provide independent control for each gate drive. The three enable inputs directly control their respective gate drive outputs. When an enable input is high the corresponding gate drive output will be on.

These inputs have nominal hysteresis of 300 mV to improve noise performance and can be shorted to  $V_{BB}$  without damage.



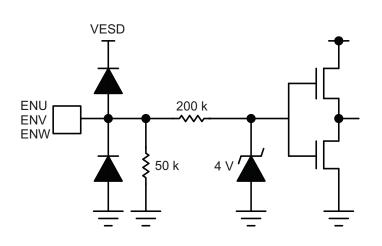
# Automotive 3-Phase Isolator MOSFET Driver

#### **Supply Monitor**

The A6861 includes undervoltage detection on the charge pump output. If the voltage at the charge pump output,  $V_{CP}$ , drops

below the falling undervoltage threshold,  $V_{CPOFF}$ , then the gate drive outputs will be held in the off state. They will remain in that state until  $V_{CP}$  rises above the rising undervoltage threshold  $V_{CPON}$ .

#### **Input and Output Structures**



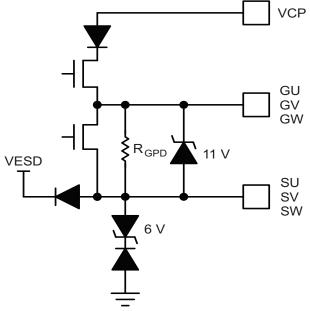


Figure 2: ENU, ENV, ENW Inputs

Figure 3: Drive Outputs

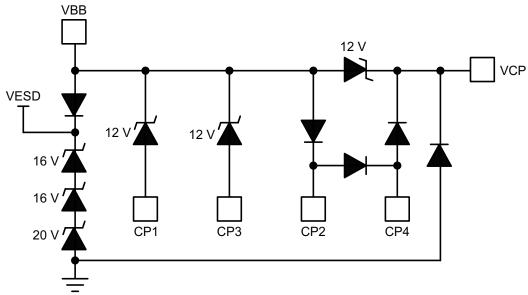


Figure 4: Supplies



# Automotive 3-Phase Isolator MOSFET Driver

#### **Battery Voltage Reversal Protection**

The charge pump output voltage may be used to drive a reverse-connected battery protection circuit as illustrated in Figure 5.

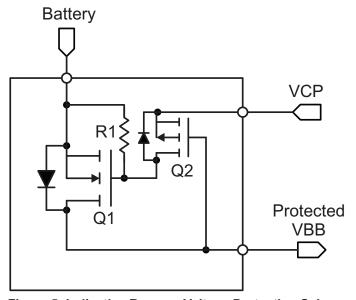


Figure 5: Indicative Reverse Voltage Protection Scheme

Transistor Q1 is an n-channel power MOSFET selected to create a low voltage drop at the full current rated for the motor drive system. It is connected with source and drain pins reversed from the normal biased condition. During power up the initial system current is supplied to VBB through the forward biased parasitic source to drain diode until  $V_{CP}$  has exceeded the threshold voltage of Q1 and turned it on.

When the battery voltage is reversed the voltage between VBB and VCP is zero, the gate source voltage on Q1 is zero and its source to drain diode becomes reverse biased. In this condition Q1 blocks current flow to VBB and the voltage between VBB and GND remains at Zero.

Transistor Q2 is a normally connected p channel, small signal MOSFET used to control the gate of Q1 in the normal and reversed battery voltage condition. Both Q1 and Q2 must be correctly rated for the full peak reversed battery voltage.

Resistor R1 is used to control the gate to source voltage of Q1 and is powered from the  $V_{CP}$  supply. To reduce the current drain from VCP the value of R1 should be a minimum defined for  $R_{CP}$ ,  $100~\rm k$ .





# Automotive 3-Phase Isolator MOSFET Driver

#### PACKAGE OUTLINE DRAWING

For Reference Only — Not for Tooling Use

(Reference MO-153 ABT)

Dimensions in millimeters. NOT TO SCALE

Dimensions exclusive of mold flash, gate burrs, and dambar protrusions

Exact case and lead configuration at supplier discretion within limits shown 1.70 B 4.40 ±0.10 6.40 ±0.20 3.00 (NOM) 3 (NOM) 0.60 ±0.15 0.29 (BSC) Branded Face SEATING PLANE 3 00 GAUGE PLANE 0.10 C PCB Layout Reference View 1.20 (MAX) 0.65 (BSC) NNNNNN 0.15  ${\mathcal A}$  YYWW 0.00 A Terminal #1 mark area 0 0 0 0 B Exposed thermal pad (bottom surface); dimensions may vary with device Reference land pattern layout (reference IPC7351 SOP65P640X110-17M);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when D Standard Branding Reference View N = Device part number  $\mathcal{A}$  = Supplier emblem Y = Last two digits of year of manufacture mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5) W = Week of manufacture L = Characters 5-8 of lot number

Figure 6: LP Package, 16-Lead TSSOP with Exposed Pad

D Branding scale and appearance at supplier discretion



# Distributor of Allegro MicroSystems, LLC: Excellent Integrated System Limited Datasheet of A6861KLPTR-T - IC MOTOR CONTROLLER PAR 16TSSOP

Contact us: sales@integrated-circuit.com Website: www.integrated-circuit.com

A6861

# Automotive 3-Phase Isolator MOSFET Driver

Revision	Date	Change		
_	February 26, 2014	Initial Release		
1	August 25, 2014	Various text edits throughout; reformatted document		
2	May 28, 2015	Corrected typo on Package Outline Drawing		
3	July 20, 2016	Updated test conditions for R <sub>CP</sub> and R <sub>GS</sub> (page 5)		

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