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[DMP6110SSS-13](#)

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DMP6110SS

60V P-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

$V_{(BR)DSS}$	$R_{DS(ON)}$ max	I_D max $T_A = +25^\circ\text{C}$
-60V	110m Ω @ $V_{GS} = -10\text{V}$	-4.5A
	130m Ω @ $V_{GS} = -4.5\text{V}$	-4.2A

Description and Applications

This MOSFET has been designed to minimize the on-state resistance ($R_{DS(ON)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

- Backlighting
- Power Management Functions
- DC-DC Converters

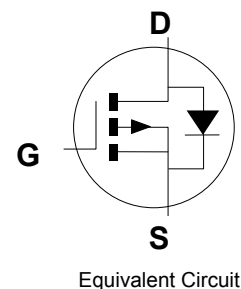
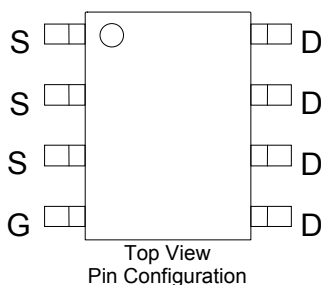
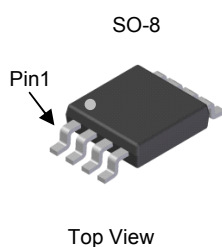
Features and Benefits

- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Low Input/ Output Leakage
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 standards for High Reliability**

Mechanical Data

- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals Connections: See Diagram
- Terminals: Finish - Matte Tin annealed over Copper lead frame. Solderable per MIL-STD-202, Method 208 (3)
- Weight: 0.072g (approximate)

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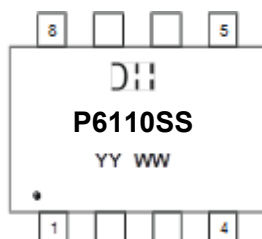
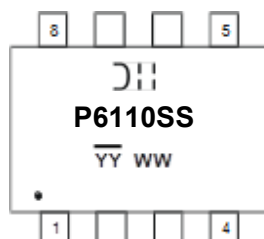


Ordering Information (Note 4)

Part Number	Case	Packaging
DMP6110SS-13	SO-8	2500/Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
 2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

Marking Information



- ⌋⌋⌋ = Manufacturer's Marking
- P6110SS = Product Type Marking Code
- YYWW = Date Code Marking
- YY or YY = Year (ex: 14 = 2014)
- WW = Week (01 - 53)
- YY = Date Code Marking for SAT (Shanghai Assembly/ Test site)
- YY = Date Code Marking for CAT (Chengdu Assembly/ Test site)

Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Value	Units
Drain-Source Voltage	V_{DSS}	-60	V
Gate-Source Voltage	V_{GSS}	± 20	V
Drain Current (Note 6) $V_{GS} = -10\text{V}$	I_D	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	A
$t < 10\text{s}$		-4.5 -3.6	
Maximum Body Diode Forward Current (Note 6)	I_S	-2.1	A
Pulsed Drain Current (10 μs pulse, duty cycle = 1%)	I_{DM}	-19	A
Avalanche Current (Notes 7) $L = 0.1\text{mH}$	I_{AS}	-17.6	A
Avalanche Energy (Notes 7) $L = 0.1\text{mH}$	E_{AS}	15.4	mJ

Thermal Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Value	Units
Total Power Dissipation (Note 5)	P_D	1.5	W
Thermal Resistance, Junction to Ambient (Note 5)	$R_{\theta JA}$	Steady State	80
		$t < 10\text{s}$	48
Total Power Dissipation (Note 6)	P_D	2.0	W
Thermal Resistance, Junction to Ambient (Note 6)	$R_{\theta JA}$	Steady State	61
		$t < 10\text{s}$	37
Thermal Resistance, Junction to Case	$R_{\theta JC}$	6.4	$^\circ\text{C/W}$
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

Electrical Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV_{DSS}	-60	—	—	V	$V_{GS} = 0\text{V}, I_D = -250\mu\text{A}$
Zero Gate Voltage Drain Current	I_{DSS}	—	—	-1	μA	$V_{DS} = -48\text{V}, V_{GS} = 0\text{V}$
Gate-Source Leakage	I_{GSS}	—	—	100	nA	$V_{GS} = \pm 16\text{V}, V_{DS} = 0\text{V}$
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	$V_{GS(th)}$	-1	—	-3	V	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$
Static Drain-Source On-Resistance	$R_{DS(on)}$	—	86	110	m Ω	$V_{GS} = -10\text{V}, I_D = -4.5\text{A}$
		—	98	130		$V_{GS} = -4.5\text{V}, I_D = -3.5\text{A}$
Diode Forward Voltage	V_{SD}	—	-0.7	-1.2	V	$V_{GS} = 0\text{V}, I_S = -1\text{A}$
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C_{iss}	—	1030	—	pF	$V_{DS} = -30\text{V}, V_{GS} = 0\text{V}, f = 1.0\text{MHz}$
Output Capacitance	C_{oss}	—	49.1	—		
Reverse Transfer Capacitance	C_{rss}	—	38.7	—		
Gate Resistance	R_G	—	13.6	—	Ω	$V_{DS} = 0\text{V}, V_{GS} = 0\text{V}, f = 1.0\text{MHz}$
Total Gate Charge ($V_{GS} = -4.5\text{V}$)	Q_g	—	9.5	—	nC	$V_{DS} = -30\text{V}, I_D = -5\text{A}$
Total Gate Charge ($V_{GS} = -10\text{V}$)	Q_g	—	19.4	—		
Gate-Source Charge	Q_{gs}	—	2.3	—		
Gate-Drain Charge	Q_{gd}	—	3.6	—		
Turn-On Delay Time	$t_{D(on)}$	—	3.7	—	ns	$V_{GS} = -10\text{V}, V_{DS} = -30\text{V}, R_{GEN} = 6\Omega, I_D = -5\text{A}$
Turn-On Rise Time	t_r	—	6.3	—		
Turn-Off Delay Time	$t_{D(off)}$	—	58.7	—		
Turn-Off Fall Time	t_f	—	26.1	—		
Body Diode Reverse Recovery Time	t_{rr}	—	14.85	—	ns	$I_S = -5\text{A}, dI/dt = 100\text{A}/\mu\text{s}$
Body Diode Reverse Recovery Charge	Q_{rr}	—	8.8	—	nC	$I_S = -5\text{A}, dI/dt = 100\text{A}/\mu\text{s}$

- Notes:
- Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
 - Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
 - UIS in production with $L = 0.1\text{mH}$, starting $T_A = +25^\circ\text{C}$.
 - Short duration pulse test used to minimize self-heating effect.
 - Guaranteed by design. Not subject to product testing.



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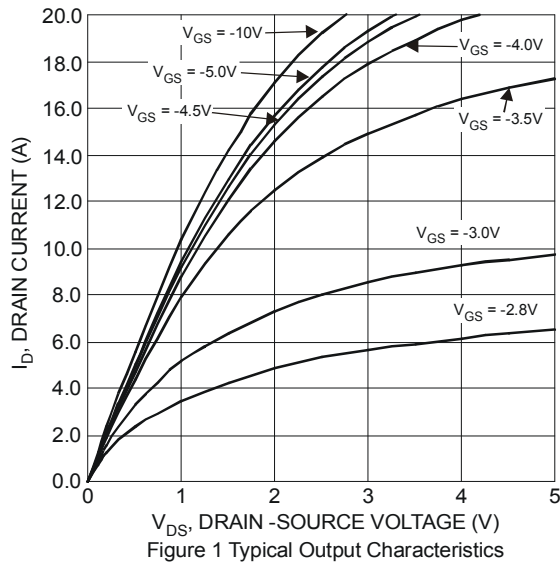


Figure 1 Typical Output Characteristics

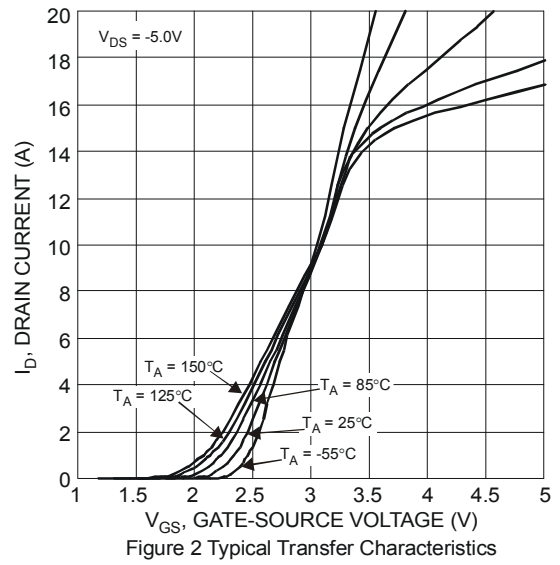


Figure 2 Typical Transfer Characteristics

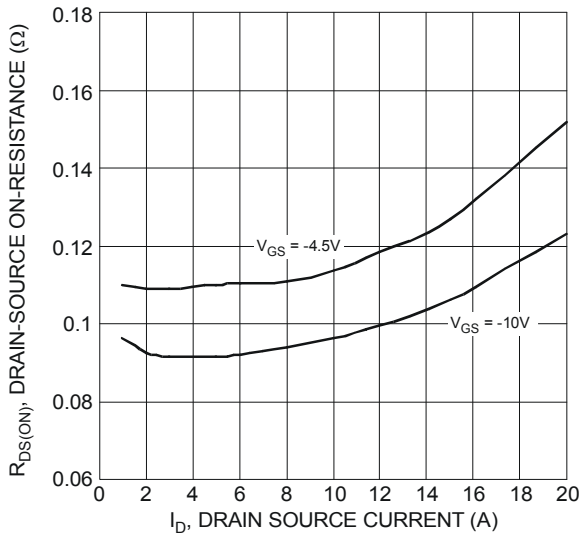


Figure 3 Typical On-Resistance vs. Drain Current and Gate Voltage

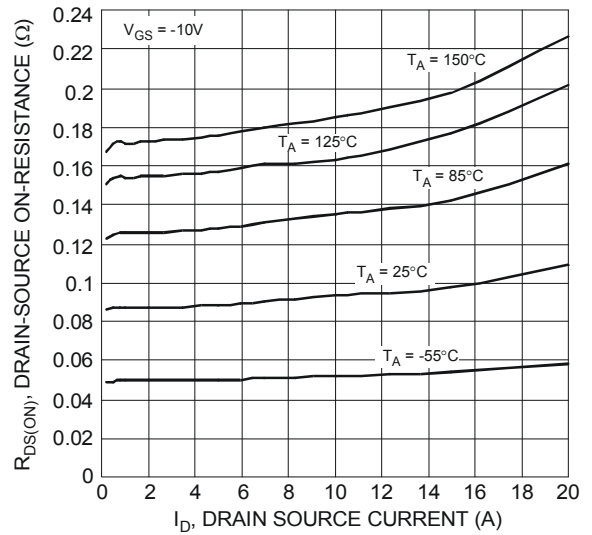


Figure 4 Typical On-Resistance vs. Drain Current and Temperature

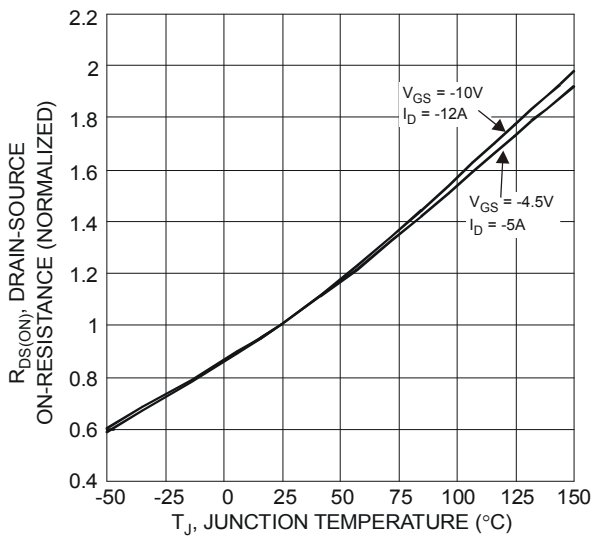


Figure 5 On-Resistance Variation with Temperature

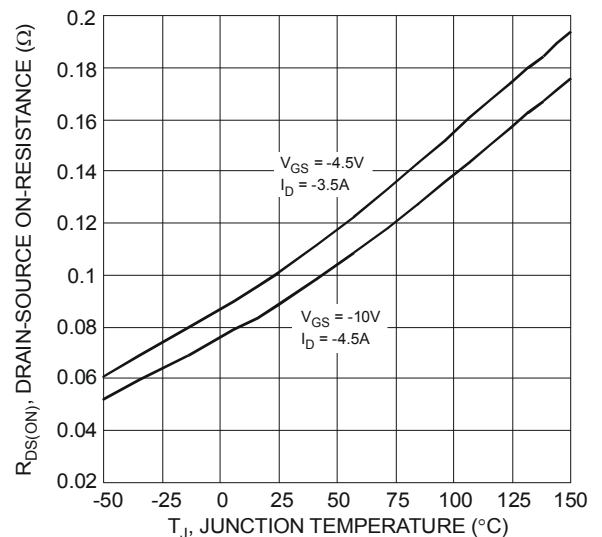


Figure 6 On-Resistance Variation with Temperature



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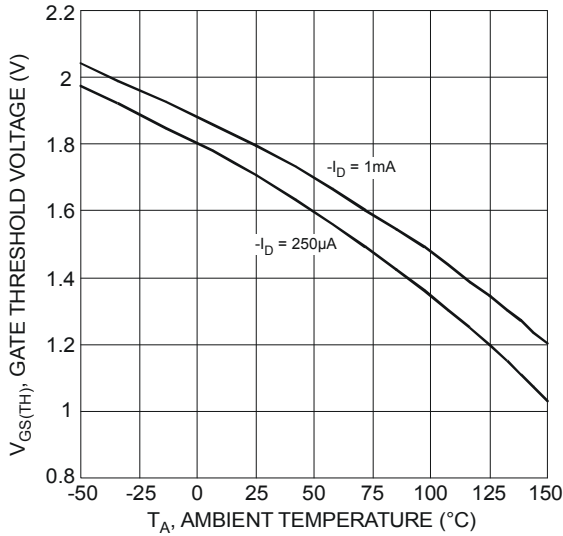


Figure 7 Gate Threshold Variation vs. Ambient Temperature

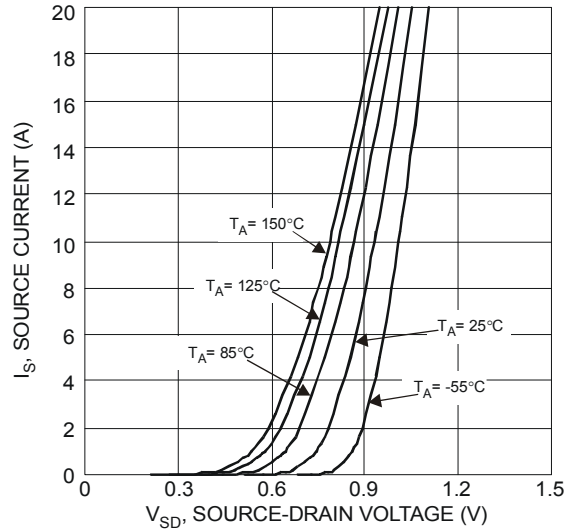


Figure 8 Diode Forward Voltage vs. Current

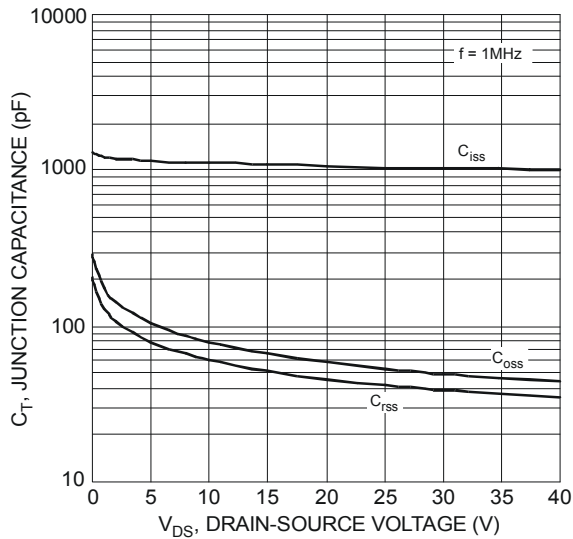


Figure 9 typical Junction Capacitance

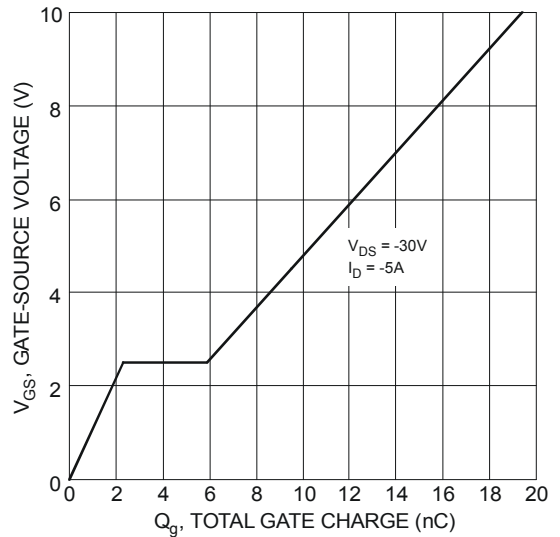


Figure 10 Gate-Charge Characteristics

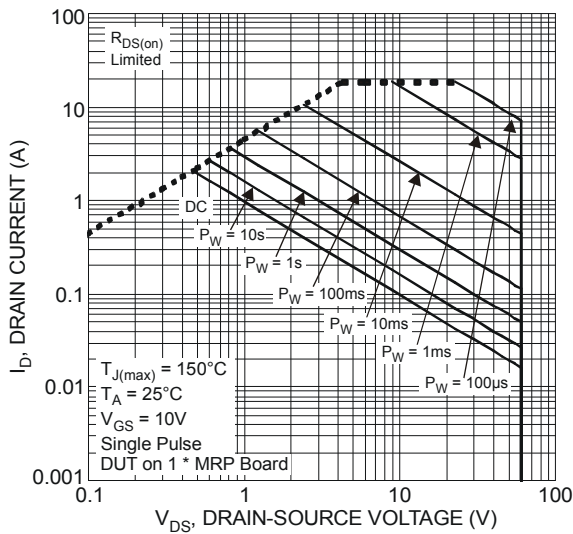
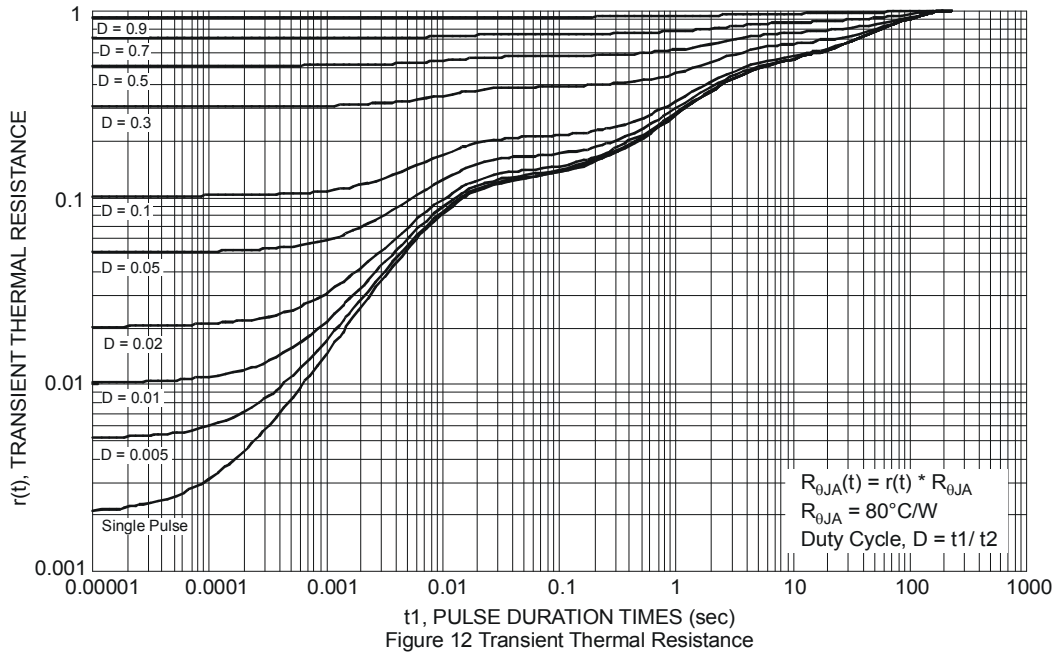
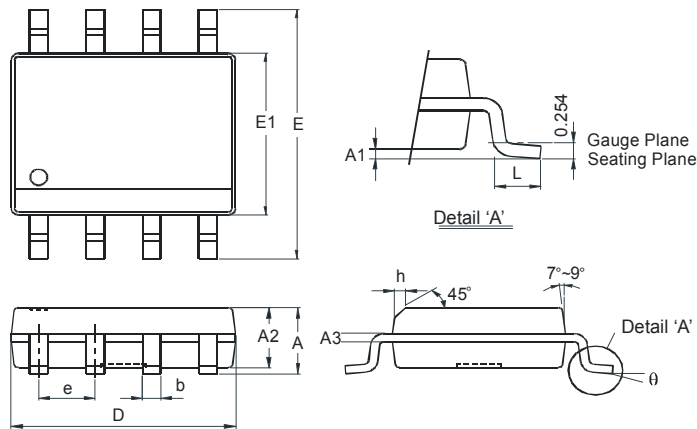


Figure 11 SOA, Safe Operation Area



Package Outline Dimensions

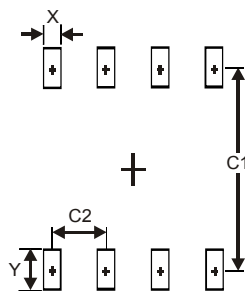
Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for the latest version.



SO-8		
Dim	Min	Max
A	-	1.75
A1	0.10	0.20
A2	1.30	1.50
A3	0.15	0.25
b	0.3	0.5
D	4.85	4.95
E	5.90	6.10
E1	3.85	3.95
e	1.27 Typ	
h	-	0.35
L	0.62	0.82
θ	0°	8°
All Dimensions in mm		

Suggested Pad Layout

Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.



Dimensions	Value (in mm)
X	0.60
Y	1.55
C1	5.4
C2	1.27

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