High Performance 1:10 Multi-Voltage CMOS Buffer

Features

- 10 single-ended outputs Fanout Buffer
- Up to 200MHz output frequency
- Ultra low output additive jitter = 0.05ps (typ.)
- Selectable reference inputs support Xtal (10~50MHz), single-ended and differential
- Low output skew ~ 50ps (typ.)
- Propagation delay ~2ns (typ@3.3V)
- 2.5V / 3.3V operation
- User configurable output VDD in different banks:
  - Mixed 3.3V core/2.5V output operating supply
  - Mixed 3.3V core/1.8V output operating supply
  - Mixed 3.3V core/1.5V output operating supply
  - Mixed 2.5V core/1.8V output operating supply
  - Mixed 2.5V core/1.5V output operating supply
- Industrial temperature range: –40°C to +85°C
- Packaging (Pb-free & Green available):
  - 32-pin TQFN (ZH)

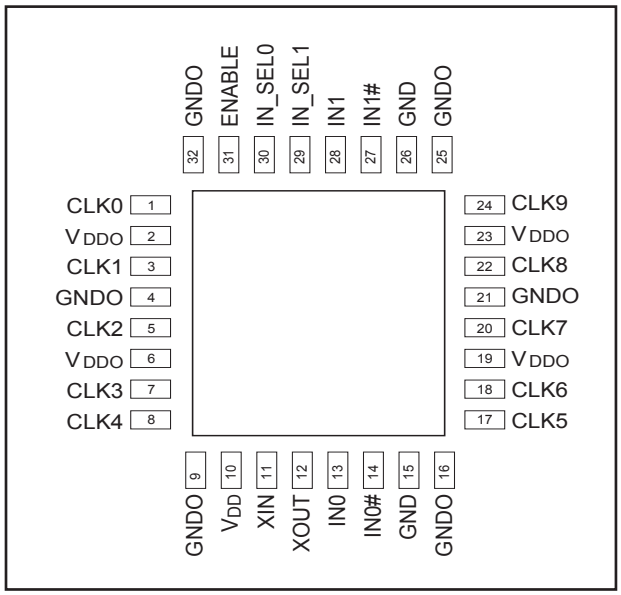
Applications

- Networking systems including switches and Routers
- High frequency backplane based computing and telecom platforms

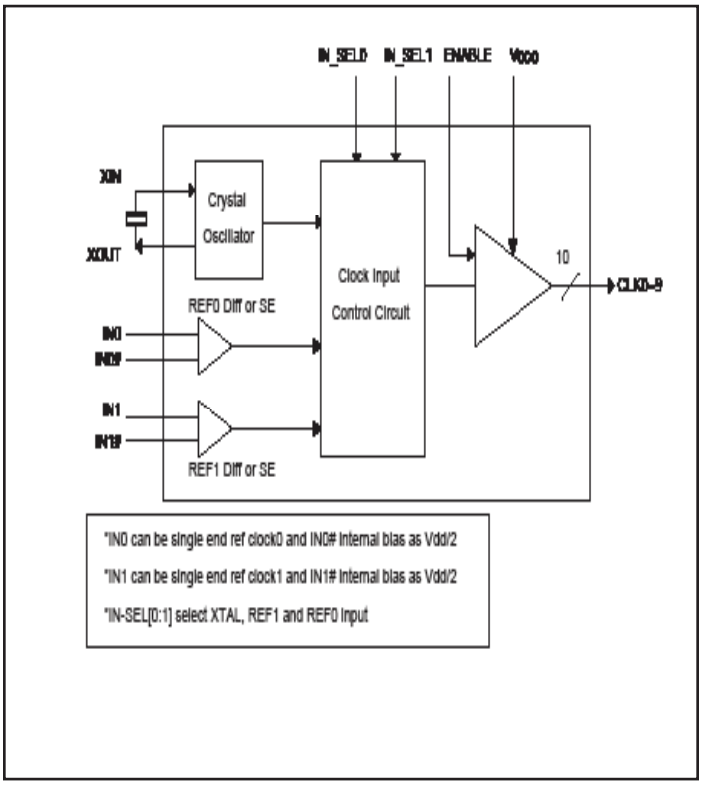
Description

The PI6C49X0210-A is a high performance multi-voltage 10-outputs CMOS Fanout Buffer with internal Crystal Oscillator. The XTAL range is from 10MHz to 50MHz. The device has a wide range of operating voltages of 2.5V and 3.3V. The device also provides user selectable output VDD option, which provides excellent flexibilities to users. This device is ideal for systems that need to distribute low jitter clock signals to multiple destinations.

Pin Configuration



Block Diagram



Pin Description

Pin#	Pin Name	Type		Description
1, 3, 5, 7, 8, 17, 18, 20, 22, 24	CLK0~9	Output		Clock Outputs
2, 6, 19, 23	V_{DDO}	Power		Output Power Supplier
15, 26	GND	Power		Output Ground
4, 9, 16, 21, 25, 32	GNDO	Power		Core Ground
10	V_{DD}	Power		Core Power Supplier
11	XIN	Input		Crystal interface
12	XOUT	Output		Crystal interface
13	IN0	Input	Pull-down	REF0 Diff or Single End
14	IN0#	Input	Pull-up/ Pull-down	REF0 Diff, When IN0 is single end ref clock0 and IN0# internal bias as Vdd/2
27	IN1#	Input	Pull-up/ Pull-down	REF1 Diff, When IN1 is single end ref clock1 and IN1# internal bias as Vdd/2
28	IN1	Input	Pull-down	REF1 Diff or Single End
30, 29	IN_SEL[0:1]	Input	Pull-down	IN-SEL[0:1] select XTAL, REF1 and REF0 input
31	ENABLE	Input		Active High Output Enable

Input Mode Selection Logic

IN_SEL0	IN_SEL1	Selected Input
1	1	XTAL
0	1	XTAL
1	0	REF1 Diff or Single End
0	0	REF0 Diff or Single End

Input/Output Operation State

Input State	Output State
IN[0:1], IN[0:1]# open	Logic Low
IN[0:1], IN[0:1]# both to ground	Logic Low
IN[0:1]=High, IN[0:1]# =Low	Logic High
IN[0:1]=Low, IN[0:1]# =High	Logic Low

Output Mode Selection

ENABLE	Output CLK0~9
GND	High-impedance
VDD	Enabled

Power Supply DC Characteristics (V_{DD}/V_{DDO} = 3.3V ± 5%, T_A = -40°C to 85°C)

Symbols	Parameters	Test Conditions	Min.	Typ	Max.	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current	ENABLE = '0'			32	mA
I_{DDO}	Output Supply Current	ENABLE = '0'			1	mA

Power Supply DC Characteristics (V_{DD}/V_{DDO} = 2.5V ± 5%, T_A = -40°C to 85°C)

Symbols	Parameters	Test Conditions	Min.	Typ	Max.	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current	ENABLE = '0'			15	mA
I_{DDO}	Output Supply Current	ENABLE = '0'			0.7	mA

Power Supply DC Characteristics (V_{DD} = 3.3V ± 5%, V_{DDO} = 2.5V ± 5%, T_A = -40°C to 85°C)

Symbols	Parameters	Test Conditions	Min.	Typ	Max.	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current	ENABLE = '0'			29	mA
I_{DDO}	Output Supply Current	ENABLE = '0'			0.6	mA

Power Supply DC Characteristics (V_{DD} = 3.3V ± 5%, V_{DDO} = 1.8V ± 0.2V, T_A = -40°C to 85°C)

Symbols	Parameters	Test Conditions	Min.	Typ	Max.	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		1.6	1.8	2.0	V
I_{DD}	Power Supply Current	ENABLE = '0'			29	mA
I_{DDO}	Output Supply Current	ENABLE = '0'			0.4	mA

Power Supply DC Characteristics (V_{DD} = 3.3V ± 5%, V_{DDO} = 1.5V ± 0.15V, T_A = -40°C to 85°C)

Symbols	Parameters	Test Conditions	Min.	Typ	Max.	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		1.35	1.5	1.65	V
I_{DD}	Power Supply Current	ENABLE = '0'			29	mA
I_{DDO}	Output Supply Current	ENABLE = '0'			0.3	mA

Power Supply DC Characteristics (V_{DD} = 2.5V ± 5%, V_{DDO} = 1.8V ± 0.2V, T_A = -40°C to 85°C)

Symbols	Parameters	Test Conditions	Min.	Typ	Max.	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		1.6	1.8	2.0	V
I_{DD}	Power Supply Current	ENABLE = '0'			13	mA
I_{DDO}	Output Supply Current	ENABLE = '0'			0.4	mA

Power Supply DC Characteristics (V_{DD} = 2.5V ± 5%, V_{DDO} = 1.5V ± 0.15V, T_A = -40°C to 85°C)

Symbols	Parameters	Test Conditions	Min.	Typ	Max.	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		1.35	1.5	1.65	V
I_{DD}	Power Supply Current	ENABLE = '0'			13	mA
I_{DDO}	Output Supply Current	ENABLE = '0'			0.3	mA

Single-Ended DC Characteristics (T_A = -40°C to 85°C)

Symbols	Parameters	Test Conditions	Min.	Typ	Max.	Units
V_{IH}	Input High Voltage	V_{DD} = 3.3V ± 5%	2		V_{DD} + 0.3	V
		V_{DD} = 2.5V ± 5%	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	V_{DD} = 3.3V ± 5%	-0.3		0.8	V
		V_{DD} = 2.5V ± 5%	-0.3		0.7	V
V_{OH}	Output High Voltage (I_{OH} = -8mA)	V_{DDO} = 3.3V ± 5% (1)	2.6			V
		V_{DDO} = 2.5V ± 5%	2.0			V
		V_{DDO} = 1.8V ± 0.2V(1)	1.5			V
		V_{DDO} = 1.5V ± 0.15V(1)	1.0			V
	Output High Voltage (I_{OH} = -12mA)	V_{DDO} = 3.3V ± 5% (1)	3.0			
		V_{DDO} = 2.5V ± 5%	2.0			
		V_{DDO} = 1.8V ± 0.2V(1)	1.5			
		V_{DDO} = 1.5V ± 0.15V(1)	1.0			
V_{OL}	Output Low Voltage (I_{OL} = 8mA)	V_{DDO} = 3.3V ± 5% (1)			0.5	V
		V_{DDO} = 2.5V ± 5%			0.5	V
		V_{DDO} = 1.8V ± 0.2V (1)			0.4	V
		V_{DDO} = 1.5V ± 0.15V (1)			0.35	V
	Output Low Voltage (I_{OL} = 12mA)	V_{DDO} = 3.3V ± 5% (1)			0.25	V
		V_{DDO} = 2.5V ± 5%			0.25	V
		V_{DDO} = 1.8V ± 0.2V (1)			0.3	V
		V_{DDO} = 1.5V ± 0.15V (1)			0.35	V
R_{OUT}	Output Impedence	V_{DDO} = 3.3V ± 5% (1)		9		Ω
		V_{DDO} = 2.5V ± 5%		10		Ω
		V_{DDO} = 1.8V ± 0.2V		20		Ω
		V_{DDO} = 1.5V ± 0.15V		30		Ω

Notes:
1. Outputs terminated with 50Ω to V_{DDO} /2. See Parameter Measurement section, "Load Test Circuit" diagrams.

Differential input DC Characteristics (T_A = -40°C to 85°C)

Symbols	Parameters		Test Conditions	Min.	Typ	Max.	Units
I_{IH}	Input High Current	IN[0:1], IN[0:1]#	V_{DD} = V_{IN} =3.465V or 2.625V			100	uA
I_{IL}	Input Low Current	IN[0:1]	V_{DD} = 3.465V or 2.625V V_{IN} = 0V	-1			uA
		IN[0:1]#	V_{DD} = 3.465V or 2.625V V_{IN} = 0V	-50			uA
V_{PP}	Peak-to-Peak Input Voltage (1)		V_{DD} = 3.3V	0.25		1.3	V
			V_{DD} = 2.5V	0.25		1.3	
V_{CMR}	Common Mode Input Voltage (1,2)		V_{DD} = 3.3V	0.5		V_{DD} -1.35V	V
			V_{DD} = 2.5V	0.5		V_{DD} -0.85V	

Notes:

1. V_{IL} should not be less than -0.3V.
2. Common mode voltage is defined as V_{IH}.

3.3V Absolute Maximum Ratings (Above which the useful life may be impaired. For user guidelines only, not tested.)

Storage Temperature	–65°C to +150°C
V_{DD}, V_{DDO} Voltage	–0.5V to +3.6V
Output Voltage (max. 4.6V)	–0.5V to V_{DD}+0.5V
Input Voltage (max 4.6V)	–0.5V to V_{DD}+0.5V

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

AC Characteristics (Over Operating Range: V_{DD}/V_{DDO} = 3.3V ± 5%, T_A = -40° to 85°C)

Parameters	Description		Test Conditions(1)	Min.	Typ	Max.	Units
f_{MAX}	Output Frequency	Using External Crystal		10		50	MHz
		Using External Clock Source (2)		DC		200	
odc	Output Duty Cycle		125MHz	45		55	%
$t_{sk(o)}$	Output Skew (3)					80	ps
$t_{jit(Ø)}$	RMS Phase Jitter (Random)		25MHz crystal @ (Integration Range: 100Hz-1MHz)		0.2		ps
$t_{jit(additive)}$	Additive RMS Phase Jitter (Random)		125MHz reference input @ (Integration Range: 12kHz-20MHz)		0.05		ps
t_R/t_F	Output Rise/Fall Time		20% to 80%	200		800	ps
t_{EN}	Output Enable Time (4)	ENABLE				5	cycles
t_{DIS}	Output Disable Time (4)	ENABLE				5	cycles
$MUX_{isolation}$	MUX Isolation		155.52MHz		64		dB

Notes:
1. Unless noted otherwise, all parameters are tested with xtal @ f <= Fxtal_max,; outputs are terminated @ 50Ω to $V_{DDO}/2$, see waveforms.
2. Diff external clock source is driving IN0/IN0# and IN1/IN1# input. IN0/IN1 can be single end ref clock when IN0# /IN1# set as $V_{DD}/2$
3. Identical conditions: loading, transitions, supply voltage, temperature, package type and speed grade.
4. These parameters are guaranteed, but not tested. Max delay is 4 cycles. Min. setup time = 3ns.

2.5V Absolute Maximum Ratings (Above which the useful life may be impaired. For user guidelines only, not tested.)

Storage Temperature	–65°C to +150°C
V_{DD}, V_{DDO} Voltage	–0.5V to +3.6V
Output Voltage (max. 4.6V)	–0.5V to V_{DD}+0.5V
Input Voltage (max 4.6V)	–0.5V to V_{DD}+0.5V

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

AC Characteristics (Over Operating Range: V_{DD}/V_{DDO} = 2.5V ± 5%, T_A = -40° to 85°C)

Parameters	Description		Test Conditions(1)	Min.	Typ	Max.	Units
f_{MAX}	Output Frequency	Using External Crystal		10		50	MHz
		Using External Clock Source (2)		DC		200	
odc	Output Duty Cycle		125MHz	45		55	%
$t_{sk(o)}$	Output Skew (3)					80	ps
$t_{jit(Ø)}$	RMS Phase Jitter (Random)		25MHz @ (Integration Range: 100Hz-1MHz)		0.2		ps
$t_{jit(additive)}$	Additive RMS Phase Jitter (Random)		125MHz @ (Integration Range: 12kHz-20MHz)		0.05		ps
t_R/t_F	Output Rise/Fall Time		20% to 80%	200		800	ps
t_{EN}	Output Enable Time (4)	ENABLE				5	cycles
t_{DIS}	Output Disable Time (4)	ENABLE				5	cycles
$MUX_{isolation}$	MUX Isolation		155.52MHz		63		dB

Notes:
1. Unless noted otherwise, all parameters are tested with xtal @ f <= Fxtal_max,; outputs are terminated @ 50Ω to $V_{DDO}/2$, see waveforms.
2. Diff external clock source is driving IN0/IN0# and IN1/IN1# input. IN0/IN1 can be single end ref clock when IN0# /IN1# set as $V_{DD}/2$
3. Identical conditions: loading, transitions, supply voltage, temperature, package type and speed grade.
4. These parameters are guaranteed, but not tested. Max delay is 4 cycles. Min. setup time = 3ns.

AC Characteristics (Over Operating Range: V_{DD} = 3.3V ± 5%, V_{DDO} = 2.5V ± 5%, T_A = -40° to 85°C)

Parameters	Description		Test Conditions[1]	Min.	Typ	Max.	Units
f_{MAX}	Output Frequency	Using External Crystal		10		50	MHz
		Using External Clock Source [2]		DC		200	
odc	Output Duty Cycle		125MHz	45		55	%
$t_{sk(o)}$	Output Skew [3]					80	ps
$t_{jit(Ø)}$	RMS Phase Jitter (Random)		25MHz @ (Integration Range: 100Hz-1MHz)		0.2		ps
$t_{jit(additive)}$	Additive RMS Phase Jitter (Random)		125MHz @ (Integration Range: 12kHz-20MHz)		0.05		ps
t_R/t_F	Output Rise/Fall Time		20% to 80%	200		800	ps
t_{EN}	Output Enable Time [4]	ENABLE				5	cycles
t_{DIS}	Output Disable Time [4]	ENABLE				5	cycles
$MUX_{isolation}$	MUX Isolation		155.52MHz		62		dB

Notes:

1. Unless noted otherwise, all parameters are tested with xtal @ f <= Fxtal_max,; outputs are terminated @ 50Ω to $V_{DDO}/2$, see waveforms.
2. Diff external clock source is driving IN0/IN0# and IN1/IN1# input. IN0/IN1 can be single end ref clock when IN0# /IN1# set as $V_{DD}/2$
3. Identical conditions: loading, transitions, supply voltage, temperature, package type and speed grade.
4. These parameters are guaranteed, but not tested. Max delay is 4 cycles. Min. setup time = 3ns.

AC Characteristics (Over Operating Range: V_{DD} = 3.3V ± 5%, V_{DDO} = 1.8V ± 0.2V, T_A = -40° to 85°C)

Parameters	Description		Test Conditions[1]	Min.	Typ	Max.	Units
f_{MAX}	Output Frequency	Using External Crystal		10		50	MHz
		Using External Clock Source [2]		DC		200	
odc	Output Duty Cycle		125MHz	45		55	%
$t_{sk(o)}$	Output Skew [3]					80	ps
$t_{jit(Ø)}$	RMS Phase Jitter (Random)		25MHz @ (Integration Range: 100Hz-1MHz)		0.15		ps
$t_{jit(additive)}$	Additive RMS Phase Jitter (Random)		125MHz @ (Integration Range: 12kHz-20MHz)		0.05		ps
t_R/t_F	Output Rise/Fall Time		20% to 80%	200		900	ps
t_{EN}	Output Enable Time [4]	ENABLE				5	cycles
t_{DIS}	Output Disable Time [4]	ENABLE				5	cycles
$MUX_{isolation}$	MUX Isolation		155.52MHz		58		dB

Notes:

1. Unless noted otherwise, all parameters are tested with xtal @ f <= Fxtal_max,; outputs are terminated @ 50Ω to $V_{DDO}/2$, see waveforms.
2. Diff external clock source is driving IN0/IN0# and IN1/IN1# input. IN0/IN1 can be single end ref clock when IN0# /IN1# set as $V_{DD}/2$
3. Identical conditions: loading, transitions, supply voltage, temperature, package type and speed grade.
4. These parameters are guaranteed, but not tested. Max delay is 4 cycles. Min. setup time = 3ns.

AC Characteristics (Over Operating Range: V_{DD} = 3.3V ± 5%, V_{DDO} = 1.5V ± 0.15V, T_A = -40° to 85°C)

Parameters	Description		Test Conditions[1]	Min.	Typ	Max.	Units
f_{MAX}	Output Frequency	Using External Crystal		10		50	MHz
		Using External Clock Source [2]		DC		200	
odc	Output Duty Cycle		125MHz	45		55	%
$t_{sk(o)}$	Output Skew [3]					80	ps
$t_{jit(Ø)}$	RMS Phase Jitter (Random)		25MHz @ (Integration Range: 100Hz-1MHz)		0.2		ps
$t_{jit(additive)}$	Additive RMS Phase Jitter (Random)		125MHz @ (Integration Range: 12kHz-20MHz)		0.05		ps
t_R/t_F	Output Rise/Fall Time		20% to 80%	200		900	ps
t_{EN}	Output Enable Time [4]	ENABLE				5	cycles
t_{DIS}	Output Disable Time [4]	ENABLE				5	cycles
$MUX_{isolation}$	MUX Isolation		155.52MHz		53		dB

Notes:

1. Unless noted otherwise, all parameters are tested with xtal @ f <= Fxtal_max,; outputs are terminated @ 50Ω to $V_{DDO}/2$, see waveforms.
2. Diff external clock source is driving IN0/IN0# and IN1/IN1# input. IN0/IN1 can be single end ref clock when IN0# /IN1# set as $V_{DD}/2$
3. Identical conditions: loading, transitions, supply voltage, temperature, package type and speed grade.
4. These parameters are guaranteed, but not tested. Max delay is 4 cycles. Min. setup time = 3ns.

AC Characteristics (Over Operating Range: V_{DD} = 2.5V ± 5%, V_{DDO} = 1.8V ± 0.2V, T_A = -40° to 85°C)

Parameters	Description		Test Conditions[1]	Min.	Typ	Max.	Units
f_{MAX}	Output Frequency	Using External Crystal		10		50	MHz
		Using External Clock Source [2]		DC		200	
odc	Output Duty Cycle		125MHz	45		55	%
$t_{sk(o)}$	Output Skew [3]					80	ps
$t_{jit(Ø)}$	RMS Phase Jitter (Random)		25MHz @ (Integration Range: 100Hz-1MHz)		0.15		ps
$t_{jit(additive)}$	Additive RMS Phase Jitter (Random)		125MHz @ (Integration Range: 12kHz-20MHz)		0.12		ps
t_R/t_F	Output Rise/Fall Time		20% to 80%	200		900	ps
t_{EN}	Output Enable Time [4]	ENABLE				5	cycles
t_{DIS}	Output Disable Time [4]	ENABLE				5	cycles
$MUX_{isolation}$	MUX Isolation		155.52MHz		59		dB

Notes:

1. Unless noted otherwise, all parameters are tested with xtal @ f <= Fxtal_max,; outputs are terminated @ 50Ω to $V_{DDO}/2$, see waveforms.
2. Diff external clock source is driving IN0/IN0# and IN1/IN1# input. IN0/IN1 can be single end ref clock when IN0# /IN1# set as $V_{DD}/2$
3. Identical conditions: loading, transitions, supply voltage, temperature, package type and speed grade.
4. These parameters are guaranteed, but not tested. Max delay is 4 cycles. Min. setup time = 3ns.

AC Characteristics (Over Operating Range: V_{DD} = 2.5V ± 5%, V_{DDO} = 1.5V ± 0.15V, T_A = -40° to 85°C)

Parameters	Description		Test Conditions[1]	Min.	Typ	Max.	Units
f_{MAX}	Output Frequency	Using External Crystal		10		50	MHz
		Using External Clock Source [2]		DC		200	
odc	Output Duty Cycle		125MHz	45		55	%
$t_{sk(o)}$	Output Skew [3]					80	ps
$t_{jit(Ø)}$	RMS Phase Jitter (Random)		25MHz @ (Integration Range: 100Hz-1MHz)		0.15		ps
$t_{jit(additive)}$	Additive RMS Phase Jitter (Random)		125MHz @ (Integration Range: 12kHz-20MHz)		0.05		ps
t_R/t_F	Output Rise/Fall Time		20% to 80%	200		900	ps
t_{EN}	Output Enable Time (4)	ENABLE				5	cycles
t_{DIS}	Output Disable Time (4)	ENABLE				5	cycles
$MUX_{isolation}$	MUX Isolation		155.52MHz		55		dB

Notes:

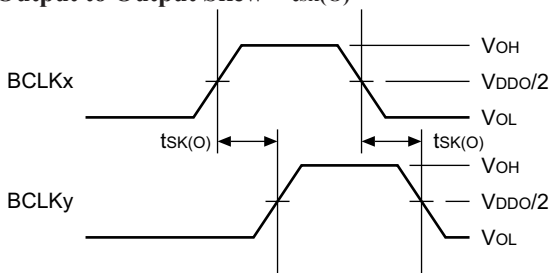
1. Unless noted otherwise, all parameters are tested with xtal @ f <= Fxtal_max,; outputs are terminated @ 50Ω to $V_{DDO}/2$, see waveforms.
2. Diff external clock source is driving IN0/IN0# and IN1/IN1# input. IN0/IN1 can be single end ref clock when IN0# /IN1# set as $V_{DD}/2$
3. Identical conditions: loading, transitions, supply voltage, temperature, package type and speed grade.
4. These parameters are guaranteed, but not tested. Max delay is 4 cycles. Min. setup time = 3ns.

Crystal Oscillator Characteristics

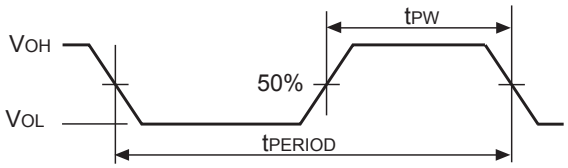
Parameters	Description	Min	Typ	Max.	Units
OSC_{MODE}	Mode of Oscillation		Fundamental		
FREQ	Frequency	10	25	50	MHz
$C_{ON-CHIP}$	On chip Load Capacitance		12		pF

Waveforms

Output to Output Skew – $t_{SK(O)}$

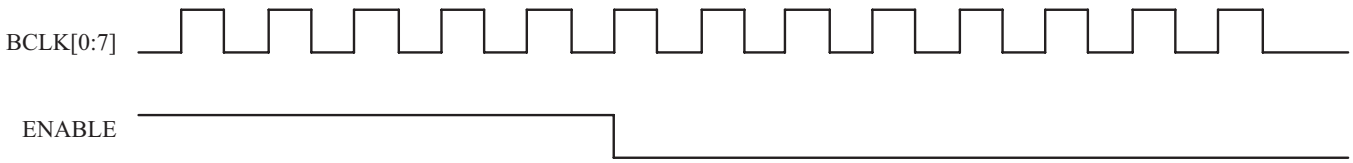


Duty Cycle – t_{DC}

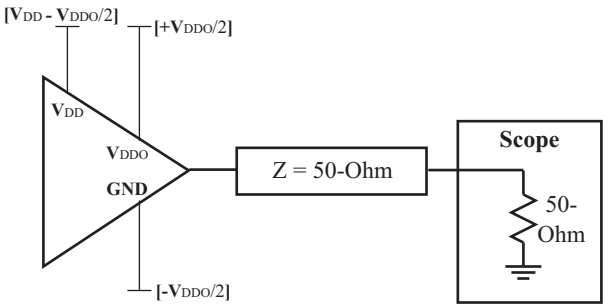


$t_{DC} = (t_{PW} / t_{PERIOD}) \times 100\%$

ENABLE Timing Diagram



AC Test Circuit Load



Note:
V_{DD}/V_{DDO} = 1.8V ± 0.2V,
2.5V ± 5%,
3.3V ± 5%

Crystal Characteristic (link to "http://www.pericom.com/products/timing/crystals/index.php" for more detailed and different size crystal specifications)

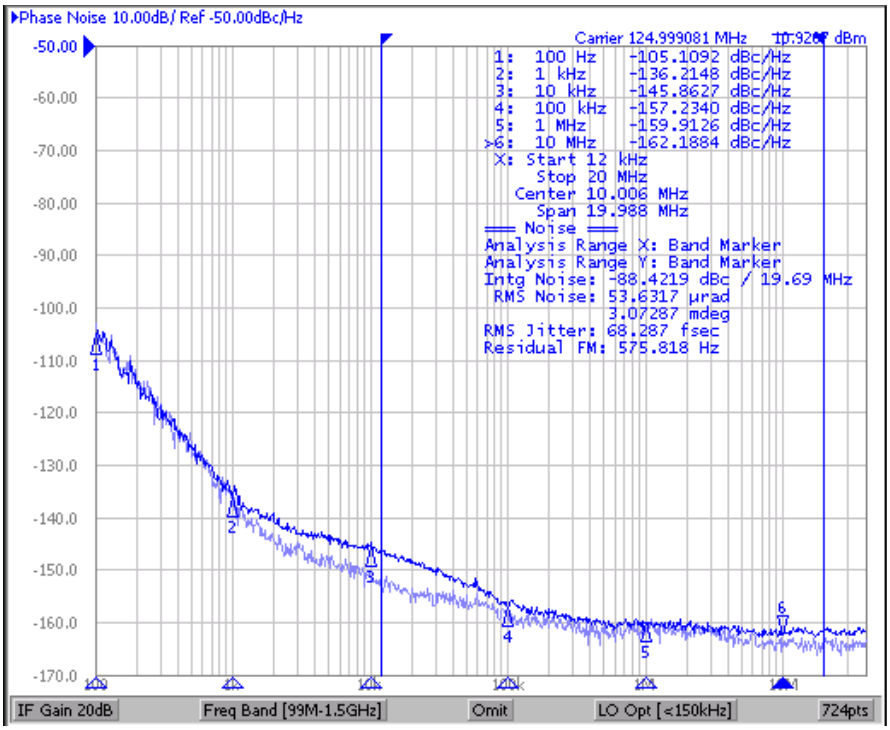
Parameters	Description	Min	Typ	Max.	Units
OSC_{MODE}	Mode of Oscillation		Fundamental		
FREQ	Frequency	10	25	50	MHz
ESR(1)	Equivalent Series Resistance	30		50	Ohm
C_{LOAD}	Load Capacitance		18		pF
C_{SHUNT}	Shunt Capacitance			7	pF
DRIVE level				1	mW

Note: 1. ESR value is dependent upon frequency of oscillation

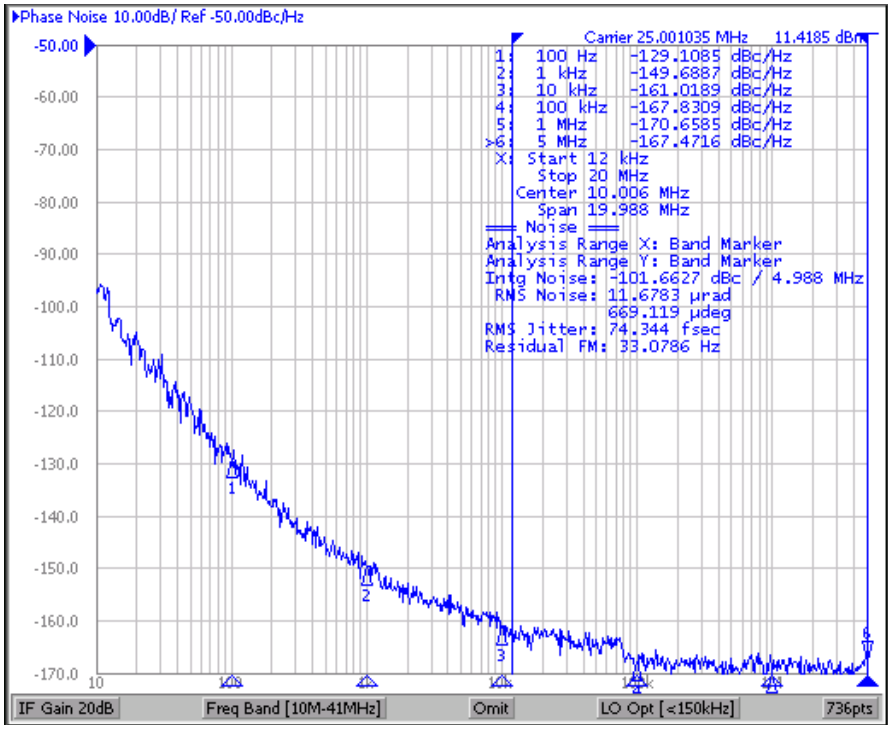
Phase Noise and Additive Jitter

Output phase noise (Dark Blue) vs Input Phase noise (light blue)

Additive jitter is calculated at ~47fs RMS (12kHz to 20MHz). Additive jitter = $\sqrt{(\text{Output jitter}^2 - \text{Input jitter}^2)}$



Oscillator Phase Jitter



Application Information

Wiring the differential input to accept single ended levels

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to postion the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R1/R2 = 0.609.

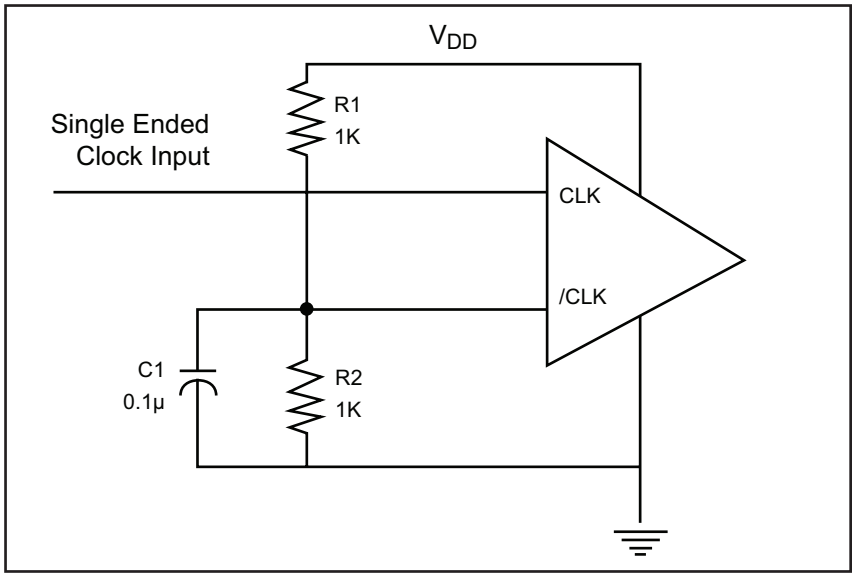
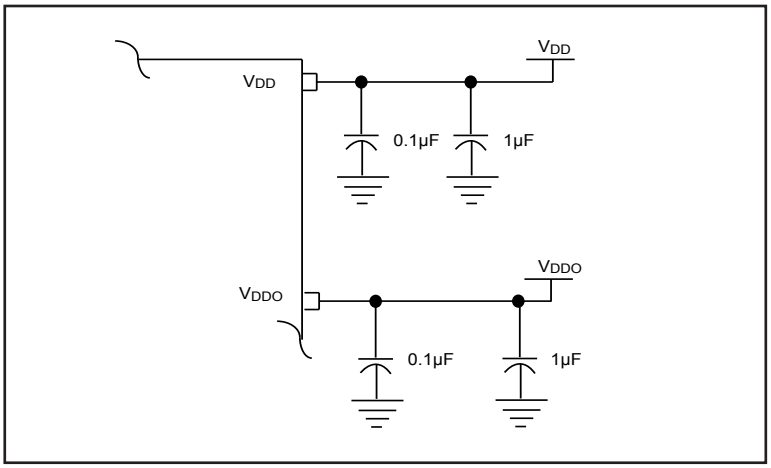


Figure 1. Single-ended input to Differential input device

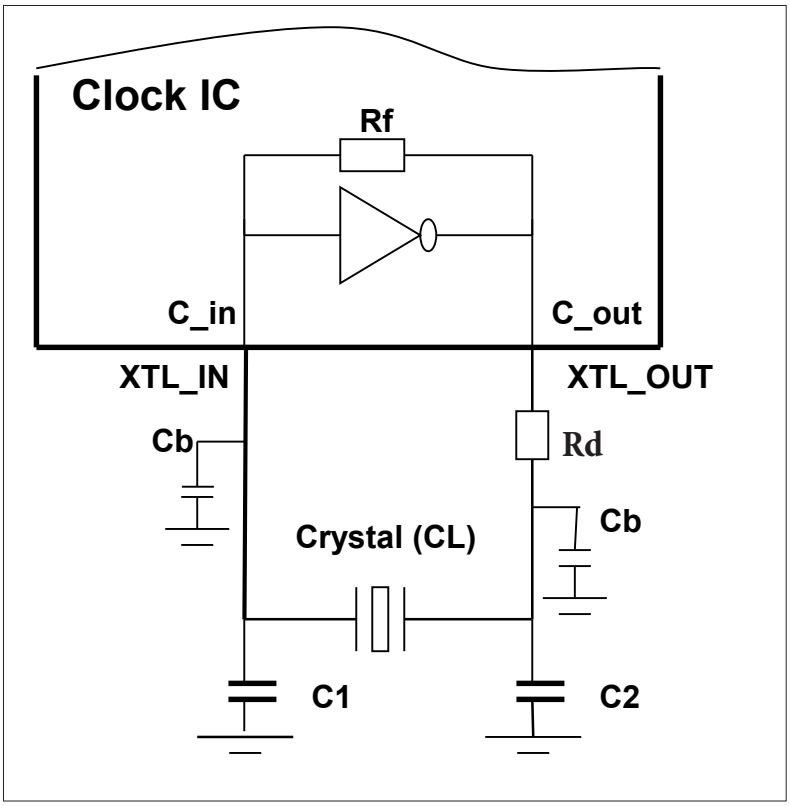
Power Supply Filtering Techniques

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. All power pins should be individually connected to the power supply plane through vias, 0.1µF and 1µF bypass capacitors should be used for each pin.



Application Notes

Clock IC Crystal loading cap. design guide



CL =crystal spec. loading cap.

C_in/out = (3~5pF) of IC pin cap.

Cb = PCB trace (2~4pF)

C1,C2 = load cap. of design

Rd = 50 to 100ohm drive level limit
(Optimized for 25MHz 18pf XTAL without Rd)

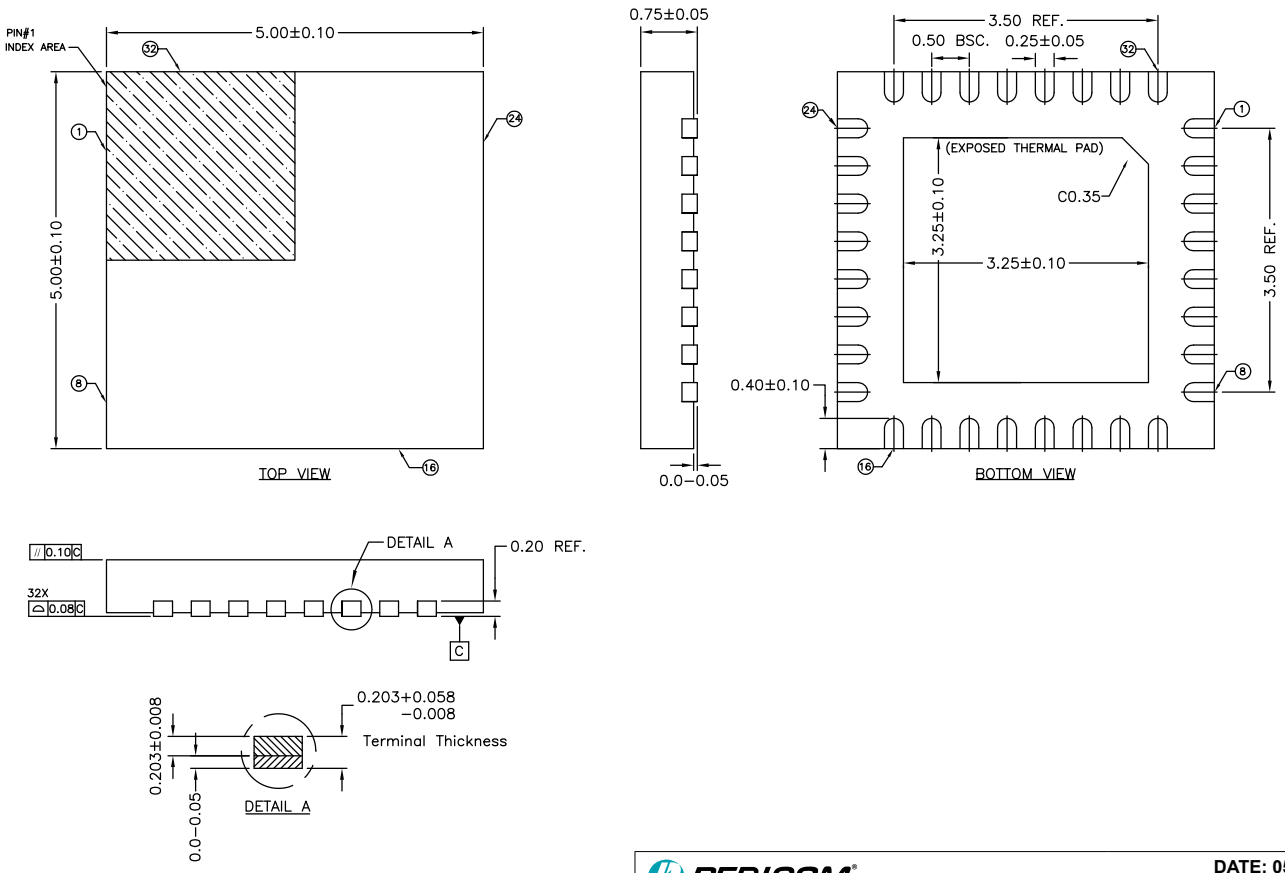
Design guide: C1=C2=2 *CL - (Cb +C_in/out) to meet target +/-ppm < 20 ppm

Example1: Select CL=18 pF crystal, C1=C2=2*(18pF) – (4pF+5pF)=27pF, check datasheet too

Example2: For higher frequency crystal (=>20MHz), can use formula C1=C2=2*(CL-6), can do fine tune of C1, C2 for more accurate ppm if necessary

Thermal Information

Symbol	Description	Condition	
Θ_{JA}	Junction-to-ambient thermal resistance	Still air	44.7 °C/W
Θ_{JC}	Junction-to-case thermal resistance		21.7 °C/W



Notes:

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO–220.
4. THERMAL PAD SOLDERING AREA (MESH STENCIL DESIGN IS RECOMMENDED)
5. THIS POD IS FOR DEVICE: **PI6C49X0210.**

PERICOM Enabling Serial Connectivity

DATE: 05/15/13

DESCRIPTION: 32-contact, Thin Quad Flat No-Lead (TQFN)

PACKAGE CODE: ZH32

DOCUMENT CONTROL #: PD-2070HW **REVISION: B**

Note:

- For latest package info, please check: http://www.pericom.com/products/packaging/mechanicals.php

Ordering Information[1,2,3]

Ordering Code	Package Code	Package Description
PI6C49X0210-AZHIE	ZH	Pb-Free and Green 32-pin TQFN

Notes:

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. E = Pb-free and Green
3. X suffix = Tape/Reel