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STF6N65M2

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STF6N65M2, STP6N65M2, STU6N65M2

N-channel 650 V, 1.2 Ω typ., 4 A MDmesh™ M2 Power MOSFETs in TO-220FP, TO-220 and IPAK packages

Datasheet - preliminary data

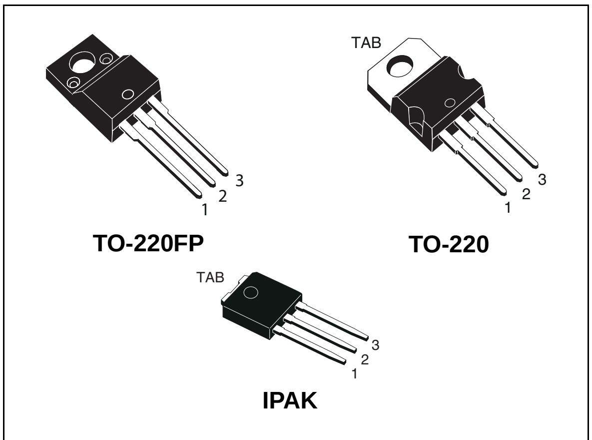
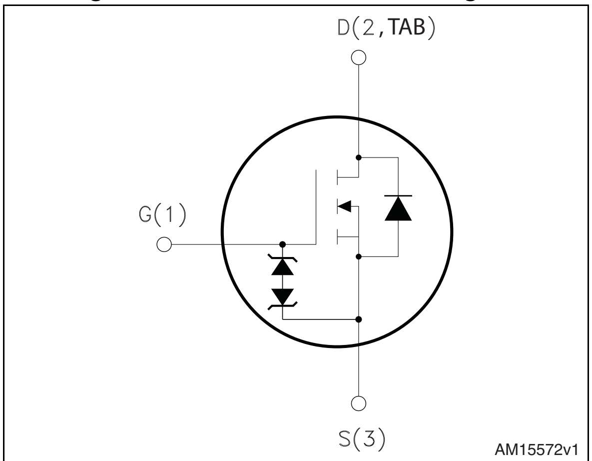


Figure 1. Internal schematic diagram



Features

Order codes	V_{DS}	$R_{DS(on)}$ max	I_D
STF6N65M2	650 V	1.35 Ω	4 A
STP6N65M2			
STU6N65M2			

- Extremely low gate charge
- Excellent output capacitance (C_{OSS}) profile
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs developed using MDmesh™ M2 technology. Thanks to their strip layout and improved vertical structure, the devices exhibit low on-resistance and optimized switching characteristics, rendering them suitable for the most demanding high efficiency converters.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STF6N65M2	6N65M2	TO-220FP	Tube
STP6N65M2		TO-220	
STU6N65M2		IPAK	

This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220FP	TO-220, IPAK	
V_{GS}	Gate-source voltage	± 25		V
I_D	Drain current (continuous) at T_C = 25 °C	4 (1)	4	A
I_D	Drain current (continuous) at T_C = 100 °C	2.5(1)	2.5	A
I_{DM}(2)	Drain current (pulsed)	16(1)	16	A
P_{TOT}	Total dissipation at T_C = 25 °C	20	60	W
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s; T_C=25 °C)	2500		V
dv/dt(3)	Peak diode recovery voltage slope	15		V/ns
dv/dt(4)	MOSFET dv/dt ruggedness	50		
T_{stg}	Storage temperature	- 55 to 150		°C
T_j	Max. operating junction temperature			

1. Limited by maximum junction temperature.
2. Pulse width limited by safe operating area.
3. $I_{SD} \leq 4$ A, di/dt ≤ 400 A/µs; $V_{DS\ peak} < V_{(BR)DSS}$, V_{DD}=400 V
4. $V_{DS} \leq 520$V

Table 3. Thermal data

Symbol	Parameter	Value			Unit
		TO-220FP	TO-220	IPAK	
$R_{thj\text{-}case}$	Thermal resistance junction-case max	6.25	2.08		°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max	62.5		100	°C/W

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	0.5	A
E_{AS}	Single pulse avalanche energy (starting T_j=25°C, I_D= I_{AR}; V_{DD}=50)	100	mJ

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0, I_D = 1 mA	650			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0, V_{DS} = 650 V			1	µA
		V_{GS} = 0, V_{DS} = 650 V, T_C=125 °C			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0, V_{GS} = ± 25 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 2 A		1.2	1.35	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{GS} = 0, V_{DS} = 100 V, f = 1 MHz	-	226	-	pF
C_{oss}	Output capacitance		-	12.8	-	pF
C_{rss}	Reverse transfer capacitance		-	0.65	-	pF
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{GS} = 0, V_{DS} = 0 to 520 V	-	114	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	6.5	-	Ω
Q_g	Total gate charge	V_{DD} = 520 V, I_D = 4 A, V_{GS} = 10 V (see *Figure 8*)	-	9.8	-	nC
Q_{gs}	Gate-source charge		-	1.7	-	nC
Q_{gd}	Gate-drain charge		-	4	-	nC

1. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 325 V, I_D = 2 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 15* and *Figure 20*)	-	19	-	ns
t_r	Rise time		-	7	-	ns
$t_{d(off)}$	Turn-off delay time		-	6.5	-	ns
t_f	Fall time		-	20	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		4	A
I_{SDM} (1)	Source-drain current (pulsed)		-		16	A
V_{SD} (2)	Forward on voltage	I_{SD} = 4 A, V_{GS} = 0	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 4 A, di/dt = 100 A/µs V_{DD} = 60 V (see *Figure 17*)	-	260		ns
Q_{rr}	Reverse recovery charge		-	1.2		µC
I_{RRM}	Reverse recovery current		-	9.2		A
t_{rr}	Reverse recovery time	I_{SD} = 4 A, di/dt = 100 A/µs V_{DD} = 60 V, T_j = 150 °C (see *Figure 17*)	-	400		ns
Q_{rr}	Reverse recovery charge		-	1.84		µC
I_{RRM}	Reverse recovery current		-	9.1		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220FP

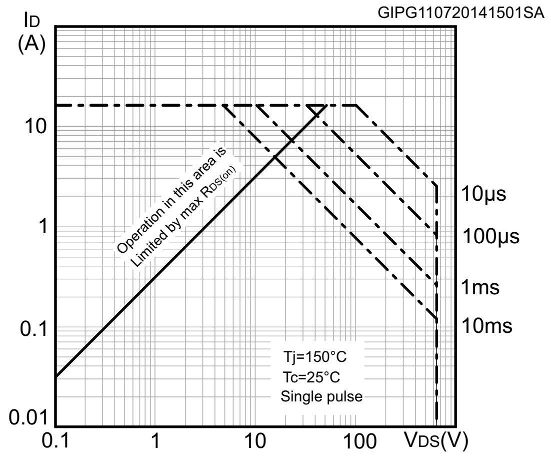


Figure 3. Thermal impedance for TO-220FP

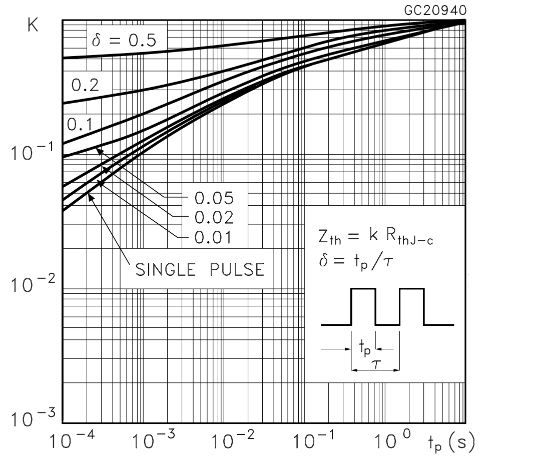


Figure 4. Safe operating area for TO-220 and IPAK

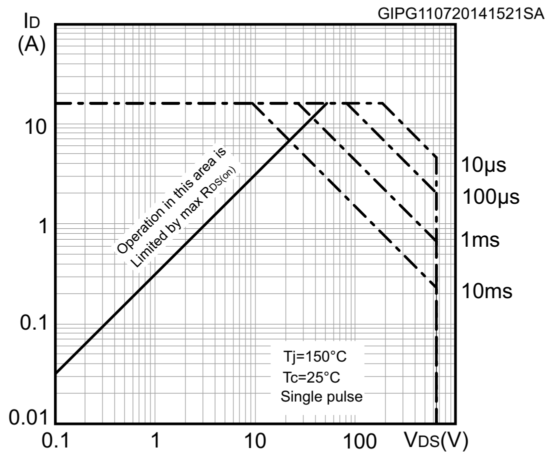


Figure 5. Thermal impedance for TO-220 and IPAK

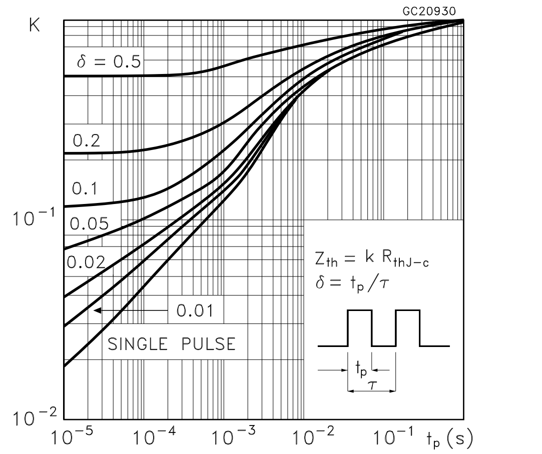


Figure 6. Output characteristics

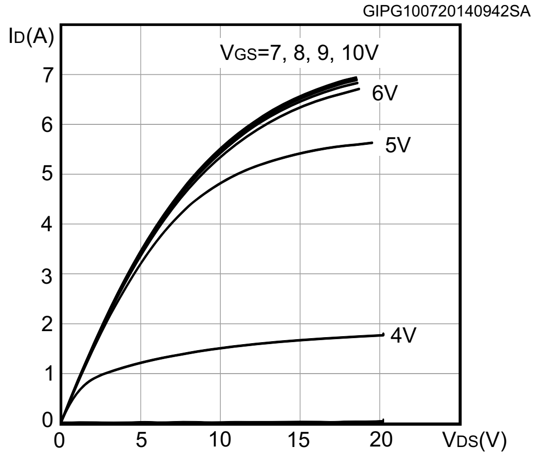


Figure 7. Transfer characteristics

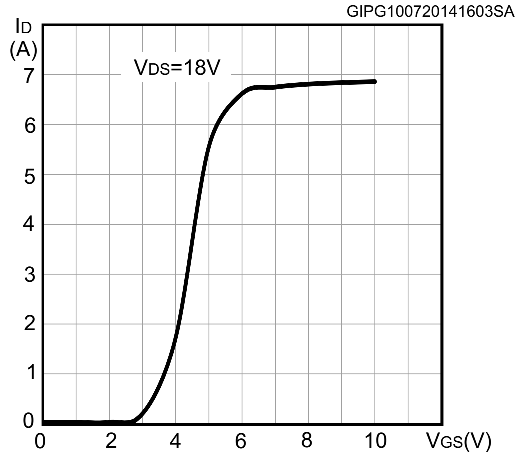


Figure 8. Gate charge vs gate-source voltage

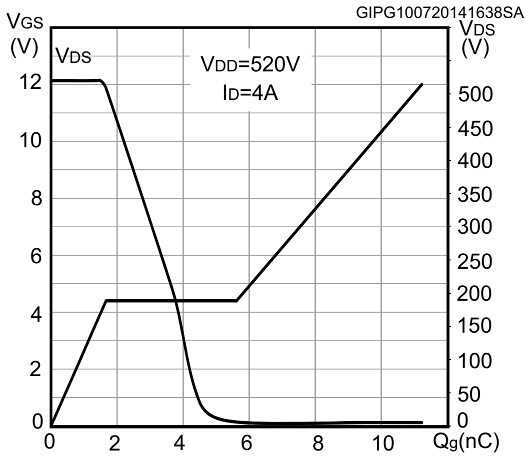


Figure 9. Static drain-source on-resistance

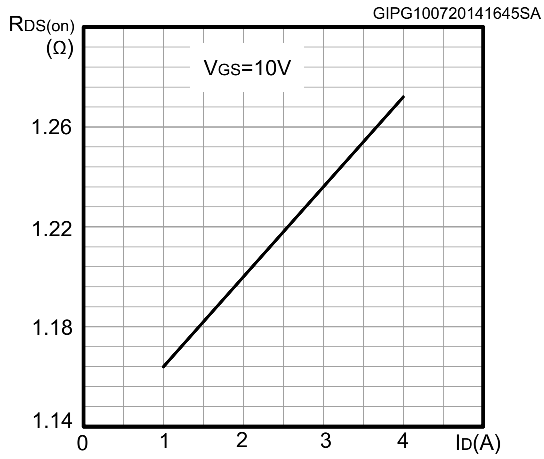


Figure 10. Capacitance variations

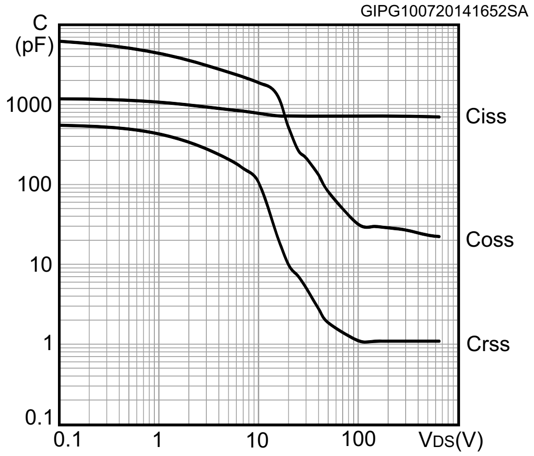


Figure 11. Normalized gate threshold voltage vs temperature

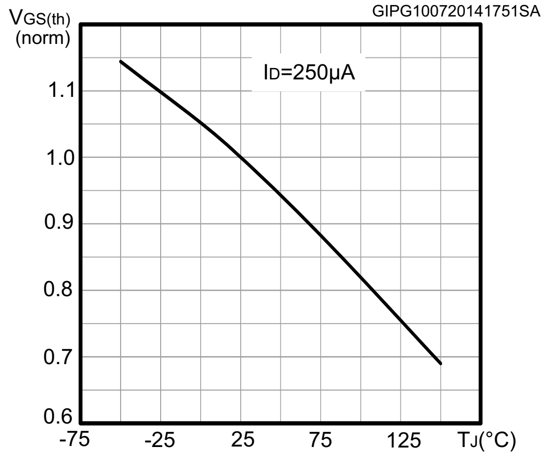


Figure 12. Normalized on-resistance vs temperature

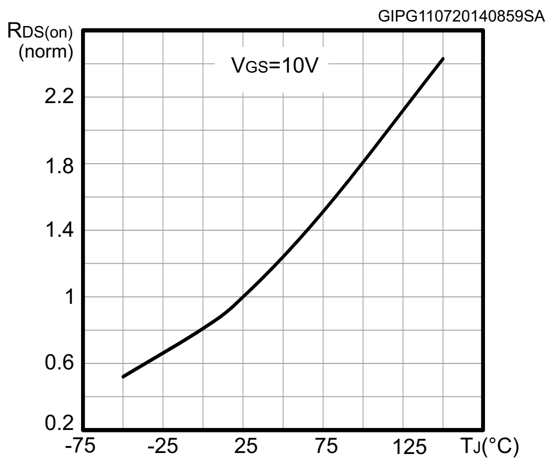


Figure 13. Normalized $V_{(BR)DSS}$ vs temperature

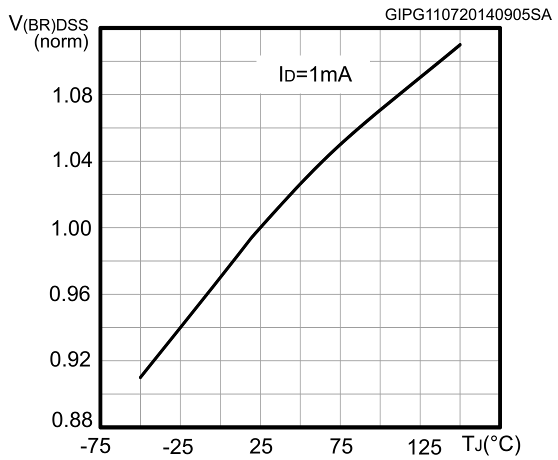
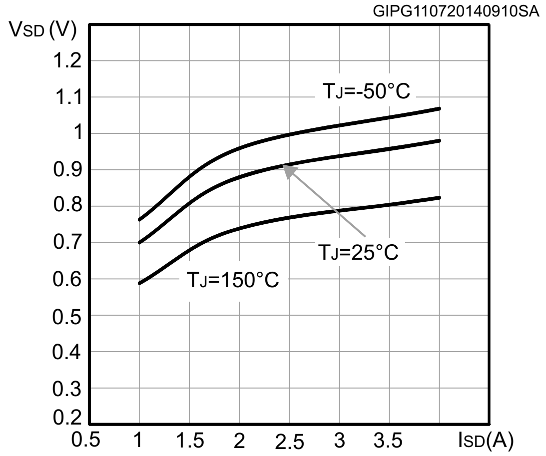


Figure 14. Source-drain diode forward characteristics



3 Test circuits

Figure 15. Switching times test circuit for resistive load

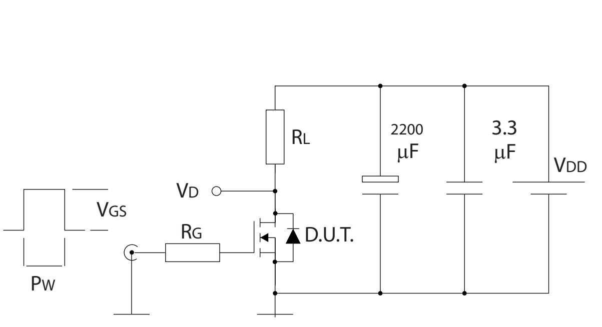


Figure 16. Gate charge test circuit

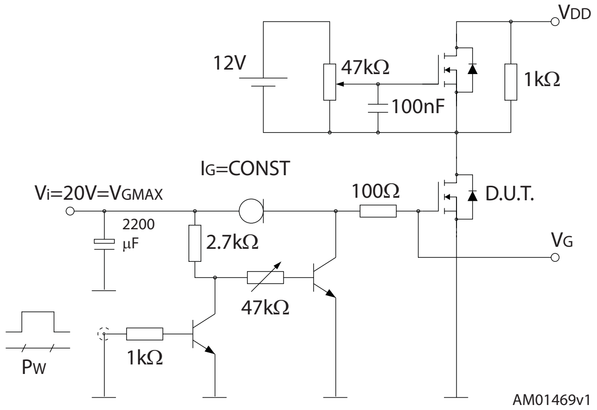


Figure 17. Test circuit for inductive load switching and diode recovery times

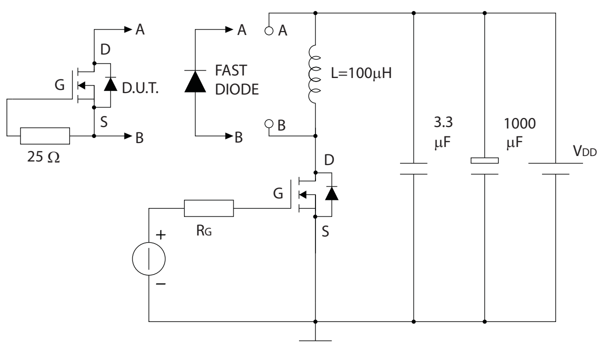


Figure 18. Unclamped inductive load test circuit

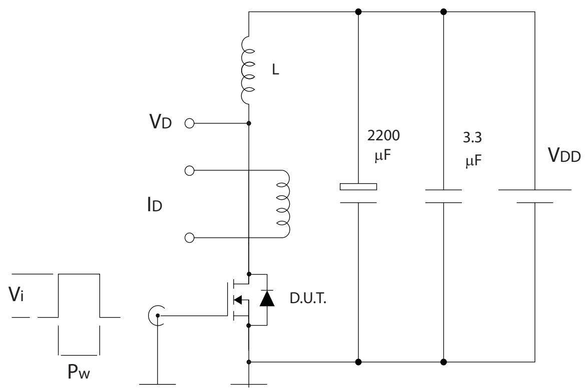


Figure 19. Unclamped inductive waveform

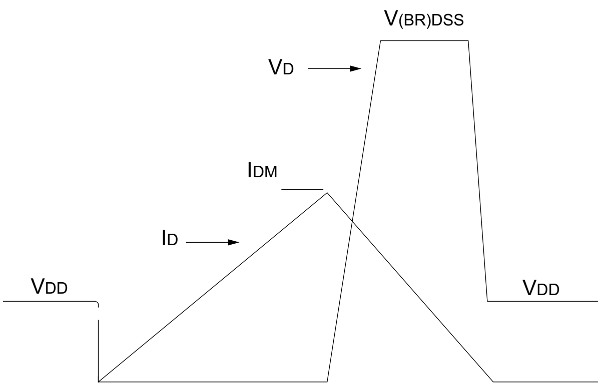
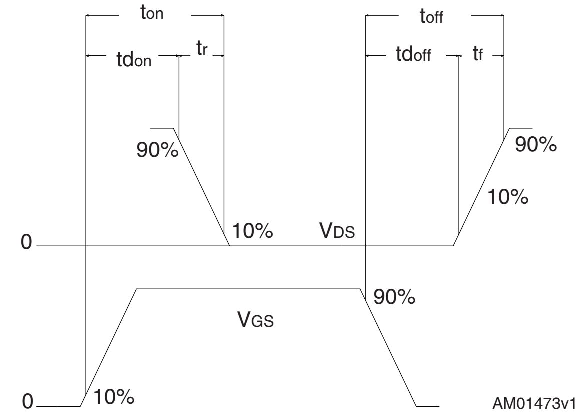


Figure 20. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

4.1 TO-220FP, STF6N65M2

Figure 21. TO-220FP drawing

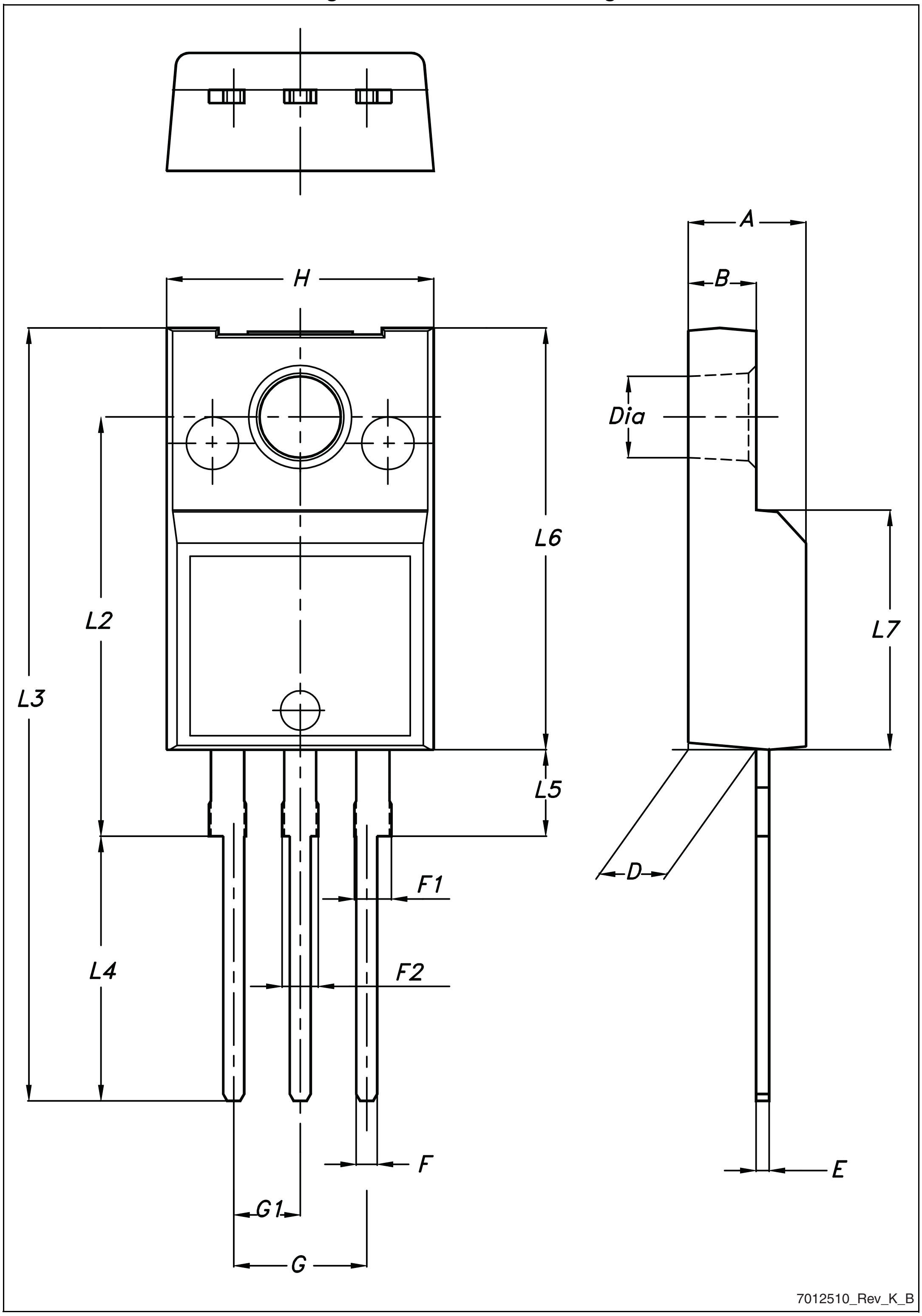


Table 9. TO-220FP mechanical data

Dim.	mm		
	Min.	**Typ.**	**Max.**
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Ø	3		3.2

4.2 TO-220, STP6N65M2

Figure 22. TO-220 type A drawing

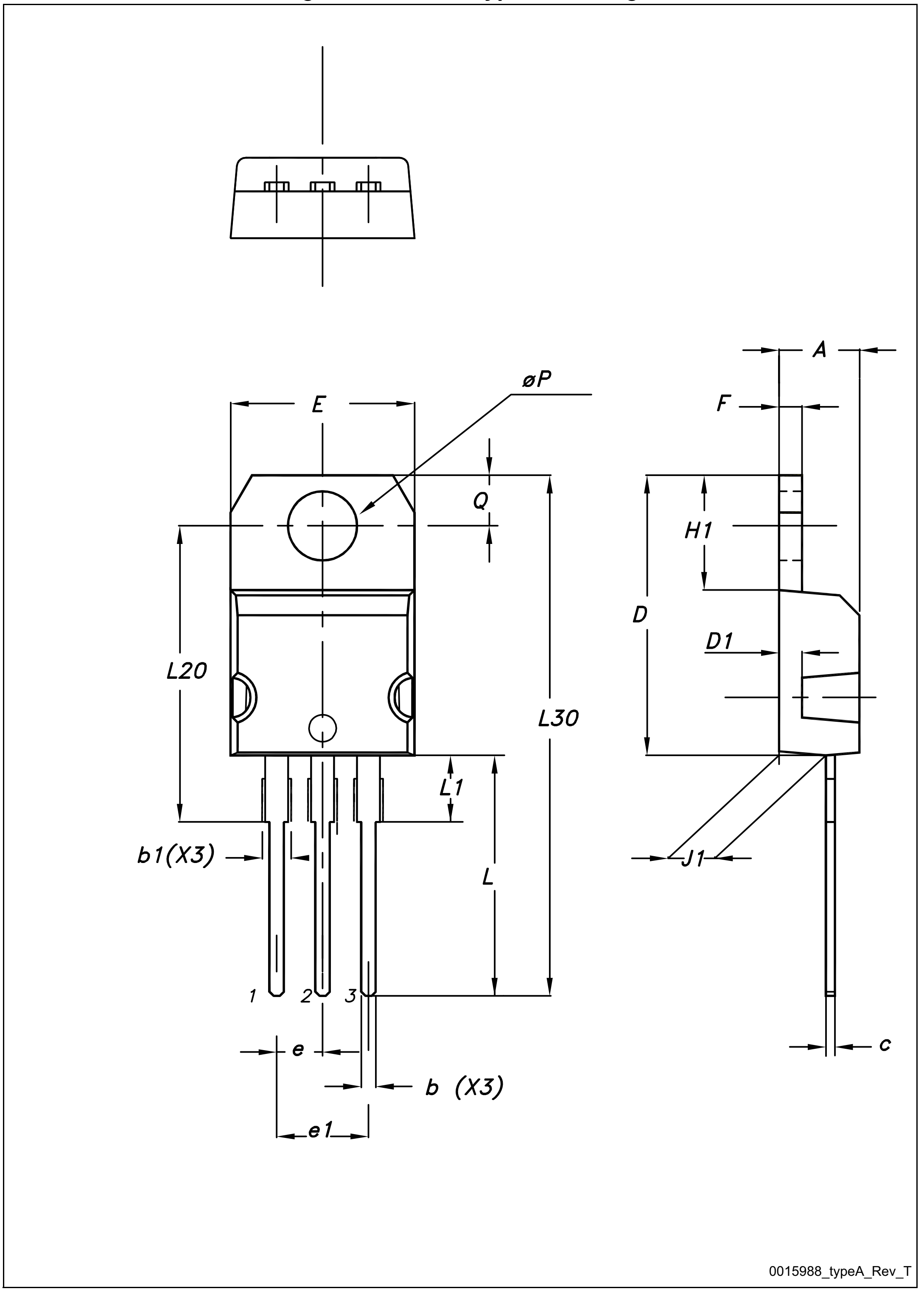


Table 10. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95

4.3 IPAK, STU6N65M2

Figure 23. IPAK (TO-251) drawing

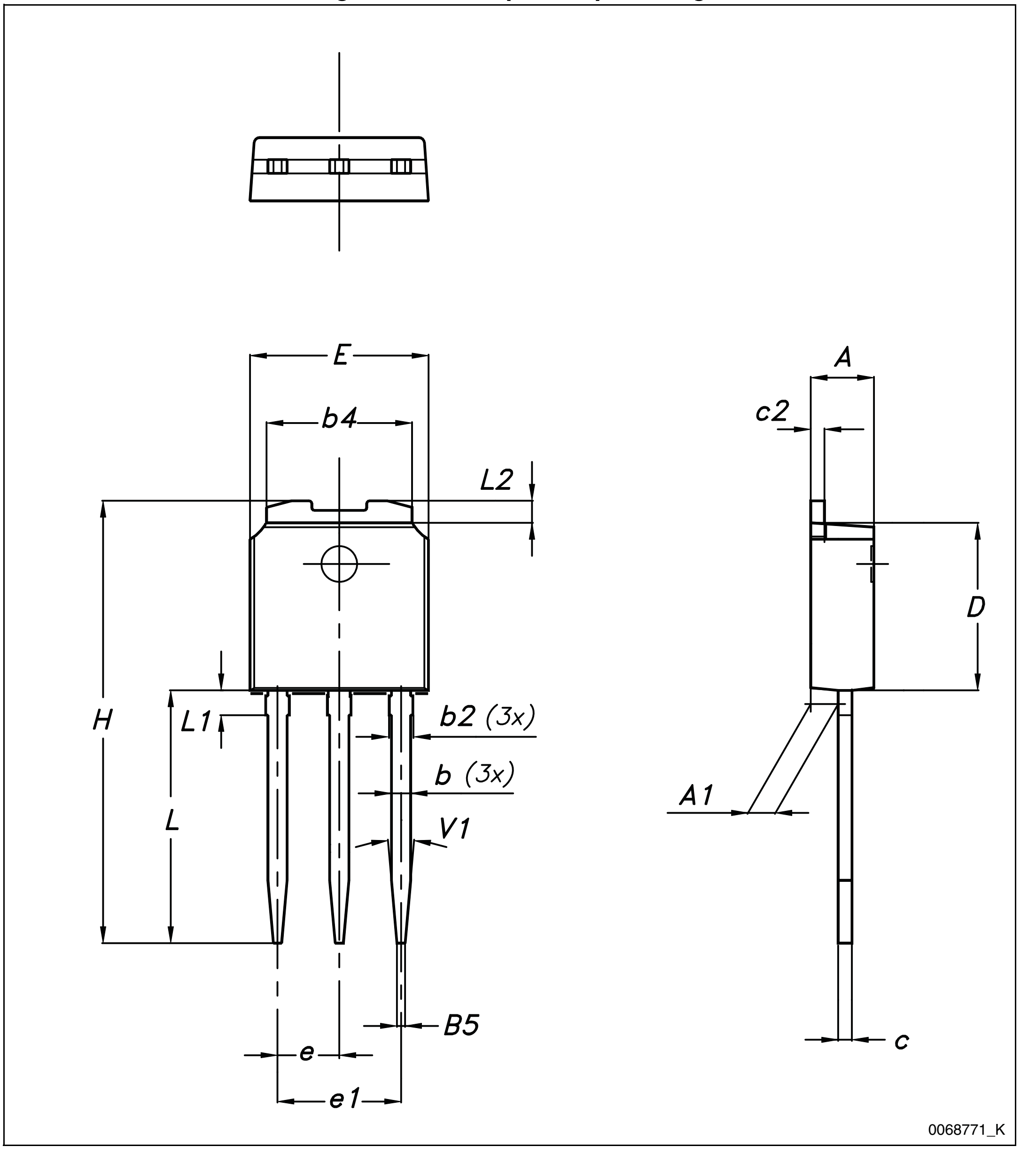


Table 11. IPAK (TO-251) mechanical data

DIM	mm.		
	min.	typ.	max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.30	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10°	

5 Revision history

Table 12. Document revision history

Date	Revision	Changes
04-Aug-2014	1	First release.