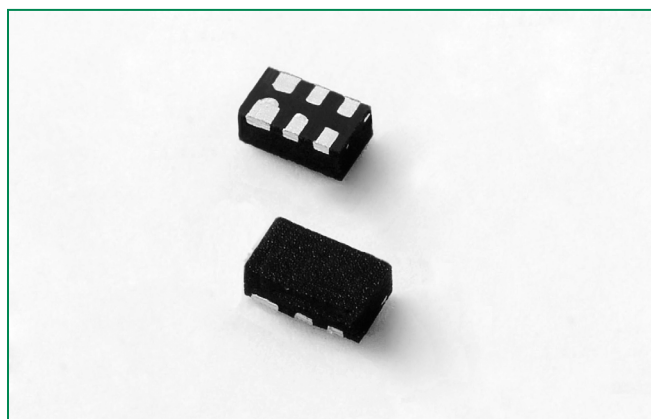
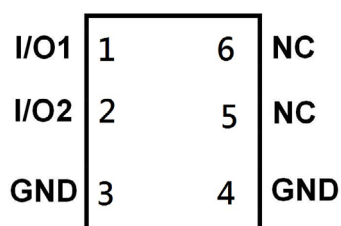


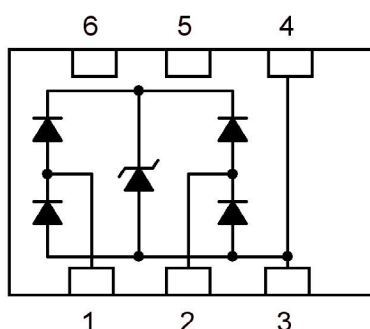
SP3014 Series 1.0pF, 15kV Diode Array



Pinout



Functional Block Diagram



Additional Information



Datasheet



Resources



Samples

Life Support Note:

Not Intended for Use in Life Support or Life Saving Applications

The products shown herein are not designed for use in life sustaining or life saving applications unless otherwise expressly indicated.

Description

The SP3014 series integrates 2 channels of low capacitance steering diodes and an additional zener diode to provide protection for electronic equipment that may experience destructive electrostatic discharges (ESD). The SP3014 can safely absorb repetitive ESD strikes above the maximum level specified in the IEC61000-4-2 international standard ($\pm 8\text{kV}$ contact discharge) without performance degradation.

The low loading capacitance makes it ideal for protecting high-speed signal lines such as USB2.0 and 1Gb Ethernet with an extremely low dynamic resistance to protect the most sensitive, state of the art chipsets against ESD transients.

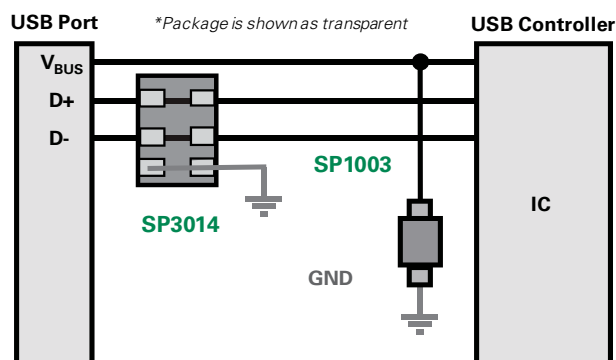
Features

- ESD, IEC61000-4-2, $\pm 15\text{kV}$ contact, $\pm 25\text{kV}$ air
- EFT, IEC61000-4-4, 80A ($t_p=5/50\text{ns}$)
- Lightning, IEC61000-4-5, 8A ($t_p=8/20\mu\text{s}$)
- Low capacitance of 1.0pF (TYP) per I/O
- Low leakage current of 1.0 μA (MAX) at 5V
- Small form factor μDFN (JEDEC MO-229) package provides flow through routing to simplify PCB layout
- AEC-Q101 qualified

Applications

- LCD/PDP TVs
- External Storages
- DVD/Blu-ray Players
- Set Top Boxes
- Smartphones
- Ultrabooks/Notebooks
- Digital Cameras
- Portable Medical
- Automotive Electronics
- Wearable Technology

USB 2.0 Protection Application Example



Absolute Maximum Ratings

Symbol	Parameter	Value	Units
I_{PP}	Peak Current ($t_p=8/20\mu s$)	8.0	A
T_{OP}	Operating Temperature	-40 to 125	°C
T_{STOR}	Storage Temperature	-55 to 150	°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Thermal Information – μ DFN-6L

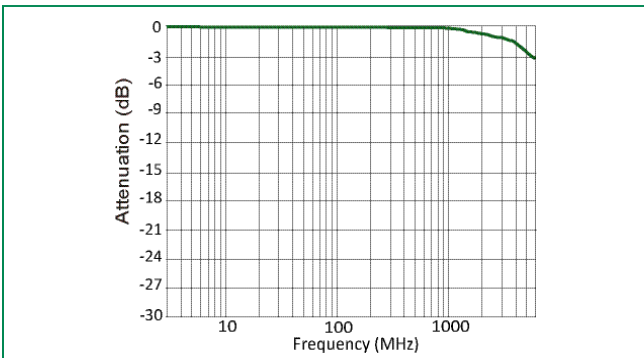
Parameter	Rating	Units
Thermal Resistance Junction to Ambient	124.21	°C/W
Thermal Resistance Junction to Case	190.54	°C/W
Power Dissipation	1	W

Electrical Characteristics ($T_{OP}=25^\circ C$)

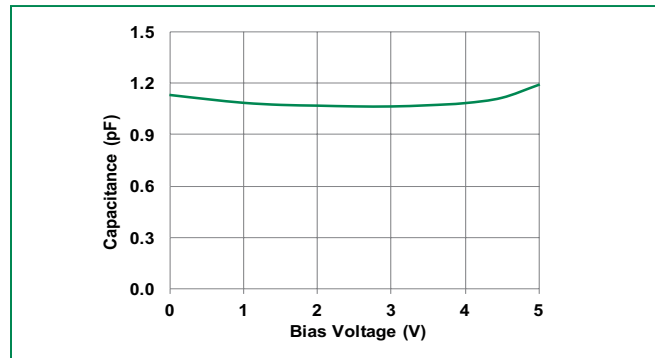
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Reverse Standoff Voltage	V_{RWM}	$I_R \leq 1\mu A$			5.0	V
Reverse Leakage Current	I_{LEAK}	$V_R=5V$, Any I/O to GND			1.0	μA
Clamp Voltage ¹	V_C	$I_{PP}=1A$, $t_p=8/20\mu s$, Fwd		6.6		V
		$I_{PP}=2A$, $t_p=8/20\mu s$, Fwd		6.8		V
Dynamic Resistance ¹	R_{DYN}	$(V_{C2} - V_{C1}) / (I_{PP2} - I_{PP1})$		0.2		Ω
Dynamic Resistance ²	R_{DYN}	TLP, $t_p=100ns$, I/O to GND		0.25		Ω
ESD Withstand Voltage ¹	V_{ESD}	IEC61000-4-2 (Contact)	± 15			kV
		IEC61000-4-2 (Air)	± 25			kV
Diode Capacitance ¹	$C_{I/O-GND}$	Reverse Bias=0V, f=1 MHz		1.0		pF
Diode Capacitance ¹	$C_{I/O-I/O}$	Reverse Bias=0V, f=1 MHz		0.5		pF

Note: 1 Parameter is guaranteed by design and/or device characterization.
 2. Transmission Line Pulse (TLP) with 100ns width and 200ps rise time.

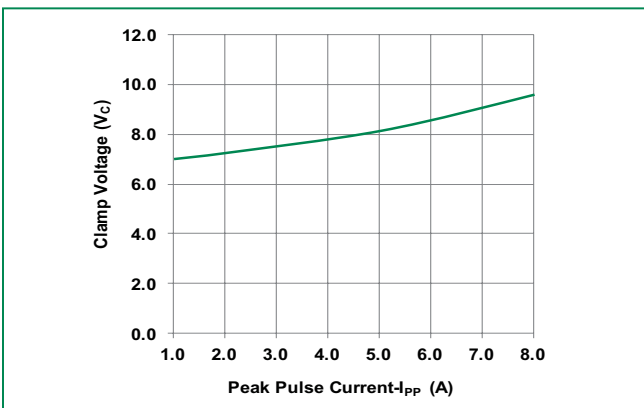
Insertion Loss (S21) I/O to GND



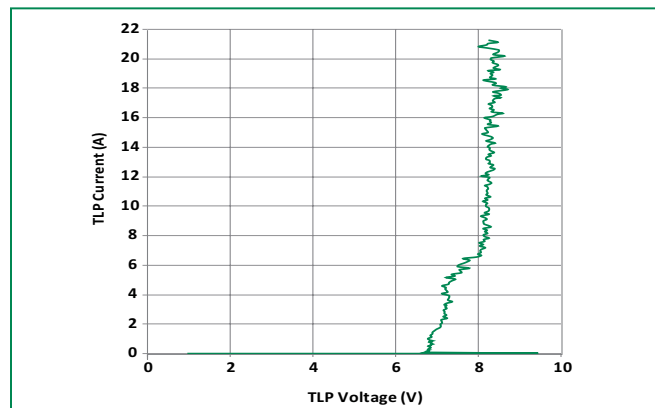
Capacitance vs. Reverse Bias



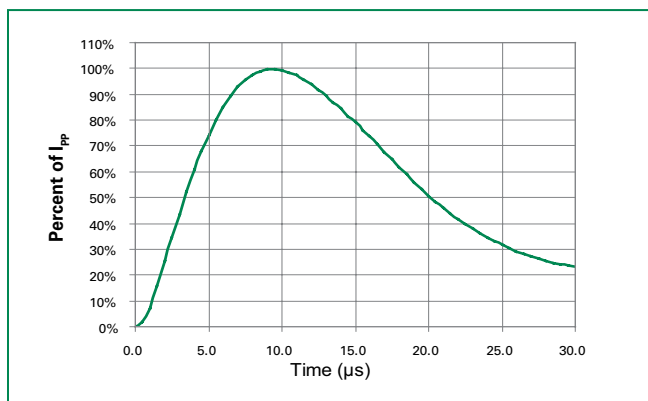
Clamping Voltage vs. I_{PP}



Transmission Line Pulse (TLP)

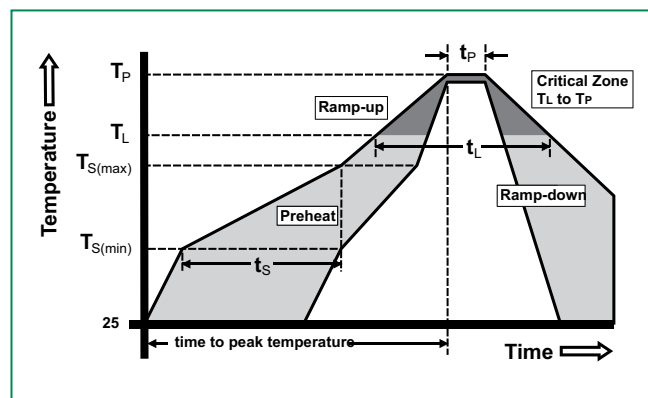


Pulse Waveform



Soldering Parameters

Reflow Condition	Pb – Free assembly	
Pre Heat	- Temperature Min ($T_{s(min)}$)	150°C
	- Temperature Max ($T_{s(max)}$)	200°C
	- Time (min to max) (t_s)	60 – 180 secs
Average ramp up rate (Liquidus) Temp (T_L) to peak	3°C/second max	
$T_{s(max)}$ to T_L - Ramp-up Rate	3°C/second max	
Reflow	- Temperature (T_L) (Liquidus)	217°C
	- Temperature (t_L)	60 – 150 seconds
Peak Temperature (T_p)	260 ^{+0/-5} °C	
Time within 5°C of actual peak Temperature (t_p)	20 – 40 seconds	
Ramp-down Rate	6°C/second max	
Time 25°C to peak Temperature (T_p)	8 minutes Max.	
Do not exceed	260°C	



Ordering Information

Part Number	Package	Marking	Min. Order Qty.
SP3014-02UTG	µDFN-6L	Ⓟ H2	3000

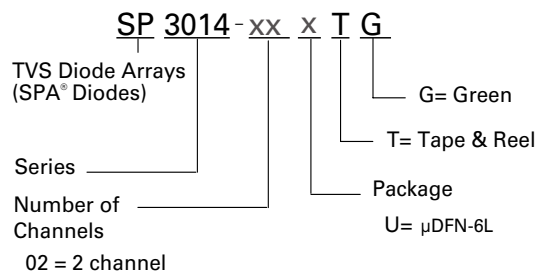
Product Characteristics

Lead Plating	Pre-Plated Frame (µDFN)
Lead Material	Copper Alloy
Lead Coplanarity	0.0004 inches (0.102mm)
Substrate material	Silicon
Body Material	Molded Epoxy
Flammability	UL 94 V-0

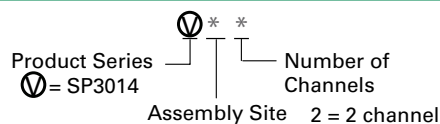
Notes :

1. All dimensions are in millimeters
2. Dimensions include solder plating.
3. Dimensions are exclusive of mold flash & metal burr.
4. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
5. Package surface matte finish VDI 11-13.

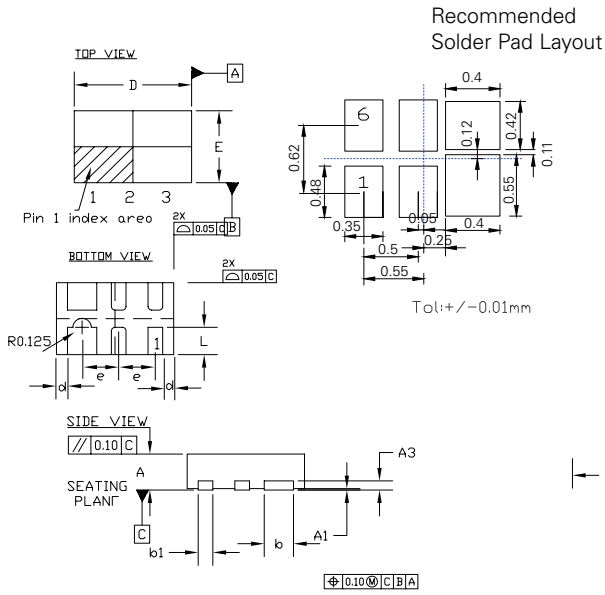
Part Numbering System



Part Marking System

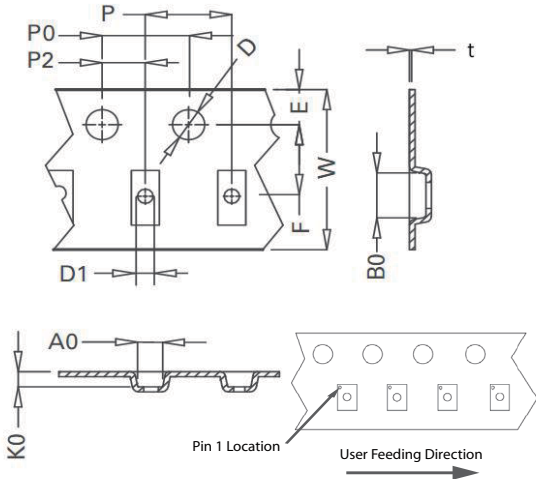


Package Dimensions —μDFN-6L



Package	μDFN-6L			
JEDEC	MO-229			
Pins	6			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.45	0.55	0.018	0.022
A1	0.00	0.05	0.000	0.002
A3	0.125 REF		0.005 REF	
b	0.35	0.45	0.014	0.018
b1	0.15	0.25	0.006	0.010
D	1.55	1.65	0.062	0.065
d	0.10	0.20	0.004	0.008
E	0.95	1.05	0.038	0.042
e	0.50 REF		0.020 REF	
L	0.33	0.43	0.013	0.017

Embossed Carrier Tape & Reel Specification — μDFN-6L



	Millimetres		Inches	
	Min	Max	Min	Max
E	1.65	1.85	0.064	0.073
F	3.45	3.55	0.135	0.139
P2	1.95	2.05	0.076	0.081
D	1.40	1.60	0.055	0.063
D1	0.45	0.55	0.017	0.021
P0	3.90	4.10	0.154	0.161
10P0	40.0+/-0.20		1.574+/-0.008	
W	7.90	8.30	0.311	0.319
P0	3.90	4.10	0.154	0.161
A0	1.15	1.25	0.045	0.049
B0	1.75	1.85	0.069	0.073
K0	0.65	0.75	0.026	0.03
t	0.22 max		0.009 max	