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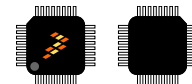
Kinetis K22F Sub-Family Data Sheet

120 MHz ARM® Cortex®-M4-based Microcontroller with FPU

The K22 product family members are optimized for cost-sensitive applications requiring low-power, USB connectivity, processing efficiency with floating point unit. It shares the comprehensive enablement and scalability of the Kinetis family. This product offers:

- Up to 1 MB of flash memory with up to 128 KB of SRAM
- Small package with high memory density
- Run power consumption down to 279 μ A/MHz. Static power consumption down to 5.1 μ A with full state retention and 5 μ s wakeup. Lowest Static mode down to 268 nA
- USB LS/FS OTG 2.0 with embedded 3.3 V, 120 mA LDO voltage regulator

MK22FX512AVLH12
MK22FN1M0AVLH12



64 LQFP
 10 x 10 x 1.4 mm Pitch 0.5 mm

Performance

- Up to 120 MHz ARM Cortex-M4-based core with DSP instructions delivering 1.25 Dhrystone MIPS per MHz

Memories and memory interfaces

- Up to 1 MB program flash memory and 128 KB RAM
- 4 KB FlexRAM and 128 KB FlexNVM on FlexMemory devices
- FlexBus external bus interface

System peripherals

- Multiple low-power modes; low leakage wakeup unit
- Memory protection unit with multi-master protection
- 16-channel DMA controller
- External watchdog monitor and software watchdog

Security and integrity modules

- Hardware CRC module
- 128-bit unique identification (ID) number per chip

Analog modules

- Two 16-bit SAR ADCs
- One 12-bit DAC
- Three analog comparators (CMP)
- Voltage reference

Communication interfaces

- USB full-/low-speed On-the-Go controller
- USB Device Charger detect
- Controller Area Network (CAN) module
- Three SPI modules
- Three I2C modules
- Six UART modules
- Secure Digital host controller (SDHC)
- I2S module

Timers

- Two 8-channel Flex-Timers (PWM/Motor Control)
- Two 2-channel Flex-Timers (PWM/Quad Decoder)
- Periodic interrupt timers and 16-bit low-power timer
- Carrier modulator transmitter
- Real-time clock
- Programmable delay block

Clocks

- 3 to 32 MHz and 32 kHz crystal oscillator
- PLL, FLL, and multiple internal oscillators

Operating Characteristics

- Voltage range: 1.71 to 3.6 V
- Flash write voltage range: 1.71 to 3.6 V
- Temperature range (ambient): -40 to 105°C

Ordering Information ¹

Part Number	Memory		Maximum number of I/O's
	Flash (KB)	SRAM (KB)	
MK22FX512AVLH12	512 KB	128	40
MK22FN1M0AVLH12	1 MB	128	40

1. To confirm current availability of orderable part numbers, go to <http://www.freescale.com> and perform a part number search.

Related Resources

Type	Description	Resource
Selector Guide	The Freescale Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector.	Solution Advisor
Product Brief	The Product Brief contains concise overview/summary information to enable quick evaluation of a device for design suitability.	K20PB ¹
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	K22P64M50SF5V2RM ¹
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	K22P64M50SF5V2 ¹
Package drawing	Package dimensions are provided in package drawings.	• LQFP 64-pin: 98ASS23234W¹

1. To find the associated resource, go to <http://www.freescale.com> and perform a search using this term.

Kinetis K21/22F Family

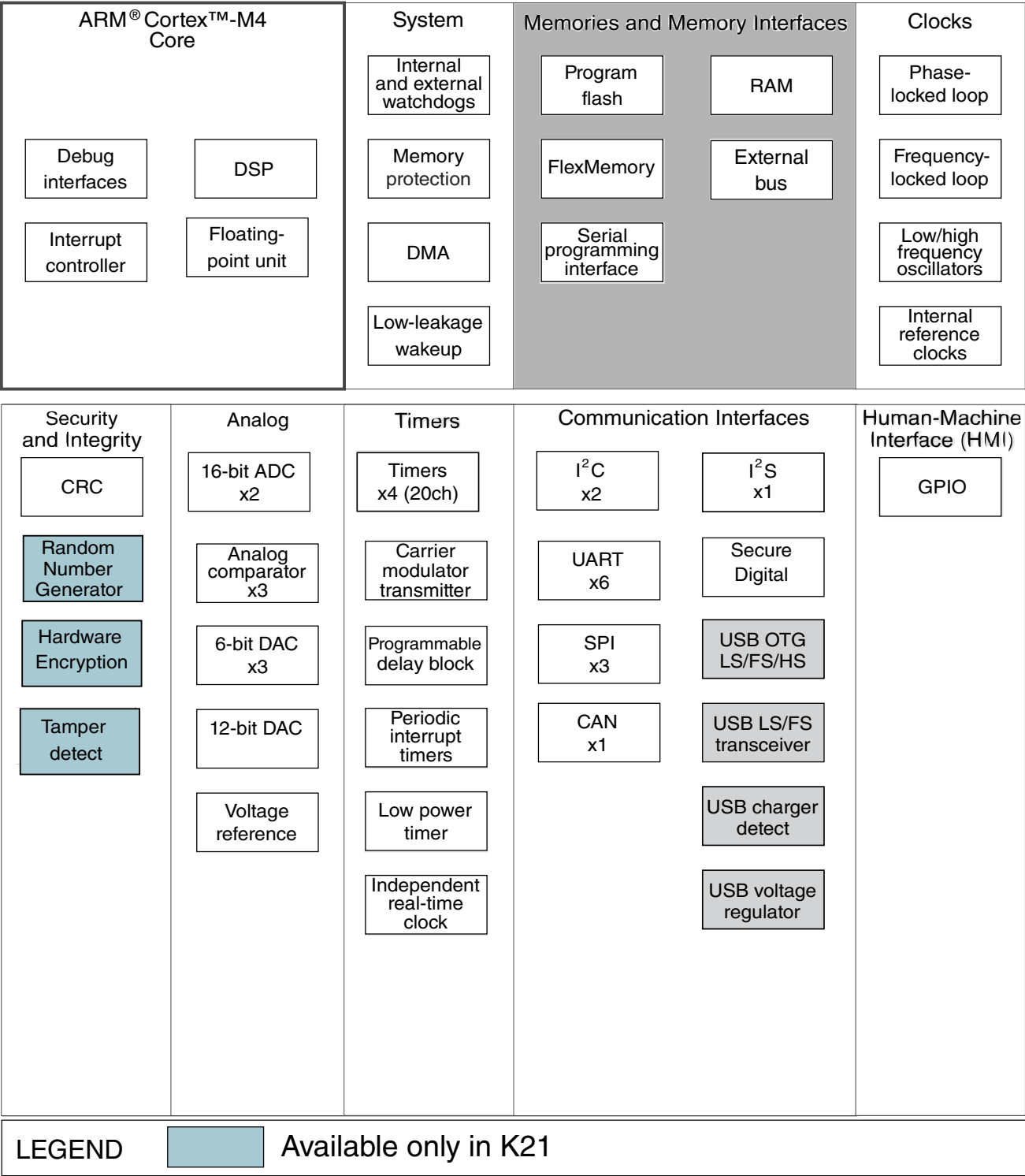


Figure 1. K20 block diagram

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1 Ratings

1.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T _{STG}	Storage temperature	-55	150	°C	1
T _{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V _{HBM}	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V _{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I _{LAT}	Latch-up current at ambient temperature of 105°C	-100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

1.4 Voltage and current operating ratings

General

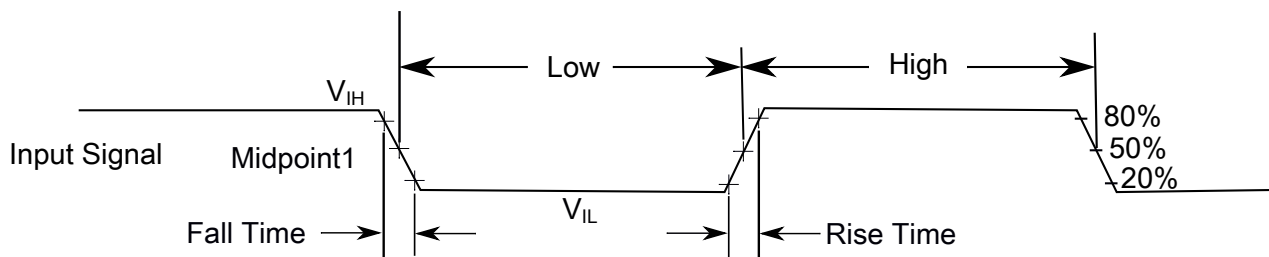
Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	-0.3	3.8	V
I_{DD}	Digital supply current	—	185	mA
V_{DIO}	Digital input voltage (except RESET, EXTAL, and XTAL)	-0.3	5.5	V
V_{AIO}	Analog ¹ , RESET, EXTAL, and XTAL input voltage	-0.3	$V_{DD} + 0.3$	V
I_D	Maximum current single pin limit (applies to all digital pins)	-25	25	mA
V_{DDA}	Analog supply voltage	$V_{DD} - 0.3$	$V_{DD} + 0.3$	V
V_{USB0_DP}	USB0_DP input voltage	-0.3	3.63	V
V_{USB0_DM}	USB0_DM input voltage	-0.3	3.63	V
V_{BAT}	RTC battery supply voltage	-0.3	3.8	V

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

2 General

2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is $V_{IL} + (V_{IH} - V_{IL}) / 2$

Figure 2. Input signal measurement reference

All digital I/O switching characteristics assume:

1. output pins
 - have $C_L=30\text{pF}$ loads,
 - are configured for fast slew rate ($\text{PORTx_PCRn}[\text{SRE}]=0$), and
 - are configured for high drive strength ($\text{PORTx_PCRn}[\text{DSE}]=1$)
2. input pins
 - have their passive filter disabled ($\text{PORTx_PCRn}[\text{PFE}]=0$)

2.2 Nonswitching electrical specifications

2.2.1 Voltage and current operating requirements

Table 1. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	3.6	V	
V_{DDA}	Analog supply voltage	1.71	3.6	V	
$V_{DD} - V_{DDA}$	V_{DD} -to- V_{DDA} differential voltage	-0.1	0.1	V	
$V_{SS} - V_{SSA}$	V_{SS} -to- V_{SSA} differential voltage	-0.1	0.1	V	
V_{BAT}	RTC battery supply voltage	1.71	3.6	V	
V_{IH}	Input high voltage $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$	$0.7 \times V_{DD}$ $0.75 \times V_{DD}$	— —	V V	
V_{IL}	Input low voltage $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$	— —	$0.35 \times V_{DD}$ $0.3 \times V_{DD}$	V V	
V_{HYS}	Input hysteresis	$0.06 \times V_{DD}$	—	V	
I_{ICDIO}	Digital pin negative DC injection current — single pin $V_{IN} < V_{SS}-0.3\text{V}$	-5	—	mA	1
I_{ICAIO}	Analog ² , EXTAL, and XTAL pin DC injection current — single pin $V_{IN} < V_{SS}-0.3\text{V}$ (Negative current injection) $V_{IN} > V_{DD}+0.3\text{V}$ (Positive current injection)	-5 —	— +5	mA	3
I_{ICcont}	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins - Negative current injection - Positive current injection	-25 —	— +25	mA	
V_{ODPU}	Open drain pullup voltage level	V_{DD}	V_{DD}	V	4
V_{RAM}	V_{DD} voltage required to retain RAM	1.2	—	V	
V_{RFVBAT}	V_{BAT} voltage required to retain the VBAT register file	V_{POR_VBAT}	—	V	

- All 5 V tolerant digital I/O pins are internally clamped to V_{SS} through an ESD protection diode. There is no diode connection to V_{DD} . If V_{IN} is less than V_{DIO_MIN} , a current limiting resistor is required. If V_{IN} greater than V_{DIO_MIN} ($=V_{SS}-0.3\text{V}$) is observed, then there is no need to provide current limiting resistors at the pads. The negative DC injection current limiting resistor is calculated as $R=(V_{DIO_MIN}-V_{IN})/|I_{ICDIO}|$.
- Analog pins are defined as pins that do not have an associated general purpose I/O port function. Additionally, EXTAL and XTAL are analog pins.

General

- All analog pins are internally clamped to V_{SS} and V_{DD} through ESD protection diodes. If V_{IN} is less than V_{AIO_MIN} or greater than V_{AIO_MAX} , a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R=(V_{AIO_MIN}-V_{IN})/|I_{ICAIOL}|$. The positive injection current limiting resistor is calculated as $R=(V_{IN}-V_{AIO_MAX})/I_{ICAIOL}$. Select the larger of these two calculated resistances if the pin is exposed to positive and negative injection currents.
- Open drain outputs must be pulled to V_{DD} .

2.2.2 LVD and POR operating requirements

Table 2. V_{DD} supply LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Falling V_{DD} POR detect voltage	0.8	1.1	1.5	V	
V_{LVDH}	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
V_{LVW1H}	Low-voltage warning thresholds — high range					1
	• Level 1 falling (LVWV=00)	2.62	2.70	2.78	V	
V_{LVW2H}	• Level 2 falling (LVWV=01)	2.72	2.80	2.88	V	
V_{LVW3H}	• Level 3 falling (LVWV=10)	2.82	2.90	2.98	V	
V_{LVW4H}	• Level 4 falling (LVWV=11)	2.92	3.00	3.08	V	
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	80	—	mV	
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
V_{LVW1L}	Low-voltage warning thresholds — low range					1
	• Level 1 falling (LVWV=00)	1.74	1.80	1.86	V	
V_{LVW2L}	• Level 2 falling (LVWV=01)	1.84	1.90	1.96	V	
V_{LVW3L}	• Level 3 falling (LVWV=10)	1.94	2.00	2.06	V	
V_{LVW4L}	• Level 4 falling (LVWV=11)	2.04	2.10	2.16	V	
V_{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	60	—	mV	
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	
t_{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	μs	

- Rising threshold is the sum of falling threshold and hysteresis voltage

Table 3. VBAT power operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR_VBAT}	Falling VBAT supply POR detect voltage	0.8	1.1	1.5	V	

2.2.3 Voltage and current operating behaviors

Table 4. Voltage and current operating behaviors

Symbol	Description	Min.	Typ	Max.	Unit	Notes
V_{OH}	Output high voltage — high drive strength					
	• $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OH} = -8\text{mA}$	$V_{DD} - 0.5$	—	—	V	
	• $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OH} = -3\text{mA}$	$V_{DD} - 0.5$	—	—	V	
	Output high voltage — low drive strength					
	• $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OH} = -2\text{mA}$	$V_{DD} - 0.5$	—	—	V	
	• $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OH} = -0.6\text{mA}$	$V_{DD} - 0.5$	—	—	V	
I_{OHT}	Output high current total for all ports	—	—	100	mA	
V_{OL}	Output low voltage — high drive strength					1
	• $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OL} = 9\text{mA}$	—	—	0.5	V	
	• $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OL} = 3\text{mA}$	—	—	0.5	V	
	Output low voltage — low drive strength					
	• $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OL} = 2\text{mA}$	—	—	0.5	V	
	• $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OL} = 0.6\text{mA}$	—	—	0.5	V	
I_{OLT}	Output low current total for all ports	—	—	100	mA	
I_{IND}	Input leakage current, digital pins					2, 3
	• $V_{SS} \leq V_{IN} \leq V_{IL}$					
	• All digital pins	—	0.002	0.5	μA	
	• $V_{IN} = V_{DD}$					
	• All digital pins except PTD7	—	0.002	0.5	μA	
	• PTD7	—	0.004	1	μA	
I_{IND}	Input leakage current, digital pins					2
	• $V_{IL} < V_{IN} < V_{DD}$					
	• $V_{DD} = 3.6\text{ V}$	—	18	26	μA	
	• $V_{DD} = 3.0\text{ V}$	—	12	19	μA	
	• $V_{DD} = 2.5\text{ V}$	—	8	13	μA	
	• $V_{DD} = 1.7\text{ V}$	—	3	6	μA	
I_{IND}	Input leakage current, digital pins					
	• $V_{DD} < V_{IN} < 5.5\text{ V}$	—	1	50	μA	
I_{OZ}	Hi-Z (off-state) leakage current (per pin)	—	—	0.25	μA	
R_{PU}	Internal pullup resistors	20	35	50	$\text{k}\Omega$	4
R_{PD}	Internal pulldown resistors	20	35	50	$\text{k}\Omega$	5

1. Open drain outputs must be pulled to V_{DD} .
2. Measured at $V_{DD}=3.6\text{V}$
3. Internal pull-up/pull-down resistors disabled.
4. Measured at V_{DD} supply voltage = V_{DD} min and $V_{input} = V_{SS}$

General

5. Measured at V_{DD} supply voltage = V_{DD} min and $V_{input} = V_{DD}$

2.2.4 Power mode transition operating behaviors

All specifications except t_{POR} , and $VLLSx \rightarrow RUN$ recovery times in the following table assume this clock configuration:

- CPU and system clocks = 100 MHz
- Bus clock = 50 MHz
- FlexBus clock = 50 MHz
- Flash clock = 25 MHz

Table 5. Power mode transition operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip.	—	300	μs	
	• $VLLS0 \rightarrow RUN$	—	183	μs	
	• $VLLS1 \rightarrow RUN$	—	183	μs	
	• $VLLS2 \rightarrow RUN$	—	105	μs	
	• $VLLS3 \rightarrow RUN$	—	105	μs	
	• $LLS \rightarrow RUN$	—	5.0	μs	
	• $VLPS \rightarrow RUN$	—	4.4	μs	
	• $STOP \rightarrow RUN$	—	4.4	μs	

2.2.5 Power consumption operating behaviors

Table 6. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA}	Analog supply current	—	—	See note	mA	1
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash	—	33.57	36.2	mA	2
		—	33.51	36.1	mA	
		—	33.51	36.1	mA	

Table continues on the next page...

General

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	@ 1.8V @ 3.0V					
I _{DD_RUN}	Run mode current — all peripheral clocks enabled, code executing from flash @ 1.8V @ 3.0V @ 25°C @ 125°C	—	46.36	50.1	mA	3, 4
I _{DD_WAIT}	Wait mode high frequency current at 3.0 V — all peripheral clocks disabled	—	18.2	—	mA	2
I _{DD_WAIT}	Wait mode reduced frequency current at 3.0 V — all peripheral clocks disabled	—	7.2	—	mA	5
I _{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled	—	1.21	—	mA	6
I _{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled	—	1.88	—	mA	7
I _{DD_VLPW}	Very-low-power wait mode current at 3.0 V — all peripheral clocks disabled	—	0.80	—	mA	8
I _{DD_STOP}	Stop mode current at 3.0 V @ -40 to 25°C @ 70°C @ 105°C	—	0.528	2.25	mA	
		—	1.6	8	mA	
		—	5.2	20	mA	
I _{DD_VLPS}	Very-low-power stop mode current at 3.0 V @ -40 to 25°C @ 70°C @ 105°C	—	78	700	μA	
		—	498	2400	μA	
		—	1300	3600	μA	
I _{DD_LLS}	Low leakage stop mode current at 3.0 V @ -40 to 25°C @ 70°C @ 105°C	—	5.1	15	μA	
		—	28	80	μA	
		—	124	300	μA	
I _{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V @ -40 to 25°C @ 70°C @ 105°C	—	3.1	7.5	μA	
		—	14.5	45	μA	
		—	63.5	195	μA	
I _{DD_VLLS2}	Very low-leakage stop mode 2 current at 3.0 V @ -40 to 25°C	—	2.0	5	μA	
		—	6.9	32	μA	

Table continues on the next page...

General

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	@ 70°C @ 105°C	—	30	112	μA	
I _{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V @ -40 to 25°C @ 70°C @ 105°C	—	1.25	2.1	μA	
		—	6.5	18.5	μA	
		—	37	108	μA	
I _{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit enabled @ -40 to 25°C @ 70°C @ 105°C	—	0.745	1.65	μA	
		—	6.03	18	μA	
		—	37	108	μA	
I _{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit disabled @ -40 to 25°C @ 70°C @ 105°C	—	0.268	1.25	μA	
		—	3.7	15	μA	
		—	22.9	95	μA	
I _{DD_VBAT}	Average current with RTC and 32kHz disabled at 3.0 V @ -40 to 25°C @ 70°C @ 105°C	—	0.19	0.22	μA	
		—	0.49	0.64	μA	
		—	2.2	3.2	μA	
I _{DD_VBAT}	Average current when CPU is not accessing RTC registers @ 1.8V @ -40 to 25°C @ 70°C @ 105°C @ 3.0V @ -40 to 25°C @ 70°C @ 105°C	—	0.68	0.8	μA	9
		—	1.2	1.56	μA	
		—	3.6	5.3	μA	
		—	0.81	0.96	μA	
		—	1.45	1.89	μA	
		—	4.3	6.33	μA	

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. 120 MHz core and system clock, 60 MHz bus 40 Mhz and FlexBus clock, and 24 MHz flash clock. MCG configured for PEE mode. All peripheral clocks disabled.
3. 120 MHz core and system clock, 60 MHz bus and FlexBus clock, and 24 MHz flash clock. MCG configured for PEE mode. All peripheral clocks enabled.
4. Max values are measured with CPU executing DSP instructions.

General

5. 25 MHz core and system clock, 25 MHz bus clock, and 12.5 MHz FlexBus and flash clock. MCG configured for FEI mode.
6. 4 MHz core, system, FlexBus, and bus clock and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing from flash.
7. 4 MHz core, system, FlexBus, and bus clock and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks enabled but peripherals are not in active operation. Code executing from flash.
8. 4 MHz core, system, FlexBus, and bus clock and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled.
9. Includes 32kHz oscillator current and RTC operation.

2.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in PEE mode at greater than 100 MHz frequencies
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFE

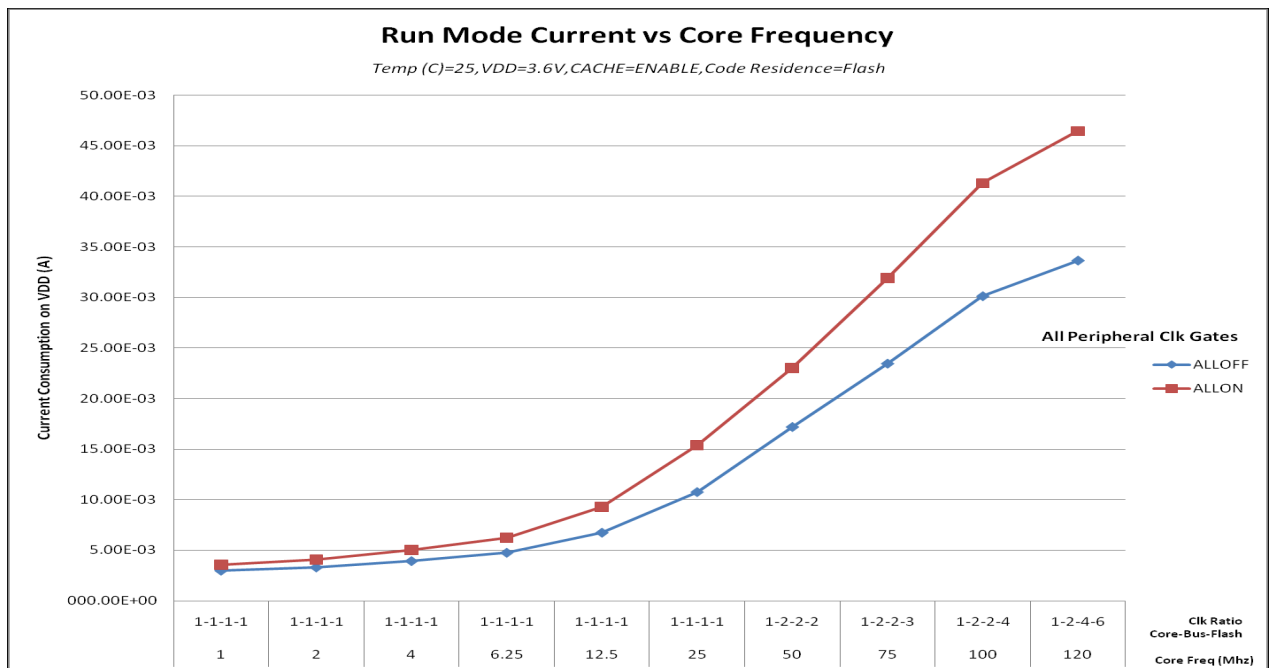


Figure 3. Run mode supply current vs. core frequency

General

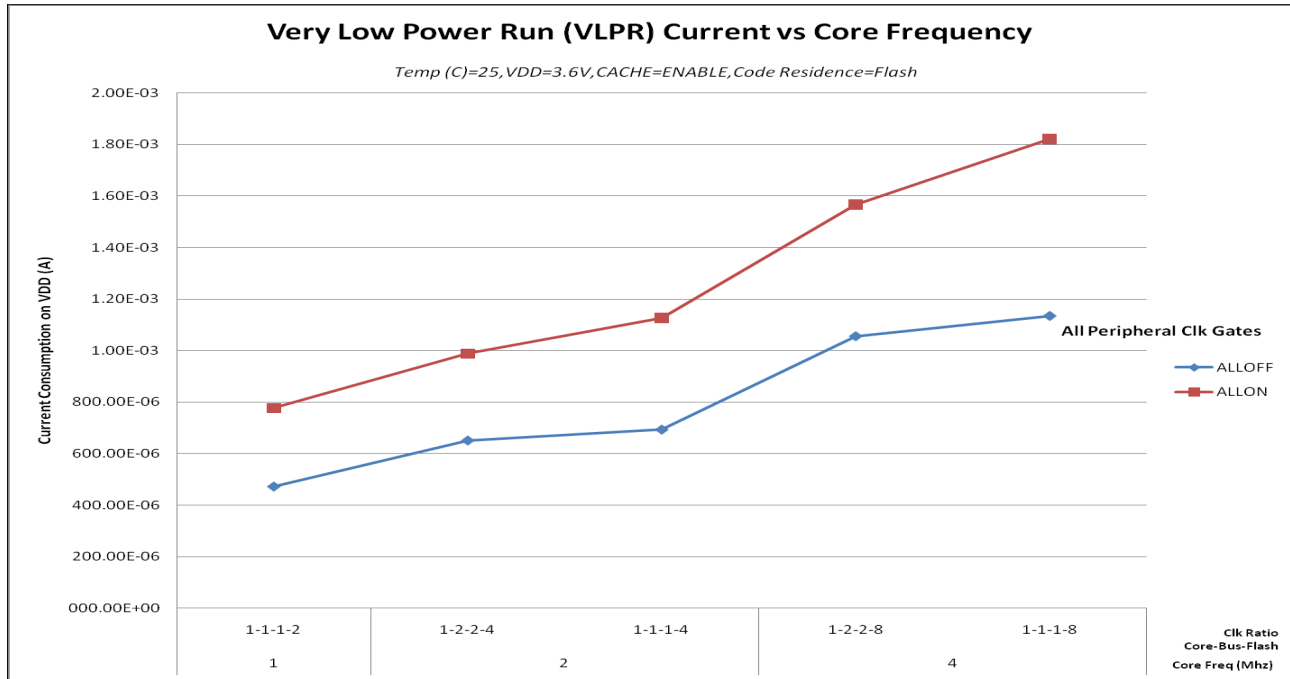


Figure 4. VLPR mode supply current vs. core frequency

2.2.6 EMC radiated emissions operating behaviors

Table 7. EMC radiated emissions operating behaviors

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V _{RE1}	Radiated emissions voltage, band 1	0.15–50	23	dBμV	1, 2
V _{RE2}	Radiated emissions voltage, band 2	50–150	27	dBμV	
V _{RE3}	Radiated emissions voltage, band 3	150–500	28	dBμV	
V _{RE4}	Radiated emissions voltage, band 4	500–1000	14	dBμV	
V _{RE_IEC}	IEC level	0.15–1000	K	—	2, 3

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic application code.

General

The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.

2. $V_{DD} = 3.3\text{ V}$, $T_A = 25\text{ }^{\circ}\text{C}$, $f_{OSC} = 12\text{ MHz}$ (crystal), $f_{SYS} = 96\text{ MHz}$, $f_{BUS} = 48\text{ MHz}$
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

2.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for “EMC design.”

2.2.8 Capacitance attributes

Table 8. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

2.3 Switching specifications

2.3.1 Device clock specifications

Table 9. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
f_{SYS}	System and core clock	—	120	MHz	
f_{SYS_USB}	System and core clock when Full Speed USB in operation	20	—	MHz	
f_{BUS}	Bus clock	—	60	MHz	
FB_CLK	FlexBus clock	—	50	MHz	
f_{FLASH}	Flash clock	—	25	MHz	
f_{LPTMR}	LPTMR clock	—	25	MHz	
VLPR mode ¹					
f_{SYS}	System and core clock	—	4	MHz	
f_{BUS}	Bus clock	—	4	MHz	

Table continues on the next page...

General

Table 9. Device clock specifications (continued)

Symbol	Description	Min.	Max.	Unit	Notes
FB_CLK	FlexBus clock	—	4	MHz	
f _{FLASH}	Flash clock	—	0.8	MHz	
f _{ERCLK}	External reference clock	—	16	MHz	
f _{LPTMR_pin}	LPTMR clock	—	25	MHz	
f _{LPTMR_ERCLK}	LPTMR external reference clock	—	16	MHz	
f _{FlexCAN_ERCLK}	FlexCAN external reference clock	—	8	MHz	
f _{I2S_MCLK}	I2S master clock	—	12.5	MHz	
f _{I2S_BCLK}	I2S bit clock	—	4	MHz	

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

2.3.2 General switching specifications

These general purpose specifications apply to all pins configured for:

- GPIO signaling
- Other peripheral module signaling not explicitly stated elsewhere

Table 10. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1, 2
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter enabled) — Asynchronous path	100	—	ns	3
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) — Asynchronous path	16	—	ns	3
	External reset pulse width (digital glitch filter disabled)	100	—	ns	3
	Mode select (EZP_CS) hold time after reset deassertion	2	—	Bus clock cycles	
	Port rise and fall time (high drive strength) • Slew disabled • $1.71 \leq V_{DD} \leq 2.7V$ • $2.7 \leq V_{DD} \leq 3.6V$ • Slew enabled • $1.71 \leq V_{DD} \leq 2.7V$ • $2.7 \leq V_{DD} \leq 3.6V$	— — — —	12 6 36 24	ns ns ns ns	4
	Port rise and fall time (low drive strength) • Slew disabled				5

General

Table 10. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	$1.71 \leq V_{DD} \leq 2.7V$ $2.7 \leq V_{DD} \leq 3.6V$ - Slew enabled	—	12	ns	
	$1.71 \leq V_{DD} \leq 2.7V$ $2.7 \leq V_{DD} \leq 3.6V$	—	6	ns	
	$1.71 \leq V_{DD} \leq 2.7V$ $2.7 \leq V_{DD} \leq 3.6V$	—	36	ns	
	$1.71 \leq V_{DD} \leq 2.7V$ $2.7 \leq V_{DD} \leq 3.6V$	—	24	ns	

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop, VLPS, LLS, and VLLSx modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
2. The greater synchronous and asynchronous timing must be met.
3. This is the minimum pulse width that is guaranteed to be recognized as a pin interrupt request in Stop, VLPS, LLS, and VLLSx modes.
4. 75 pF load
5. 15 pF load

2.4 Thermal specifications

2.4.1 Thermal operating requirements

Table 11. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T_J	Die junction temperature	−40	125	°C
T_A	Ambient temperature	−40	105	°C

2.4.2 Thermal attributes

Board type	Symbol	Description	64 LQFP	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	59	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	41	°C/W	1

Table continues on the next page...

Peripheral operating requirements and behaviors

Board type	Symbol	Description	64 LQFP	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	48	°C/W	¹
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	35	°C/W	¹
—	$R_{\theta JB}$	Thermal resistance, junction to board	23	°C/W	²
—	$R_{\theta JC}$	Thermal resistance, junction to case	11	°C/W	³
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	3	°C/W	⁴

Notes

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

3 Peripheral operating requirements and behaviors

3.1 Core modules

3.1.1 Debug trace timing specifications

Table 12. Debug trace operating behaviors

Symbol	Description	Min.	Max.	Unit
T_{cyc}	Clock period	Frequency dependent (limited to 50 MHz)		MHz
T_{wl}	Low pulse width	2	—	ns
T_{wh}	High pulse width	2	—	ns
T_r	Clock and data rise time	—	3	ns
T_f	Clock and data fall time	—	3	ns
T_s	Data setup	3	—	ns
T_h	Data hold	2	—	ns

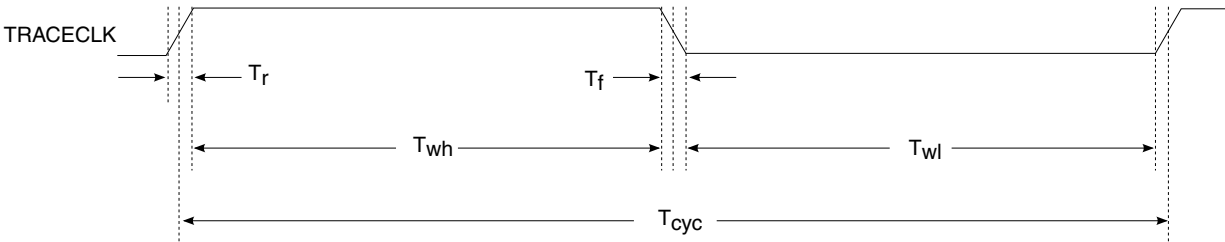


Figure 5. TRACE_CLKOUT specifications

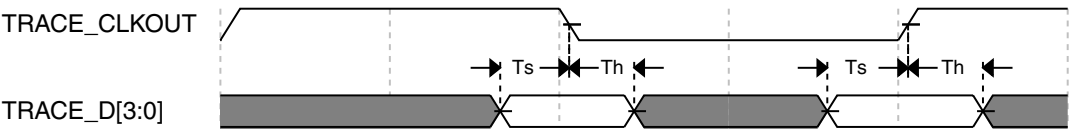


Figure 6. Trace data specifications

3.1.2 JTAG electricals

Table 13. JTAG limited voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
J1	TCLK frequency of operation			MHz

Table continues on the next page...

Peripheral operating requirements and behaviors

Table 13. JTAG limited voltage range electricals (continued)

Symbol	Description	Min.	Max.	Unit
	- Boundary Scan - JTAG and CJTAG - Serial Wire Debug	0	10	
		0	25	
		0	50	
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width			
	Boundary Scan	50	—	ns
	JTAG and CJTAG	20	—	ns
	Serial Wire Debug	10	—	ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	2.6	—	ns
J7	TCLK low to boundary scan output data valid	—	25	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1	—	ns
J11	TCLK low to TDO data valid	—	17	ns
J12	TCLK low to TDO high-Z	—	17	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

Table 14. JTAG full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	TCLK frequency of operation			MHz
	Boundary Scan	0	10	
	JTAG and CJTAG	0	20	
	Serial Wire Debug	0	40	
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width			
	Boundary Scan	50	—	ns
	JTAG and CJTAG	25	—	ns
	Serial Wire Debug	12.5	—	ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	0	—	ns

Table continues on the next page...

Peripheral operating requirements and behaviors

Table 14. JTAG full voltage range electricals (continued)

Symbol	Description	Min.	Max.	Unit
J7	TCLK low to boundary scan output data valid	—	25	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1.4	—	ns
J11	TCLK low to TDO data valid	—	22.1	ns
J12	TCLK low to TDO high-Z	—	22.1	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

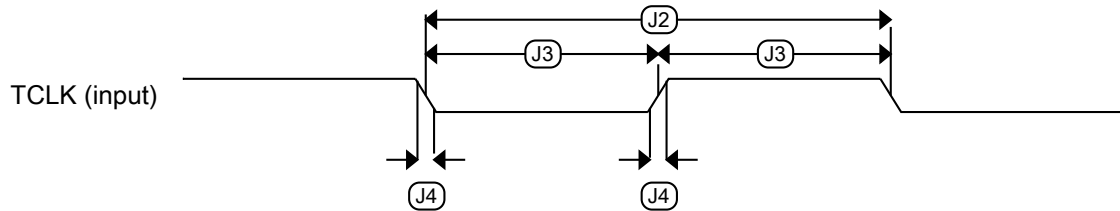


Figure 7. Test clock input timing

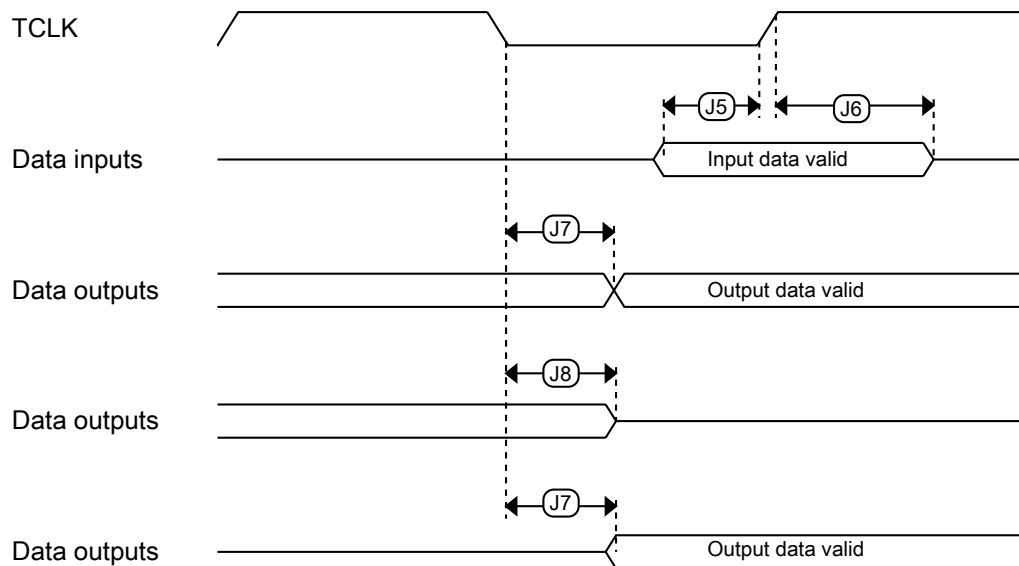


Figure 8. Boundary scan (JTAG) timing

Peripheral operating requirements and behaviors

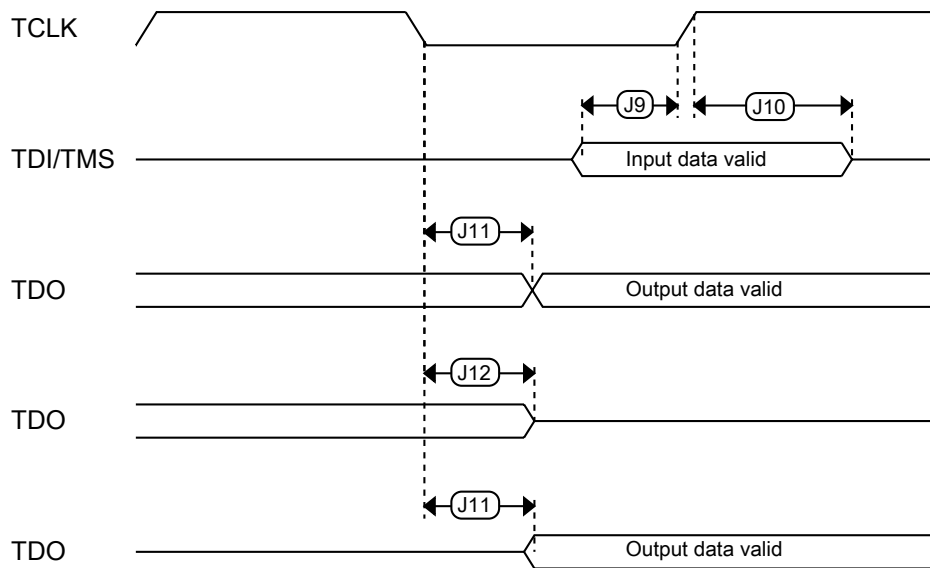


Figure 9. Test Access Port timing

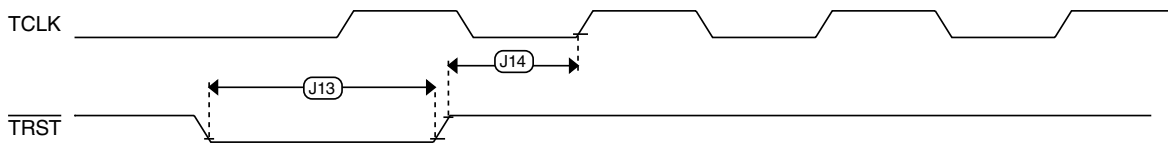


Figure 10. TRST timing

3.2 System modules

There are no specifications necessary for the device's system modules.

3.3 Clock modules

Peripheral operating requirements and behaviors

3.3.1 MCG specifications

Table 15. MCG specifications

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
f _{ints_ft}	Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C		—	32.768	—	kHz	
f _{ints_t}	Internal reference frequency (slow clock) — user trimmed		31.25	—	39.0625	kHz	
I _{ints}	Internal reference (slow clock) current		—	20	—	μA	
Δf _{dco_res_t}	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM		—	± 0.3	± 0.6	%f _{dco}	1
Δf _{dco_res_t}	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM only		—	± 0.2	± 0.5	%f _{dco}	1
Δf _{dco_t}	Total deviation of trimmed average DCO output frequency over voltage and temperature		—	± 0.5	± 2	%f _{dco}	1, 2
Δf _{dco_t}	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C		—	± 0.3	± 1	%f _{dco}	1
f _{intf_ft}	Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C		—	4	—	MHz	
f _{intf_t}	Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C		3	—	5	MHz	
I _{intf}	Internal reference (fast clock) current		—	25	—	μA	
f _{loc_low}	Loss of external clock minimum frequency — RANGE = 00		(3/5) x f _{ints_t}	—	—	kHz	
f _{loc_high}	Loss of external clock minimum frequency — RANGE = 01, 10, or 11		(16/5) x f _{ints_t}	—	—	kHz	
FLL							
f _{fill_ref}	FLL reference frequency range		31.25	—	39.0625	kHz	
f _{dco}	DCO output frequency range	Low range (DRS=00) 640 × f _{fill_ref}	20	20.97	25	MHz	3, 4
		Mid range (DRS=01) 1280 × f _{fill_ref}	40	41.94	50	MHz	
		Mid-high range (DRS=10) 1920 × f _{fill_ref}	60	62.91	75	MHz	
		High range (DRS=11) 2560 × f _{fill_ref}	80	83.89	100	MHz	
f _{dco_t_DMx3_2}	DCO output frequency	Low range (DRS=00) 732 × f _{fill_ref}	—	23.99	—	MHz	5, 6
		Mid range (DRS=01) 1464 × f _{fill_ref}	—	47.97	—	MHz	
		Mid-high range (DRS=10)	—	71.99	—	MHz	

Table continues on the next page...

Peripheral operating requirements and behaviors

Table 15. MCG specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
		$2197 \times f_{\text{fll_ref}}$				
		High range (DRS=11)	—	95.98	—	MHz
		$2929 \times f_{\text{fll_ref}}$				
$J_{\text{cyc_fll}}$	FLL period jitter $f_{\text{DCO}} = 48 \text{ MHz}$ $f_{\text{DCO}} = 98 \text{ MHz}$	—	180	—	ps	
$t_{\text{fll_acquire}}$	FLL target frequency acquisition time	—	—	1	ms	7
PLL						
f_{vco}	VCO operating frequency	48.0	—	120	MHz	
I_{pll}	PLL operating current PLL @ 96 MHz ($f_{\text{osc_hi_1}} = 8 \text{ MHz}$, $f_{\text{pll_ref}} = 2 \text{ MHz}$, VDIV multiplier = 48)	—	1060	—	μA	8
I_{pll}	PLL operating current PLL @ 48 MHz ($f_{\text{osc_hi_1}} = 8 \text{ MHz}$, $f_{\text{pll_ref}} = 2 \text{ MHz}$, VDIV multiplier = 24)	—	600	—	μA	8
$f_{\text{pll_ref}}$	PLL reference frequency range	2.0	—	4.0	MHz	
$J_{\text{cyc_pll}}$	PLL period jitter (RMS) $f_{\text{vco}} = 48 \text{ MHz}$ $f_{\text{vco}} = 120 \text{ MHz}$	—	120	—	ps	9
$J_{\text{acc_pll}}$	PLL accumulated jitter over 1μs (RMS) $f_{\text{vco}} = 48 \text{ MHz}$ $f_{\text{vco}} = 120 \text{ MHz}$	—	1350	—	ps	9
		—	600	—	ps	
D_{lock}	Lock entry frequency tolerance	± 1.49	—	± 2.98	%	
D_{unl}	Lock exit frequency tolerance	± 4.47	—	± 5.97	%	
$t_{\text{pll_lock}}$	Lock detector detection time	—	—	$150 \times 10^{-6} + 1075(1/f_{\text{pll_ref}})$	s	10

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. $2 \text{ V} \leq V_{\text{DD}} \leq 3.6 \text{ V}$.
3. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
4. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation ($\Delta f_{\text{dco_t}}$) over voltage and temperature should be considered.
5. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
6. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
7. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
8. Excludes any oscillator currents that are also consuming power while PLL is in operation.
9. This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
10. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

3.3.2 Oscillator electrical specifications

3.3.2.1 Oscillator DC electrical specifications

Table 16. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	
I_{DDOSC}	Supply current — low-power mode (HGO=0)					1
	• 32 kHz	—	600	—	nA	
	• 4 MHz	—	200	—	μ A	
	• 8 MHz (RANGE=01)	—	300	—	μ A	
	• 16 MHz	—	950	—	μ A	
	• 24 MHz	—	1.2	—	mA	
	• 32 MHz	—	1.5	—	mA	
I_{DDOSC}	Supply current — high gain mode (HGO=1)					1
	• 32 kHz	—	7.5	—	μ A	
	• 4 MHz	—	500	—	μ A	
	• 8 MHz (RANGE=01)	—	650	—	μ A	
	• 16 MHz	—	2.5	—	mA	
	• 24 MHz	—	3.25	—	mA	
	• 32 MHz	—	4	—	mA	
C_x	EXTAL load capacitance	—	—	—		2, 3
C_y	XTAL load capacitance	—	—	—		2, 3
R_F	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	M Ω	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	M Ω	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	M Ω	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	M Ω	
R_S	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	k Ω	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	k Ω	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	k Ω	
	Series resistor — high-frequency, high-gain mode (HGO=1)					

Table continues on the next page...

Peripheral operating requirements and behaviors

Table 16. Oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
		—	0	—	kΩ	
V_{pp}^5	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	

1. V_{DD} =3.3 V, Temperature =25 °C, Internal capacitance = 20 pF
2. See crystal or resonator manufacturer's recommendation
3. C_x, C_y can be provided by using either the integrated capacitors or by using external components.
4. When low power mode is selected, R_F is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

3.3.2.2 Oscillator frequency specifications

Table 17. Oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal or resonator frequency — low-frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
$f_{osc_hi_1}$	Oscillator crystal or resonator frequency — high-frequency mode (low range) (MCG_C2[RANGE]=01)	3	—	8	MHz	
$f_{osc_hi_2}$	Oscillator crystal or resonator frequency — high-frequency mode (high range) (MCG_C2[RANGE]=1x)	8	—	32	MHz	
f_{ec_extal}	Input clock frequency (external clock mode)	—	—	50	MHz	1, 2
t_{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t_{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—	750	—	ms	3, 4
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—	250	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	—	0.6	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	—	1	—	ms	

1. Other frequency limits may apply when external clock is being used as a reference for the FLL or PLL.

Peripheral operating requirements and behaviors

- When transitioning from FEI or FBI to FBE mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
- Proper PC board layout procedures must be followed to achieve specifications.
- Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

NOTE

The 32 kHz oscillator works in low power mode by default and cannot be moved into high power/gain mode.

3.3.3 32 kHz oscillator electrical characteristics

3.3.3.1 32 kHz oscillator DC electrical specifications

Table 18. 32kHz oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{BAT}	Supply voltage	1.71	—	3.6	V
R_F	Internal feedback resistor	—	100	—	$M\Omega$
C_{para}	Parasitical capacitance of EXTAL32 and XTAL32	—	5	7	pF
V_{pp}^1	Peak-to-peak amplitude of oscillation	—	0.6	—	V

- When a crystal is being used with the 32 kHz oscillator, the EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

3.3.3.2 32 kHz oscillator frequency specifications

Table 19. 32 kHz oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal	—	32.768	—	kHz	
t_{start}	Crystal start-up time	—	1000	—	ms	1
$V_{ec_extal32}$	Externally provided input clock amplitude	700	—	V_{BAT}	mV	2, 3

- Proper PC board layout procedures must be followed to achieve specifications.
- This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.
- The parameter specified is a peak-to-peak value and V_{IH} and V_{IL} specifications do not apply. The voltage of the applied clock must be within the range of V_{SS} to V_{BAT} .

3.4 Memories and memory interfaces

Peripheral operating requirements and behaviors

3.4.1 Flash (FTFE) electrical specifications

This section describes the electrical characteristics of the FTFE module.

3.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 20. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{hvp\text{gm}8}$	Program Phrase high-voltage time	—	7.5	18	μs	
$t_{h\text{versscr}}$	Erase Flash Sector high-voltage time	—	13	113	ms	1
$t_{h\text{versblk}128\text{k}}$	Erase Flash Block high-voltage time for 128 KB	—	104	904	ms	1
$t_{h\text{versblk}512\text{k}}$	Erase Flash Block high-voltage time for 512 KB	—	416	3616	ms	1

1. Maximum time based on expectations at cycling end-of-life.

3.4.1.2 Flash timing specifications — commands

Table 21. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1\text{blk}128\text{k}}$	Read 1s Block execution time • 128 KB data flash	—	—	0.5	ms	
$t_{rd1\text{blk}512\text{k}}$	• 512 KB program flash	—	—	1.8	ms	
$t_{rd1\text{sec}4\text{k}}$	Read 1s Section execution time (4 KB flash)	—	—	100	μs	1
t_{pgmchk}	Program Check execution time	—	—	95	μs	1
$t_{rd\text{rsrc}}$	Read Resource execution time	—	—	40	μs	1
t_{pgm8}	Program Phrase execution time	—	90	150	μs	
$t_{ers\text{blk}128\text{k}}$	Erase Flash Block execution time • 128 KB data flash	—	110	925	ms	2
$t_{ers\text{blk}512\text{k}}$	• 512 KB program flash	—	435	3700	ms	
t_{ersscr}	Erase Flash Sector execution time	—	15	115	ms	2
$t_{pgmsec1\text{k}}$	Program Section execution time (1KB flash)	—	5	—	ms	
$t_{rd1\text{allx}}$	Read 1s All Blocks execution time • FlexNVM devices	—	—	2.2	ms	
t_{rdonce}	Read Once execution time	—	—	30	μs	1
$t_{pgmonce}$	Program Once execution time	—	90	—	μs	
t_{ersall}	Erase All Blocks execution time	—	870	7400	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	μs	1

Table continues on the next page...

Peripheral operating requirements and behaviors

Table 21. Flash command timing specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{swapx01}	Swap Control execution time • control code 0x01	—	200	—	μs	
t_{swapx02}	• control code 0x02	—	90	150	μs	
t_{swapx04}	• control code 0x04	—	90	150	μs	
t_{swapx08}	• control code 0x08	—	—	30	μs	
$t_{\text{pgmpart32k}}$	Program Partition for EEPROM execution time • 32 KB EEPROM backup	—	70	—	ms	
$t_{\text{pgmpart128k}}$	• 128 KB EEPROM backup	—	75	—	ms	
t_{setramff}	Set FlexRAM Function execution time: • Control Code 0xFF	—	70	—	μs	
$t_{\text{setram32k}}$	• 32 KB EEPROM backup	—	0.8	1.2	ms	
$t_{\text{setram64k}}$	• 64 KB EEPROM backup	—	1.3	1.9	ms	
$t_{\text{setram128k}}$	• 128 KB EEPROM backup	—	2.4	3.1	ms	
$t_{\text{eewr8bers}}$	Byte-write to erased FlexRAM location execution time	—	175	275	μs	3
$t_{\text{eewr8b32k}}$	Byte-write to FlexRAM execution time: • 32 KB EEPROM backup	—	385	1700	μs	
$t_{\text{eewr8b64k}}$	• 64 KB EEPROM backup	—	475	2000	μs	
$t_{\text{eewr8b128k}}$	• 128 KB EEPROM backup	—	650	2350	μs	
$t_{\text{eewr16bers}}$	16-bit write to erased FlexRAM location execution time	—	175	275	μs	
$t_{\text{eewr16b32k}}$	16-bit write to FlexRAM execution time: • 32 KB EEPROM backup	—	385	1700	μs	
$t_{\text{eewr16b64k}}$	• 64 KB EEPROM backup	—	475	2000	μs	
$t_{\text{eewr16b128k}}$	• 128 KB EEPROM backup	—	650	2350	μs	
$t_{\text{eewr32bers}}$	32-bit write to erased FlexRAM location execution time	—	360	550	μs	
$t_{\text{eewr32b32k}}$	32-bit write to FlexRAM execution time: • 32 KB EEPROM backup	—	630	2000	μs	
$t_{\text{eewr32b64k}}$	• 64 KB EEPROM backup	—	810	2250	μs	
$t_{\text{eewr32b128k}}$	• 128 KB EEPROM backup	—	1200	2650	μs	

1. Assumes 25MHz or greater flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.
3. For byte-writes to an erased FlexRAM location, the aligned word containing the byte must be erased.

Peripheral operating requirements and behaviors

3.4.1.3 Flash high voltage current behaviors

Table 22. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I _{DD_PGM}	Average current adder during high voltage flash programming operation	—	3.5	7.5	mA
I _{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

3.4.1.4 Reliability specifications

Table 23. NVM reliability specifications

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes
Program Flash						
t _{nvmretp10k}	Data retention after up to 10 K cycles	5	50	—	years	
t _{nvmretp1k}	Data retention after up to 1 K cycles	20	100	—	years	
n _{nvmcycp}	Cycling endurance	10 K	50 K	—	cycles	2
Data Flash						
t _{nvmretd10k}	Data retention after up to 10 K cycles	5	50	—	years	
t _{nvmretd1k}	Data retention after up to 1 K cycles	20	100	—	years	
n _{nvmcycd}	Cycling endurance	10 K	50 K	—	cycles	2
FlexRAM as EEPROM						
t _{nvmretee100}	Data retention up to 100% of write endurance	5	50	—	years	
t _{nvmretee10}	Data retention up to 10% of write endurance	20	100	—	years	
n _{nvmcycee}	Cycling endurance for EEPROM backup	20 K	50 K	—	cycles	2
n _{nvmwree16}	Write endurance	70 K	175 K	—	writes	3
n _{nvmwree128}	• EEPROM backup to FlexRAM ratio = 16	630 K	1.6 M	—	writes	
n _{nvmwree512}	• EEPROM backup to FlexRAM ratio = 128	2.5 M	6.4 M	—	writes	
n _{nvmwree2k}	• EEPROM backup to FlexRAM ratio = 512	10 M	25 M	—	writes	
n _{nvmwree4k}	• EEPROM backup to FlexRAM ratio = 2,048	20 M	50 M	—	writes	
	• EEPROM backup to FlexRAM ratio = 4,096					

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at -40°C ≤ T_j ≤ 125°C.
3. Write endurance represents the number of writes to each FlexRAM location at -40°C ≤ T_j ≤ 125°C influenced by the cycling endurance of the FlexNVM (same value as data flash) and the allocated EEPROM backup per subsystem. Minimum and typical values assume all byte-writes to FlexRAM.

3.4.1.5 Write endurance to FlexRAM for EEPROM

When the FlexNVM partition code is not set to full data flash, the EEPROM data set size can be set to any of several non-zero values.

The bytes not assigned to data flash via the FlexNVM partition code are used by the FTFE to obtain an effective endurance increase for the EEPROM data. The built-in EEPROM record management system raises the number of program/erase cycles that can be attained prior to device wear-out by cycling the EEPROM data through a larger EEPROM NVM storage space.

While different partitions of the FlexNVM are available, the intention is that a single choice for the FlexNVM partition code and EEPROM data set size is used throughout the entire lifetime of a given application. The EEPROM endurance equation and graph shown below assume that only one configuration is ever used.

$$\text{Writes_subsystem} = \frac{\text{EEPROM} - 2 \times \text{EEESPLIT} \times \text{EEESIZE}}{\text{EEESPLIT} \times \text{EEESIZE}} \times \text{Write_efficiency} \times n_{\text{nvmcycee}}$$

where

- Writes_subsystem — minimum number of writes to each FlexRAM location for subsystem (each subsystem can have different endurance)
- EEPROM — allocated FlexNVM for each EEPROM subsystem based on DEPART; entered with the Program Partition command
- EEESPLIT — FlexRAM split factor for subsystem; entered with the Program Partition command
- EEESIZE — allocated FlexRAM based on DEPART; entered with the Program Partition command
- Write_efficiency —
 - 0.25 for 8-bit writes to FlexRAM
 - 0.50 for 16-bit or 32-bit writes to FlexRAM
- n_{nvmcycee} — EEPROM-backup cycling endurance

Peripheral operating requirements and behaviors

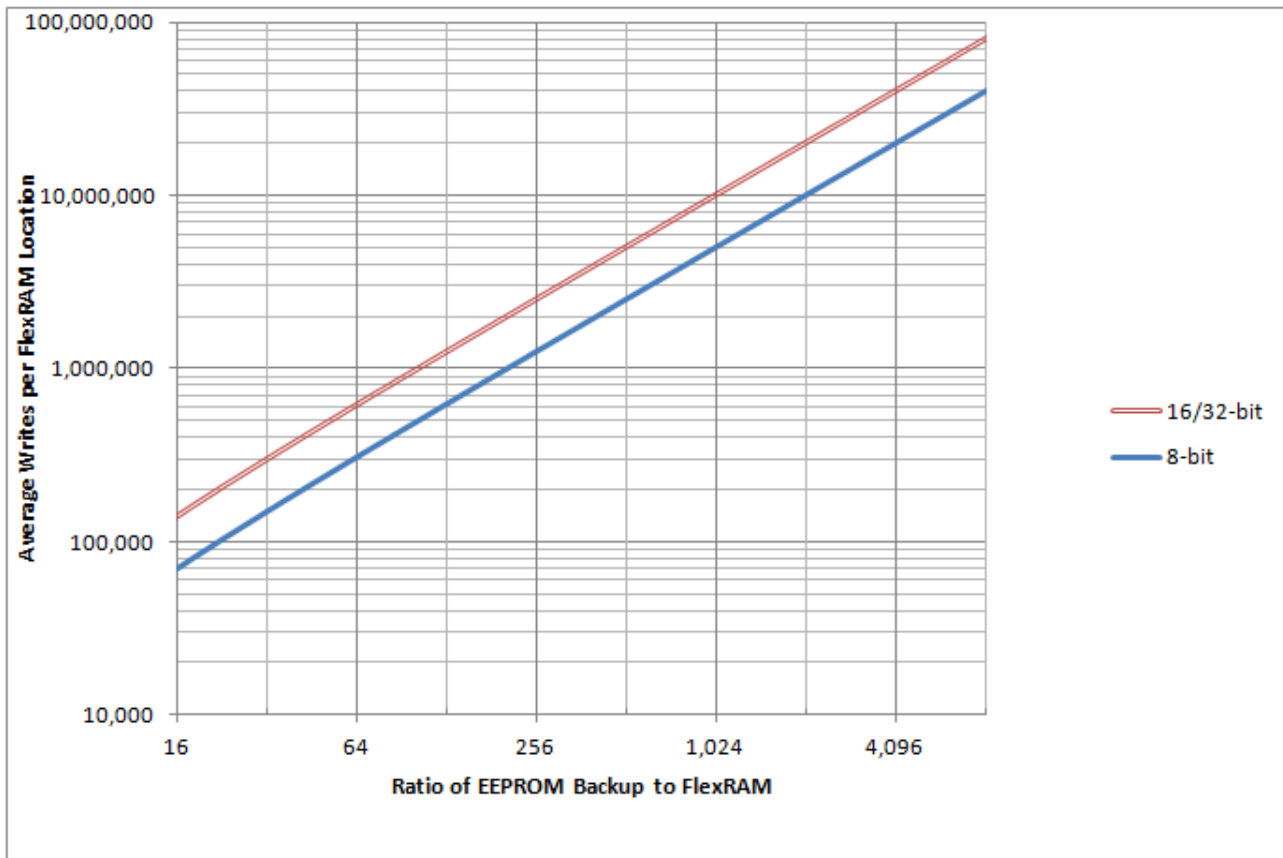


Figure 11. EEPROM backup writes to FlexRAM

3.4.2 EzPort switching specifications

Table 24. EzPort switching specifications

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
EP1	EZP_CK frequency of operation (all commands except READ)	—	$f_{SYS}/2$	MHz
EP1a	EZP_CK frequency of operation (READ command)	—	$f_{SYS}/8$	MHz
EP2	$\overline{EZP_CS}$ negation to next $\overline{EZP_CS}$ assertion	$2 \times t_{EZP_CK}$	—	ns
EP3	$\overline{EZP_CS}$ input valid to EZP_CK high (setup)	5	—	ns
EP4	EZP_CK high to $\overline{EZP_CS}$ input invalid (hold)	5	—	ns
EP5	EZP_D input valid to EZP_CK high (setup)	2	—	ns
EP6	EZP_CK high to EZP_D input invalid (hold)	5	—	ns
EP7	EZP_CK low to EZP_Q output valid	—	18	ns
EP8	EZP_CK low to EZP_Q output invalid (hold)	0	—	ns
EP9	$\overline{EZP_CS}$ negation to EZP_Q tri-state	—	12	ns

Peripheral operating requirements and behaviors

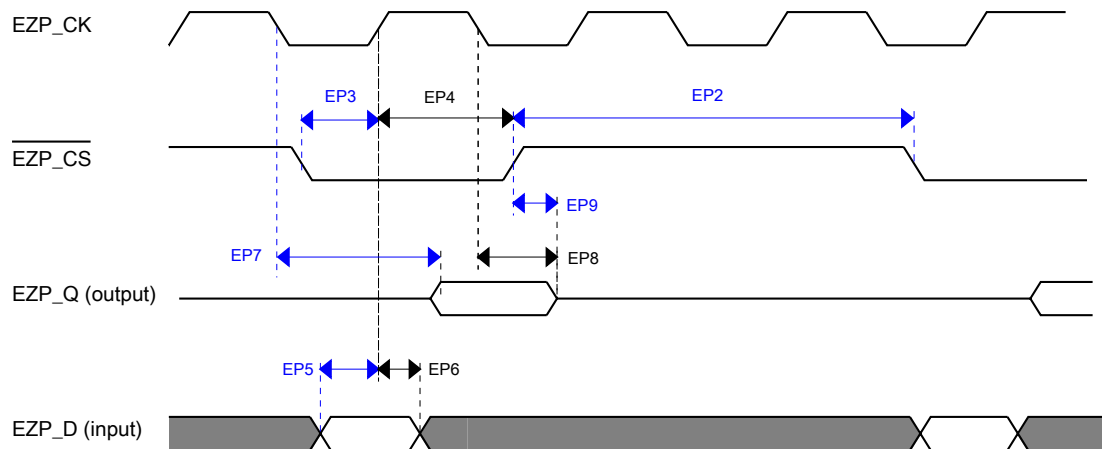


Figure 12. EzPort Timing Diagram

3.4.3 Flexbus switching specifications

All processor bus timings are synchronous; input setup/hold and output delay are given in respect to the rising edge of a reference clock, FB_CLK. The FB_CLK frequency may be the same as the internal system bus frequency or an integer divider of that frequency.

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the Flexbus output clock (FB_CLK). All other timing relationships can be derived from these values.

Table 25. Flexbus limited voltage range switching specifications

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	FB_CLK	MHz	
FB1	Clock period	20	—	ns	
FB2	Address, data, and control output valid	—	11.5	ns	1
FB3	Address, data, and control output hold	0.5	—	ns	1
FB4	Data and $\overline{\text{FB_TA}}$ input setup	8.5	—	ns	2
FB5	Data and $\overline{\text{FB_TA}}$ input hold	0.5	—	ns	2

1. Specification is valid for all FB_AD[31:0], $\overline{\text{FB_BE/BWEn}}$, $\overline{\text{FB_CSn}}$, $\overline{\text{FB_OE}}$, FB_R/W, FB_TBST, FB_TSIZ[1:0], FB_ALE, and FB_TS.

Peripheral operating requirements and behaviors

- Specification is valid for all FB_AD[31:0] and $\overline{\text{FB_TA}}$.

Table 26. Flexbus full voltage range switching specifications

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	
	Frequency of operation	—	FB_CLK	MHz	
FB1	Clock period	1/FB_CLK	—	ns	
FB2	Address, data, and control output valid	—	13.5	ns	1
FB3	Address, data, and control output hold	0	—	ns	1
FB4	Data and $\overline{\text{FB_TA}}$ input setup	13.7	—	ns	2
FB5	Data and $\overline{\text{FB_TA}}$ input hold	0.5	—	ns	2

- Specification is valid for all FB_AD[31:0], $\overline{\text{FB_BE/BWE}}$, $\overline{\text{FB_CS}}$, $\overline{\text{FB_OE}}$, $\overline{\text{FB_R/W}}$, $\overline{\text{FB_TBST}}$, $\overline{\text{FB_TSIZ}}[1:0]$, $\overline{\text{FB_ALE}}$, and $\overline{\text{FB_TS}}$.
- Specification is valid for all FB_AD[31:0] and $\overline{\text{FB_TA}}$.

Peripheral operating requirements and behaviors

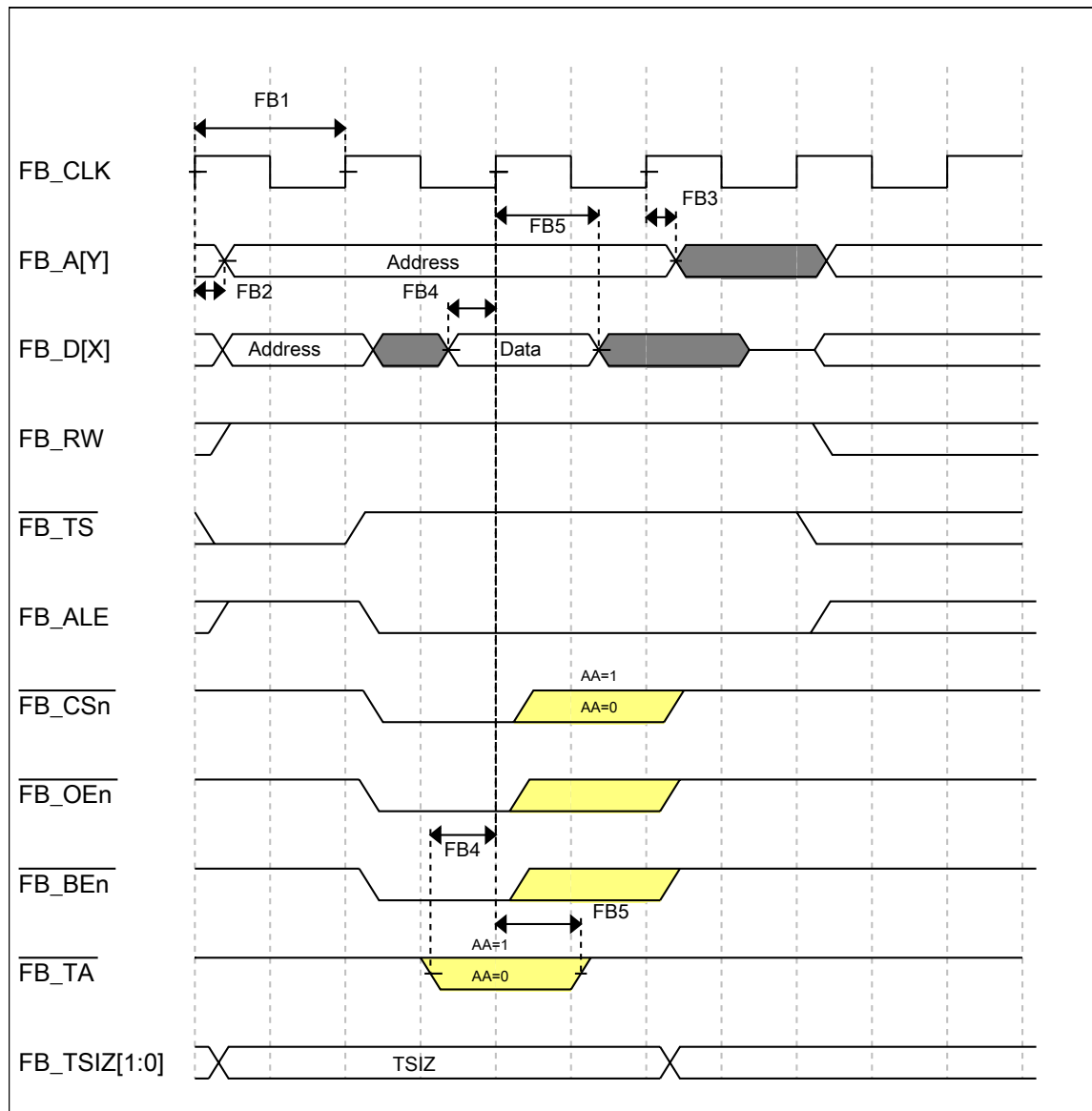


Figure 13. FlexBus read timing diagram

Peripheral operating requirements and behaviors

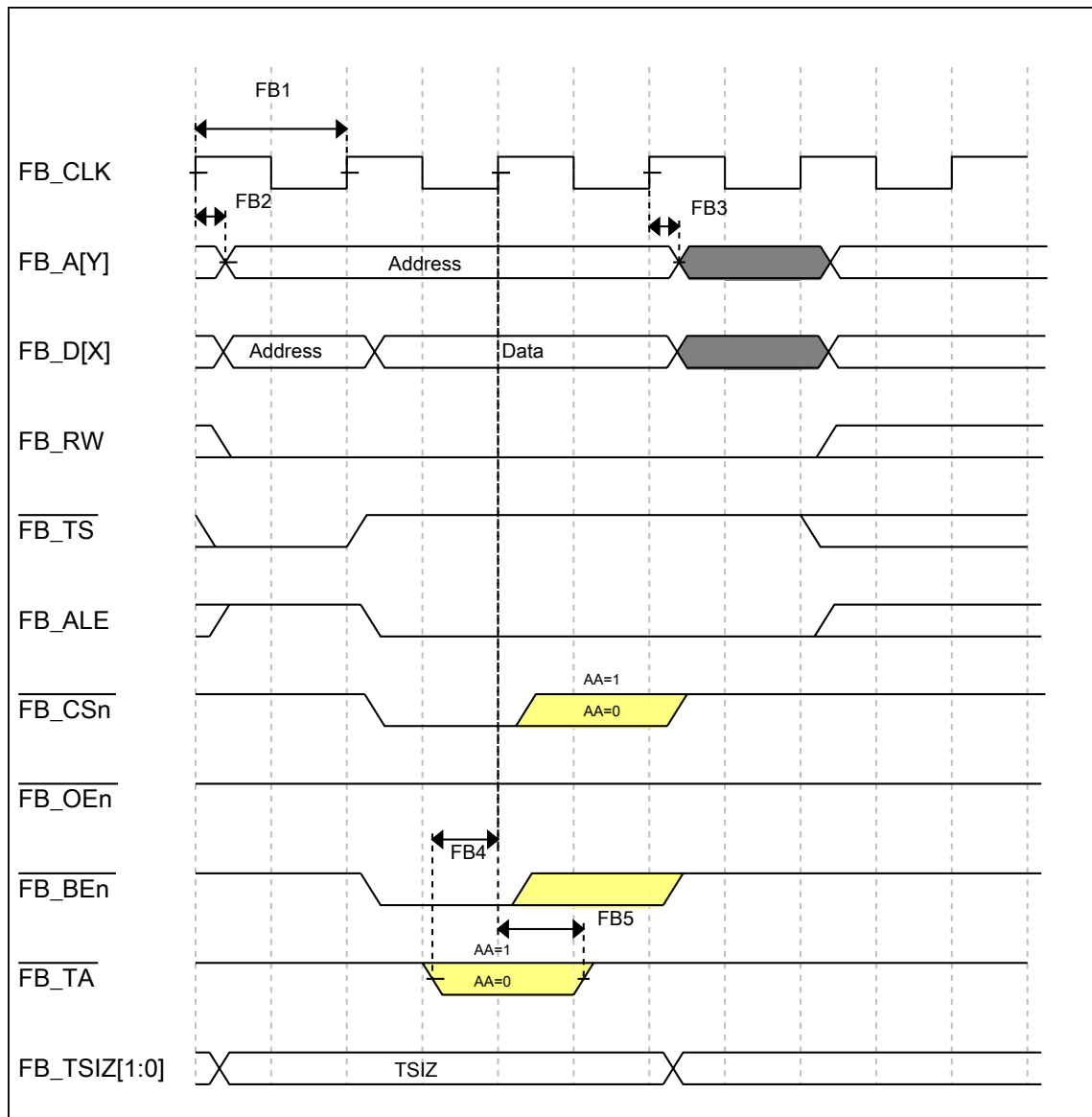


Figure 14. FlexBus write timing diagram

3.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

3.6 Analog

3.6.1 ADC electrical specifications

The 16-bit accuracy specifications listed in [Table 27](#) and [Table 28](#) are achievable on the differential pins ADCx_DP0, ADCx_DM0.

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

3.6.1.1 16-bit ADC operating conditions

Table 27. 16-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
V _{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	—
ΔV _{DDA}	Supply voltage	Delta to V _{DD} (V _{DD} – V _{DDA})	-100	0	+100	mV	2
ΔV _{SSA}	Ground voltage	Delta to V _{SS} (V _{SS} – V _{SSA})	-100	0	+100	mV	2
V _{REFH}	ADC reference voltage high		1.13	V _{DDA}	V _{DDA}	V	
V _{REFL}	ADC reference voltage low		V _{SSA}	V _{SSA}	V _{SSA}	V	
V _{ADIN}	Input voltage	16-bit differential mode - All other modes	V _{REFL} V _{REFL}	— —	31/32 * V _{REFH} V _{REFH}	V	—
C _{ADIN}	Input capacitance	16-bit mode 8-bit / 10-bit / 12-bit modes	— —	8 4	10 5	pF	—
R _{ADIN}	Input series resistance		—	2	5	kΩ	—
R _{AS}	Analog source resistance (external)	13-bit / 12-bit modes f _{ADCK} < 4 MHz	—	—	5	kΩ	3
f _{ADCK}	ADC conversion clock frequency	≤ 13-bit mode	1.0	—	18.0	MHz	4
f _{ADCK}	ADC conversion clock frequency	16-bit mode	2.0	—	12.0	MHz	4
C _{rate}	ADC conversion rate	≤ 13-bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20.000	—	818.330	Ksps	5
C _{rate}	ADC conversion rate	16-bit mode No ADC hardware averaging	37.037	—	461.467	Ksps	5

Peripheral operating requirements and behaviors

Table 27. 16-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
		Continuous conversions enabled, subsequent conversion time					

1. Typical values assume $V_{DDA} = 3.0\text{ V}$, $\text{Temp} = 25\text{ }^{\circ}\text{C}$, $f_{\text{ADCK}} = 1.0\text{ MHz}$, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had $< 8\text{ }\Omega$ analog source resistance. The $R_{\text{AS}}/C_{\text{AS}}$ time constant should be kept to $< 1\text{ ns}$.
4. To use the maximum ADC conversion clock frequency, $\text{CFG2}[\text{ADHSC}]$ must be set and $\text{CFG1}[\text{ADLPC}]$ must be clear.
5. For guidelines and examples of conversion rate calculation, download the [ADC calculator tool](#).

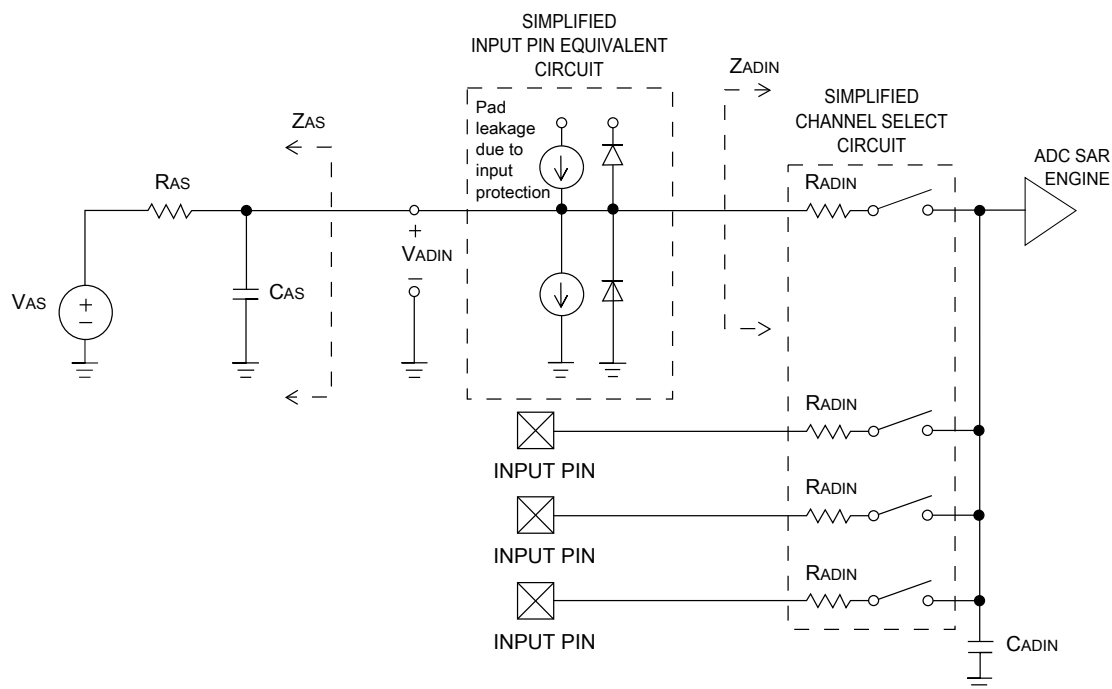


Figure 15. ADC input impedance equivalency diagram

3.6.1.2 16-bit ADC electrical characteristics

Table 28. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
I _{DDA ADC}	Supply current		0.215	—	1.7	mA	3

Table continues on the next page...

Peripheral operating requirements and behaviors

Table 28. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
f_{ADACK}	ADC asynchronous clock source	• ADLPC = 1, ADHSC = 0 • ADLPC = 1, ADHSC = 1 • ADLPC = 0, ADHSC = 0 • ADLPC = 0, ADHSC = 1	1.2 2.4 3.0 4.4	2.4 4.0 5.2 6.2	3.9 6.1 7.3 9.5	MHz MHz MHz MHz	$t_{ADACK} = 1/f_{ADACK}$
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	• 12-bit modes • <12-bit modes	— —	± 4 ± 1.4	± 6.8 ± 2.1	LSB ⁴	5
DNL	Differential non-linearity	• 12-bit modes • <12-bit modes	— —	± 0.7 ± 0.2	–1.1 to +1.9 –0.3 to 0.5	LSB ⁴	5
INL	Integral non-linearity	• 12-bit modes • <12-bit modes	— —	± 1.0 ± 0.5	–2.7 to +1.9 –0.7 to +0.5	LSB ⁴	5
E_{FS}	Full-scale error	• 12-bit modes • <12-bit modes	— —	–4 –1.4	–5.4 –1.8	LSB ⁴	$V_{ADIN} = V_{DDA}$ ⁵
E_Q	Quantization error	• 16-bit modes • ≤ 13-bit modes	— —	–1 to 0 —	— ± 0.5	LSB ⁴	
ENOB	Effective number of bits	16-bit differential mode • Avg = 32 • Avg = 4 16-bit single-ended mode • Avg = 32 • Avg = 4	12.8 11.9 12.2 11.4	14.5 13.8 13.9 13.1	 — — — —	bits bits bits bits	6
SINAD	Signal-to-noise plus distortion	See ENOB	$6.02 \times \text{ENOB} + 1.76$			dB	
THD	Total harmonic distortion	16-bit differential mode • Avg = 32 16-bit single-ended mode • Avg = 32	— —	–94 –85	— —	dB dB	7
SFDR	Spurious free dynamic range	16-bit differential mode • Avg = 32 16-bit single-ended mode • Avg = 32	82 78	95 90	— —	dB dB	7

Table continues on the next page...

Peripheral operating requirements and behaviors

Table 28. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
E_{IL}	Input leakage error			$I_{IN} \times R_{AS}$		mV	I_{IN} = leakage current (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	1.55	1.62	1.69	mV/°C	8
V_{TEMP25}	Temp sensor voltage	25 °C	706	716	726	mV	8

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH} = V_{DDA}$
2. Typical values assume $V_{DDA} = 3.0$ V, Temp = 25 °C, $f_{ADCK} = 2.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
4. $1 \text{ LSB} = (V_{REFH} - V_{REFL})/2^N$
5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
7. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.
8. ADC conversion clock < 3 MHz

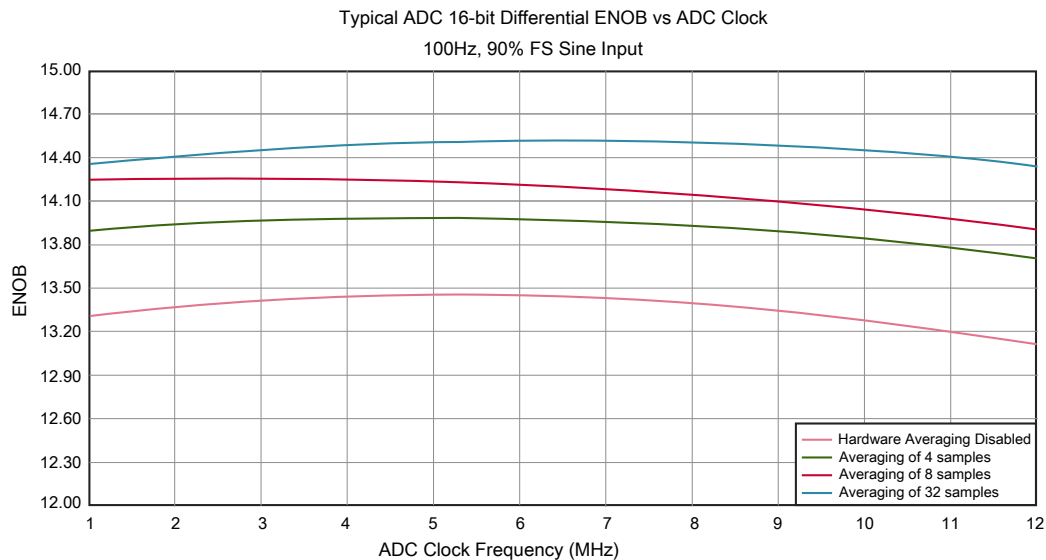


Figure 16. Typical ENOB vs. ADC_CLK for 16-bit differential mode

Peripheral operating requirements and behaviors

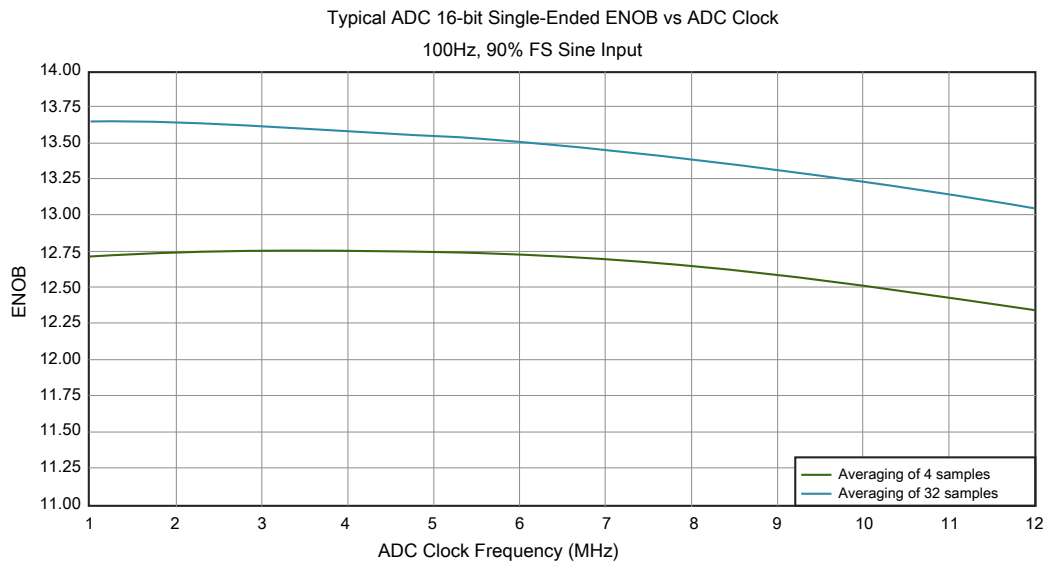


Figure 17. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode

3.6.2 CMP and 6-bit DAC electrical specifications

Table 29. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	1.71	—	3.6	V
I_{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	200	μ A
I_{DDLs}	Supply current, low-speed mode (EN=1, PMODE=0)	—	—	20	μ A
V_{AIN}	Analog input voltage	$V_{SS} - 0.3$	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV
V_H	Analog comparator hysteresis ¹ - CR0[HYSTCTR] = 00 - CR0[HYSTCTR] = 01 - CR0[HYSTCTR] = 10 - CR0[HYSTCTR] = 11	—	5 10 20 30	—	mV mV mV mV
V_{CMPOh}	Output high	$V_{DD} - 0.5$	—	—	V
V_{CMPOl}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay ²	—	—	40	μ s
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	μ A
INL	6-bit DAC integral non-linearity	-0.5	—	0.5	LSB ³
DNL	6-bit DAC differential non-linearity	-0.3	—	0.3	LSB

Peripheral operating requirements and behaviors

1. Typical hysteresis is measured with input voltage range limited to 0.6 to $V_{DD}-0.6$ V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP_DACCR[DACEN], CMP_DACCR[VRSEL], CMP_DACCR[VOSEL], CMP_MUXCR[PSEL], and CMP_MUXCR[MSEL]) and the comparator output settling to a stable level.
3. $1 \text{ LSB} = V_{\text{reference}}/64$

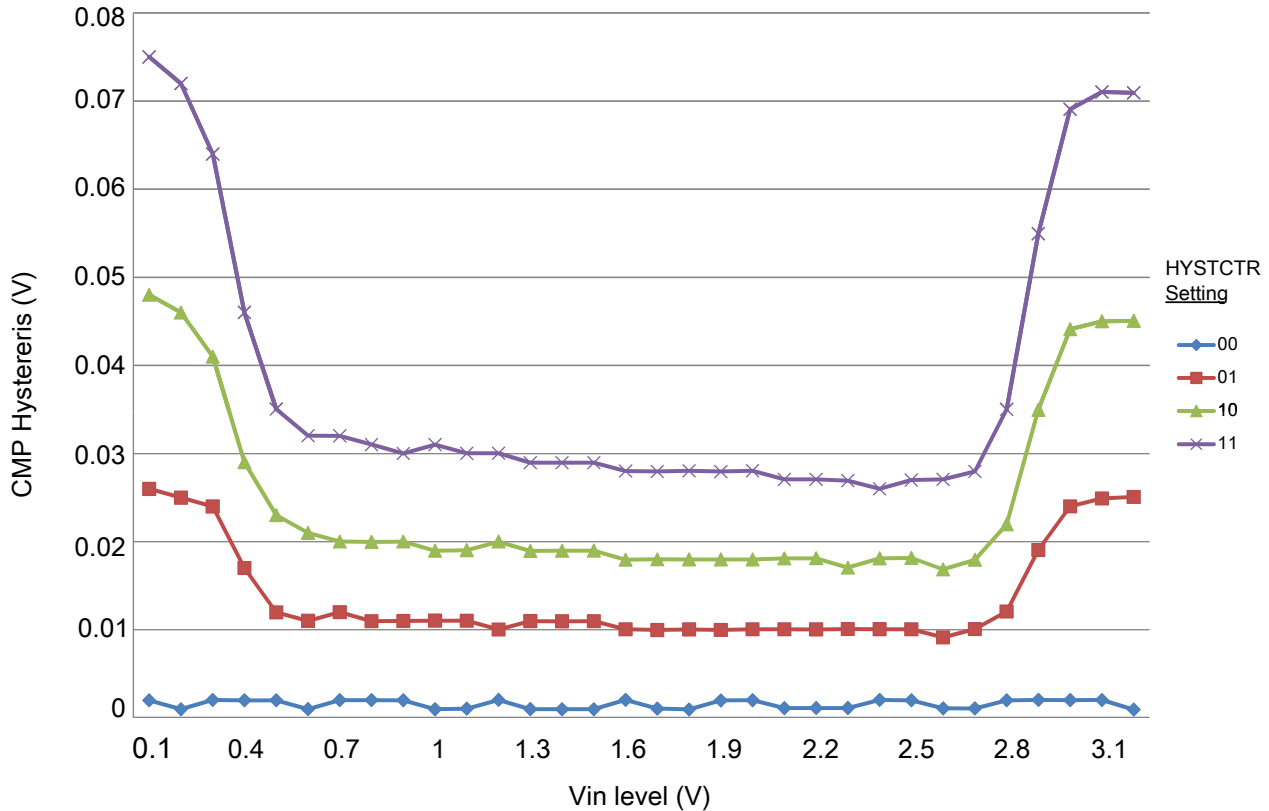


Figure 18. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)

Peripheral operating requirements and behaviors

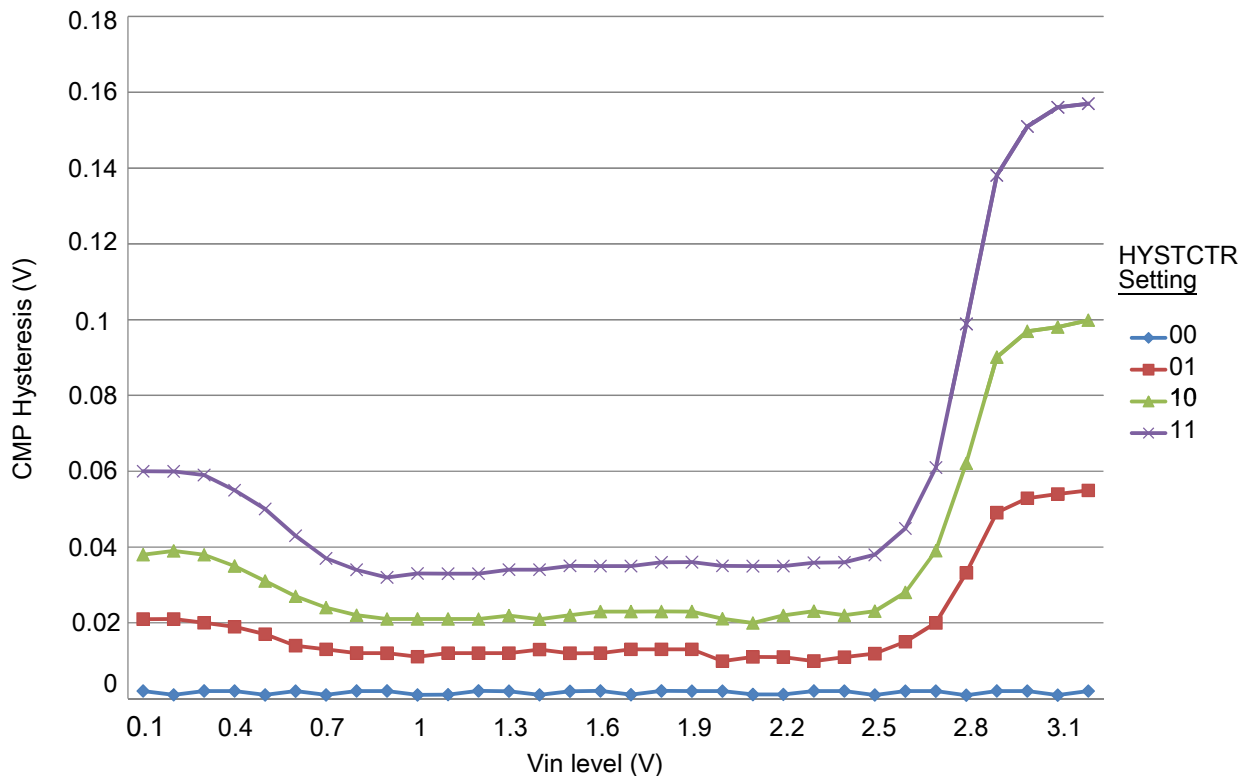


Figure 19. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)

3.6.3 12-bit DAC electrical characteristics

3.6.3.1 12-bit DAC operating requirements

Table 30. 12-bit DAC operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	1.71	3.6	V	
V_{DACR}	Reference voltage	1.13	3.6	V	1
C_L	Output load capacitance	—	100	pF	2
I_L	Output load current	—	1	mA	

1. The DAC reference can be selected to be V_{DDA} or V_{REFH} .
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC.

Peripheral operating requirements and behaviors

3.6.3.2 12-bit DAC operating behaviors

Table 31. 12-bit DAC operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA_DACLP}	Supply current — low-power mode	—	—	150	μA	
I_{DDA_DACHP}	Supply current — high-speed mode	—	—	700	μA	
t_{DACLP}	Full-scale settling time (0x080 to 0xF7F) — low-power mode	—	100	200	μs	1
t_{DACHP}	Full-scale settling time (0x080 to 0xF7F) — high-power mode	—	15	30	μs	1
$t_{CCDACLP}$	Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode	—	0.7	1	μs	1
$V_{dacoutl}$	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000	—	—	100	mV	
$V_{dacouth}$	DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFFF	$V_{DACR} - 100$	—	V_{DACR}	mV	
INL	Integral non-linearity error — high speed mode	—	—	± 8	LSB	2
DNL	Differential non-linearity error — $V_{DACR} > 2 V$	—	—	± 1	LSB	3
DNL	Differential non-linearity error — $V_{DACR} = V_{REF_OUT}$	—	—	± 1	LSB	4
V_{OFFSET}	Offset error	—	± 0.4	± 0.8	%FSR	5
E_G	Gain error	—	± 0.1	± 0.6	%FSR	5
PSRR	Power supply rejection ratio, $V_{DDA} \geq 2.4 V$	60	—	90	dB	
T_{CO}	Temperature coefficient offset voltage	—	3.7	—	$\mu V/C$	6
T_{GE}	Temperature coefficient gain error	—	0.000421	—	%FSR/C	
A_C	Offset aging coefficient	—	—	100	$\mu V/yr$	
R_{op}	Output resistance (load = 3 k Ω)	—	—	250	Ω	
SR	Slew rate -80h → F7Fh → 80h - High power (SP_{HP}) - Low power (SP_{LP})	1.2 0.05	1.7 0.12	— —	V/ μs	
CT	Channel to channel cross talk	—	—	-80	dB	
BW	3dB bandwidth - High power (SP_{HP}) - Low power (SP_{LP})	550 40	— —	— —	kHz	

1. Settling within ± 1 LSB
2. The INL is measured for 0 + 100 mV to $V_{DACR} - 100$ mV
3. The DNL is measured for 0 + 100 mV to $V_{DACR} - 100$ mV
4. The DNL is measured for 0 + 100 mV to $V_{DACR} - 100$ mV with $V_{DDA} > 2.4 V$
5. Calculated by a best fit curve from $V_{SS} + 100$ mV to $V_{DACR} - 100$ mV

Peripheral operating requirements and behaviors

6. $V_{DDA} = 3.0\text{ V}$, reference select set for V_{DDA} (DACx_CO:DACRFS = 1), high power mode (DACx_C0:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device

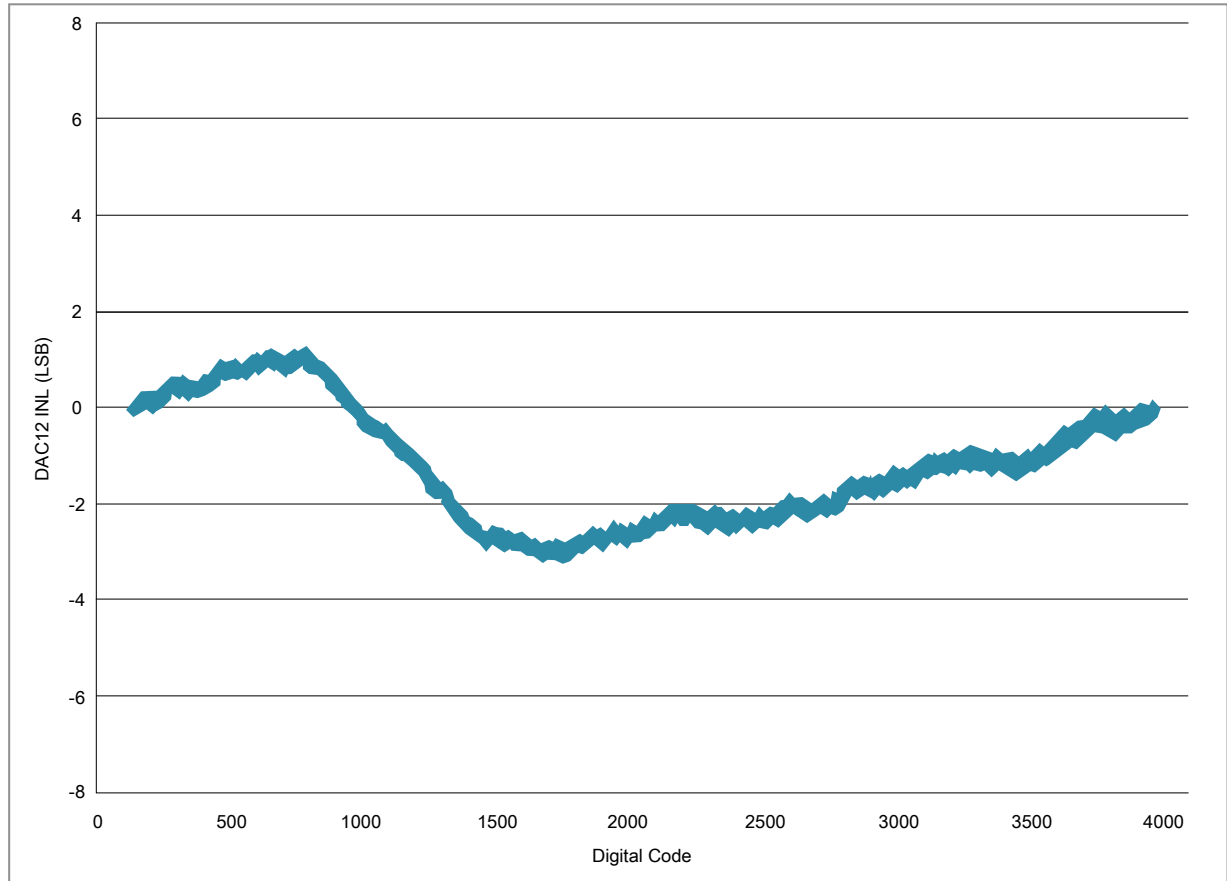


Figure 20. Typical INL error vs. digital code

Peripheral operating requirements and behaviors

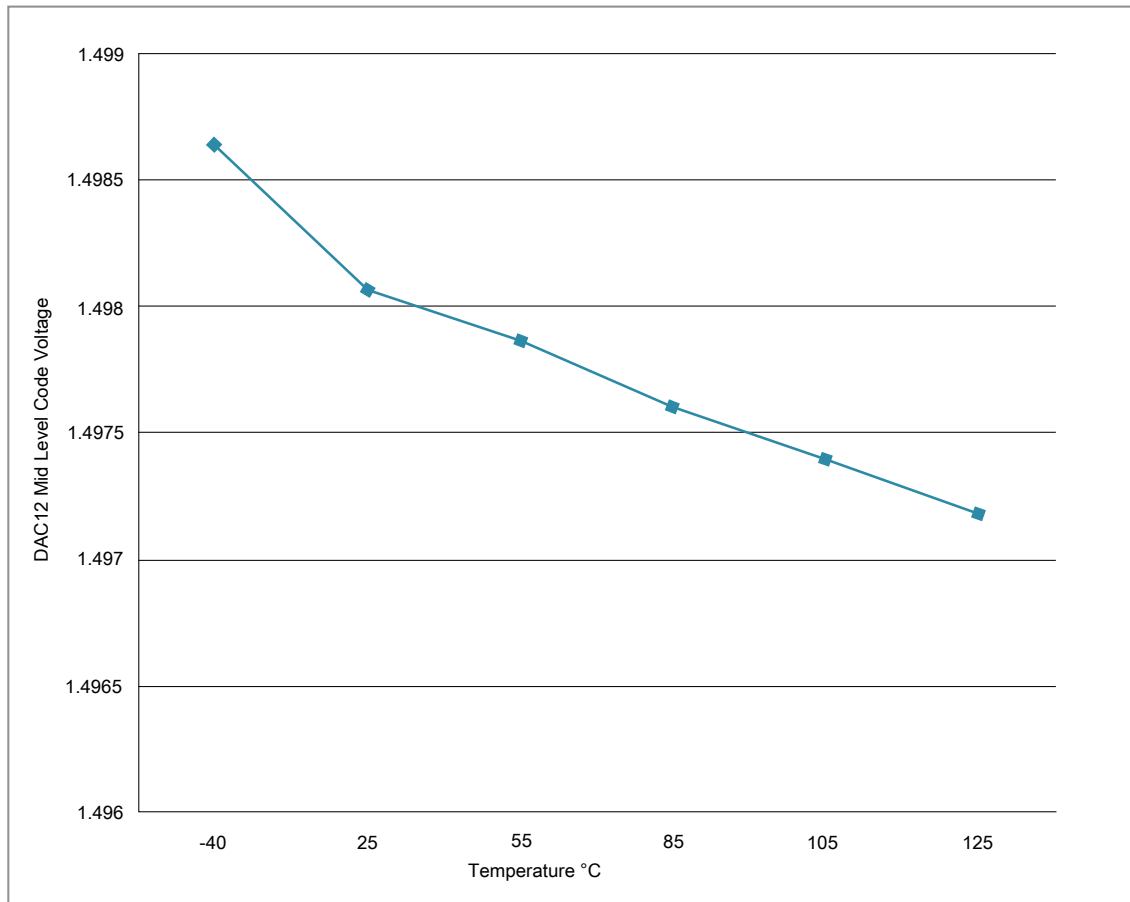


Figure 21. Offset at half scale vs. temperature

3.6.4 Voltage reference electrical specifications

Table 32. VREF full-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V _{DDA}	Supply voltage	1.71	3.6	V	—
T _A	Temperature	Operating temperature range of the device		°C	—
C _L	Output load capacitance	100		nF	1, 2

1. C_L must be connected to VREF_OUT if the VREF_OUT functionality is being used for either an internal or external reference.
2. The load capacitance should not exceed +/-25% of the nominal specified C_L value over the operating temperature range of the device.

Peripheral operating requirements and behaviors

Table 33. VREF full-range operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{out}	Voltage reference output with factory trim at nominal V_{DDA} and temperature=25C	1.1915	1.195	1.1977	V	1
V_{out}	Voltage reference output — factory trim	1.1584	—	1.2376	V	1
V_{out}	Voltage reference output — user trim	1.193	—	1.197	V	1
V_{step}	Voltage reference trim step	—	0.5	—	mV	1
V_{tdrift}	Temperature drift (V_{max} - V_{min} across the full temperature range)	—	—	80	mV	1
I_{bg}	Bandgap only current	—	—	80	μ A	1
ΔV_{LOAD}	Load regulation • current = ± 1.0 mA	—	200	—	μ V	1, 2
T_{stup}	Buffer startup time	—	—	100	μ s	—
V_{vdift}	Voltage drift (V_{max} - V_{min} across the full voltage range)	—	2	—	mV	1

1. See the chip's Reference Manual for the appropriate settings of the VREF Status and Control register.
2. Load regulation voltage is the difference between the VREF_OUT voltage with no load vs. voltage with defined load

Table 34. VREF limited-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T_A	Temperature	0	50	$^{\circ}$ C	—

Table 35. VREF limited-range operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{out}	Voltage reference output with factory trim	1.173	1.225	V	—

3.7 Timers

See [General switching specifications](#).

3.8 Communication interfaces

Peripheral operating requirements and behaviors

3.8.1 USB electrical specifications

The USB electricals for the USB On-the-Go module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit usb.org.

NOTE

The MCGFLLCLK does not meet the USB jitter specifications for certification.

3.8.2 USB DCD electrical specifications

Table 36. USB0 DCD electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V _{DP_SRC}	USB_DP source voltage (up to 250 μ A)	0.5	—	0.7	V
V _{LGC}	Threshold voltage for logic high	0.8	—	2.0	V
I _{DP_SRC}	USB_DP source current	7	10	13	μ A
I _{DM_SINK}	USB_DM sink current	50	100	150	μ A
R _{DM_DWN}	D- pulldown resistance for data pin contact detect	14.25	—	24.8	k Ω
V _{DAT_REF}	Data detect voltage	0.25	0.33	0.4	V

3.8.3 USB VREG electrical specifications

Table 37. USB VREG electrical specifications

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes
VREGIN	Input supply voltage	2.7	—	5.5	V	
I _{DDon}	Quiescent current — Run mode, load current equal zero, input supply (VREGIN) > 3.6 V	—	125	186	μ A	
I _{DDstby}	Quiescent current — Standby mode, load current equal zero	—	1.1	10	μ A	
I _{DDoff}	Quiescent current — Shutdown mode • VREGIN = 5.0 V and temperature=25 °C • Across operating voltage and temperature	—	650	—	nA	
		—	—	4	μ A	
I _{LOADrun}	Maximum load current — Run mode	—	—	120	mA	
I _{LOADstby}	Maximum load current — Standby mode	—	—	1	mA	
V _{Reg33out}	Regulator output voltage — Input supply (VREGIN) > 3.6 V	3	3.3	3.6	V	

Table continues on the next page...

Peripheral operating requirements and behaviors

Table 37. USB VREG electrical specifications (continued)

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes
	- Run mode - Standby mode	2.1	2.8	3.6	V	
V _{Reg33out}	Regulator output voltage — Input supply (VREGIN) < 3.6 V, pass-through mode	2.1	—	3.6	V	2
C _{OUT}	External output capacitor	1.76	2.2	8.16	μF	
ESR	External output capacitor equivalent series resistance	1	—	100	mΩ	
I _{LIM}	Short circuit current	—	290	—	mA	

1. Typical values assume VREGIN = 5.0 V, Temp = 25 °C unless otherwise stated.

2. Operating in pass-through mode: regulator output voltage equal to the input voltage minus a drop proportional to I_{Load}.

3.8.4 CAN switching specifications

See [General switching specifications](#).

3.8.5 DSPI switching specifications (limited voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 38. Master mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	30	MHz	
DS1	DSPI_SCK output cycle time	2 × t _{BUS}	—	ns	
DS2	DSPI_SCK output high/low time	(t _{SCK} /2) – 2	(t _{SCK} /2) + 2	ns	
DS3	DSPI_PCSn valid to DSPI_SCK delay	(t _{BUS} × 2) – 2	—	ns	1
DS4	DSPI_SCK to DSPI_PCSn invalid delay	(t _{BUS} × 2) – 2	—	ns	2
DS5	DSPI_SCK to DSPI_SOUT valid	—	8.5	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	–2	—	ns	

Table continues on the next page...

Peripheral operating requirements and behaviors

Table 38. Master mode DSPI timing (limited voltage range) (continued)

Num	Description	Min.	Max.	Unit	Notes
DS7	DSPI_SIN to DSPI_SCK input setup	15	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
2. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

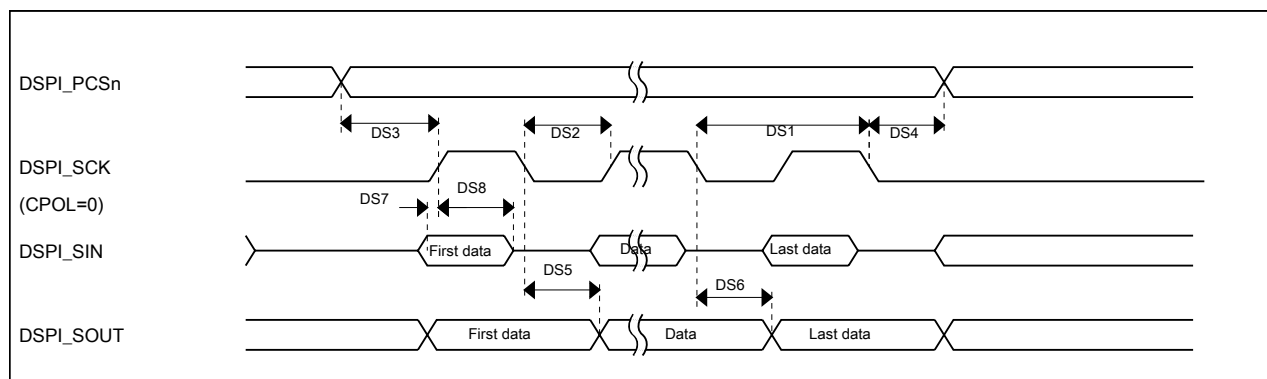


Figure 22. DSPI classic SPI timing — master mode

Table 39. Slave mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation		15	MHz
DS9	DSPI_SCK input cycle time	$4 \times t_{BUS}$	—	ns
DS10	DSPI_SCK input high/low time	$(t_{SCK}/2) - 2$	$(t_{SCK}/2) + 2$	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	17.4	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	DSPI_SS active to DSPI_SOUT driven	—	16	ns
DS16	DSPI_SS inactive to DSPI_SOUT not driven	—	16	ns

Peripheral operating requirements and behaviors

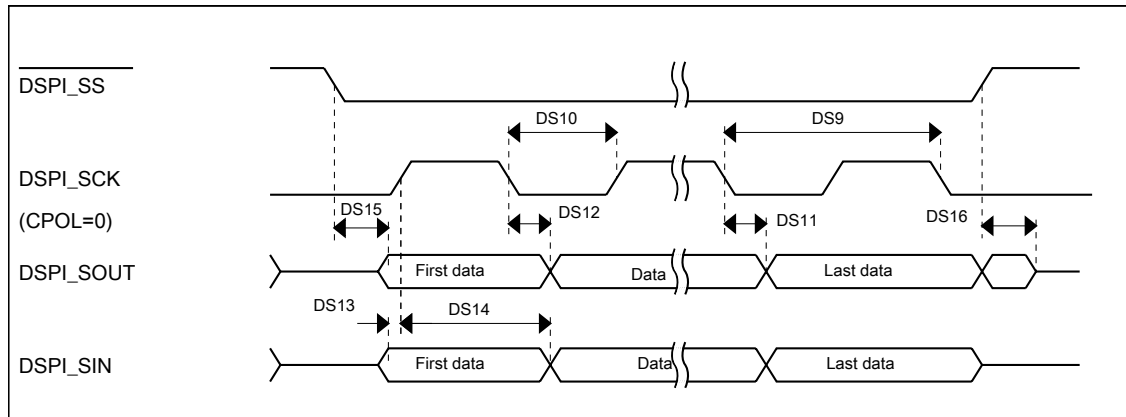


Figure 23. DSPI classic SPI timing — slave mode

3.8.6 DSPI switching specifications (full voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 40. Master mode DSPI timing (full voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	1
	Frequency of operation	—	15	MHz	
DS1	DSPI_SCK output cycle time	$4 \times t_{BUS}$	—	ns	
DS2	DSPI_SCK output high/low time	$(t_{SCK}/2) - 4$	$(t_{SCK}/2) + 4$	ns	
DS3	DSPI_PCSn valid to DSPI_SCK delay	$(t_{BUS} \times 2) - 4$	—	ns	2
DS4	DSPI_SCK to DSPI_PCSn invalid delay	$(t_{BUS} \times 2) - 4$	—	ns	3
DS5	DSPI_SCK to DSPI_SOUT valid	—	10	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-4.5	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	20.5	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
2. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
3. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

Peripheral operating requirements and behaviors

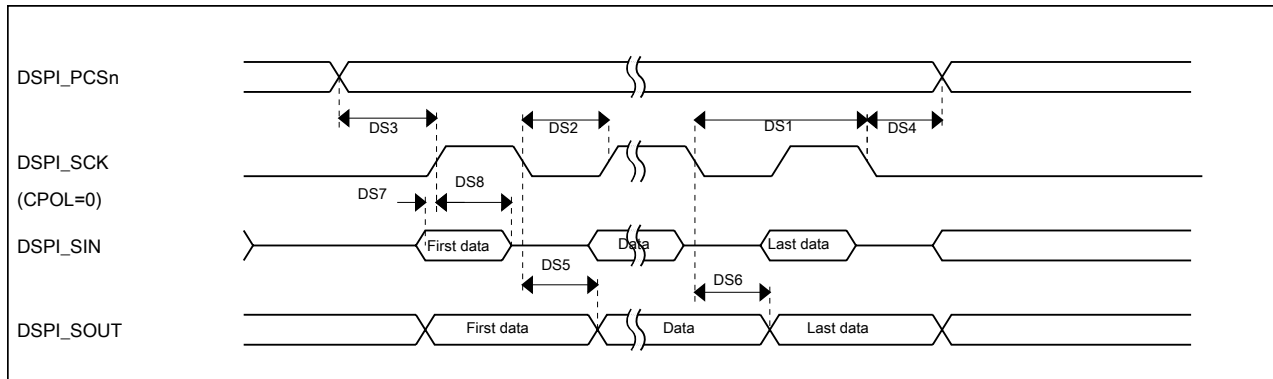


Figure 24. DSPI classic SPI timing — master mode

Table 41. Slave mode DSPI timing (full voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	—	7.5	MHz
DS9	DSPI_SCK input cycle time	$8 \times t_{BUS}$	—	ns
DS10	DSPI_SCK input high/low time	$(t_{SCK}/2) - 4$	$(t_{SCK}/2) + 4$	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	20	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	DSPI_SS active to DSPI_SOUT driven	—	19	ns </td
DS16	DSPI_SS inactive to DSPI_SOUT not driven	—	19	ns

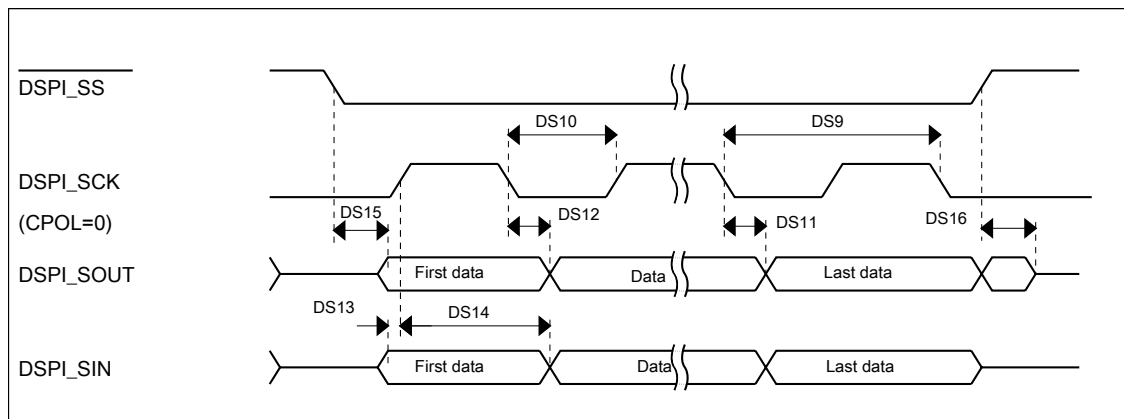


Figure 25. DSPI classic SPI timing — slave mode

3.8.7 I²C switching specifications

See [General switching specifications](#).

3.8.8 UART switching specifications

See [General switching specifications](#).

3.8.9 I²S switching specifications

This section provides the AC timings for the I²S in master (clocks driven) and slave modes (clocks input). All timings are given for non-inverted serial clock polarity (TCR[TSCKP] = 0, RCR[RSCKP] = 0) and a non-inverted frame sync (TCR[TFSI] = 0, RCR[RFSI] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (I2S_BCLK) and/or the frame sync (I2S_FS) shown in the figures below.

Table 42. I²S master mode timing

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
S1	I2S_MCLK cycle time	40	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_BCLK cycle time	80	—	ns
S4	I2S_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_BCLK to I2S_FS output valid	—	15	ns
S6	I2S_BCLK to I2S_FS output invalid	0	—	ns
S7	I2S_BCLK to I2S_TXD valid	—	15	ns
S8	I2S_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_FS input setup before I2S_BCLK	15	—	ns
S10	I2S_RXD/I2S_FS input hold after I2S_BCLK	0	—	ns

Peripheral operating requirements and behaviors

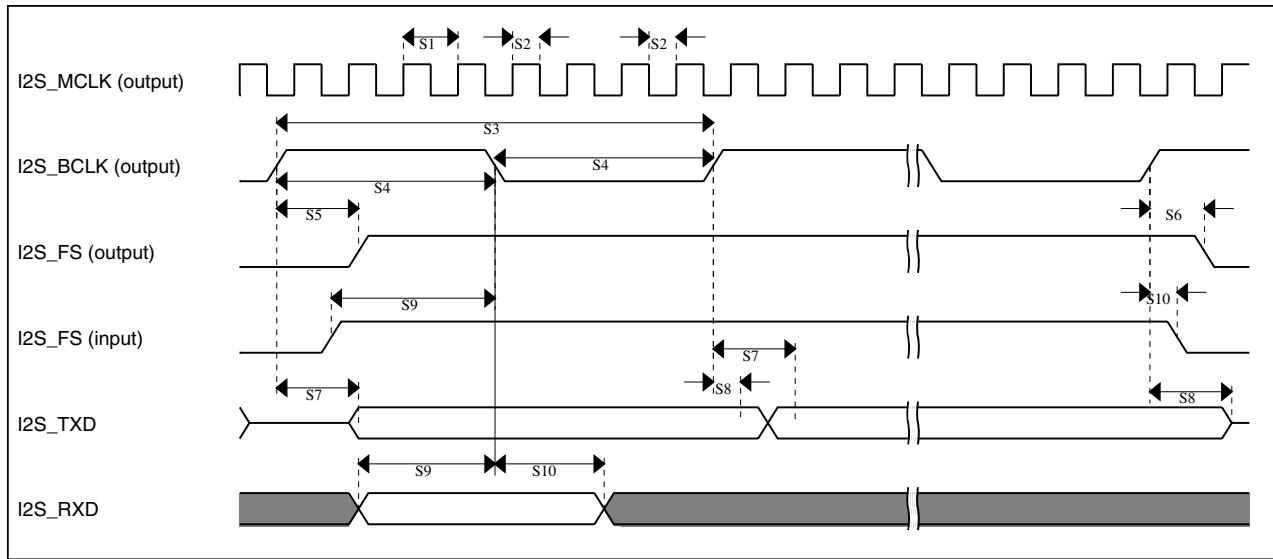


Figure 26. I²S timing — master mode

Table 43. I²S slave mode timing

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
S11	I2S_BCLK cycle time (input)	80	—	ns
S12	I2S_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_FS input setup before I2S_BCLK	4.5	—	ns
S14	I2S_FS input hold after I2S_BCLK	2	—	ns
S15	I2S_BCLK to I2S_TXD/I2S_FS output valid	—	18	ns
S16	I2S_BCLK to I2S_TXD/I2S_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_BCLK	4.5	—	ns
S18	I2S_RXD hold after I2S_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid ¹		21	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

Peripheral operating requirements and behaviors

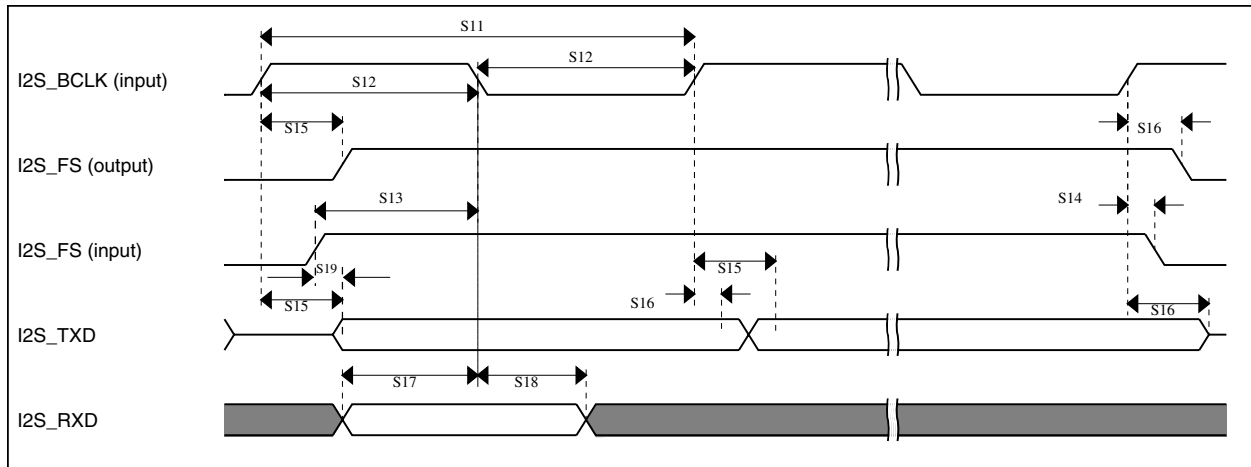


Figure 27. I²S timing — slave modes

3.8.9.1 Normal Run, Wait and Stop mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in Normal Run, Wait and Stop modes.

Table 44. I2S/SAI master mode timing

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	40	—	ns
S2	I2S_MCLK (as an input) pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	80	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	15	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	-1	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	15	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	20.5	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

Peripheral operating requirements and behaviors

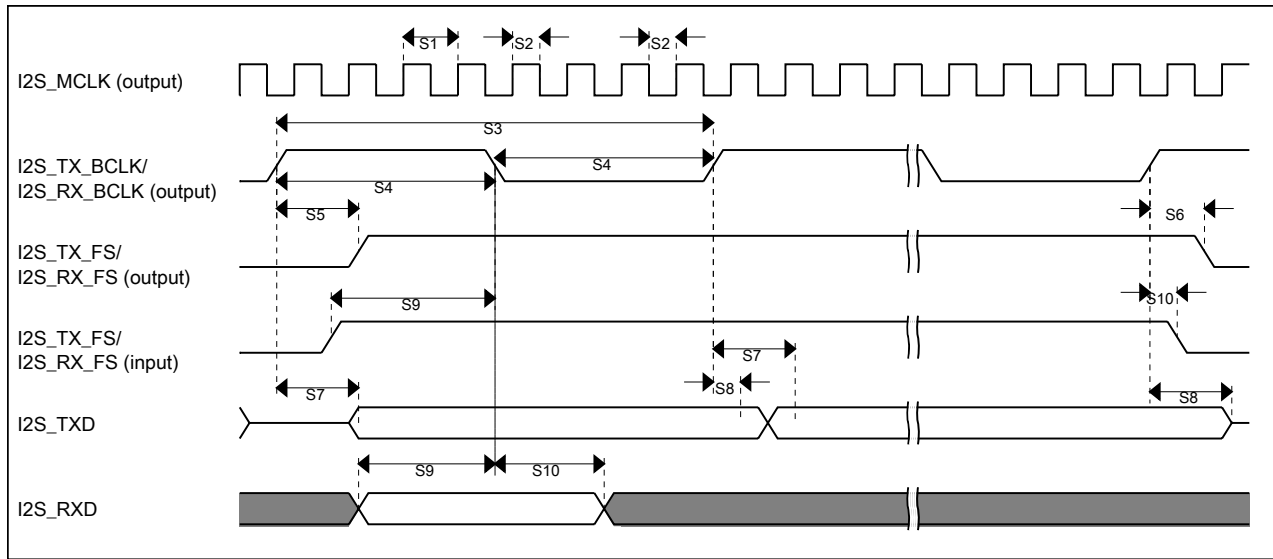


Figure 28. I2S/SAI timing — master modes

Table 45. I2S/SAI slave mode timing

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	80	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	5.8	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	23.5	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	5.8	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid ¹	—	25	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

Peripheral operating requirements and behaviors

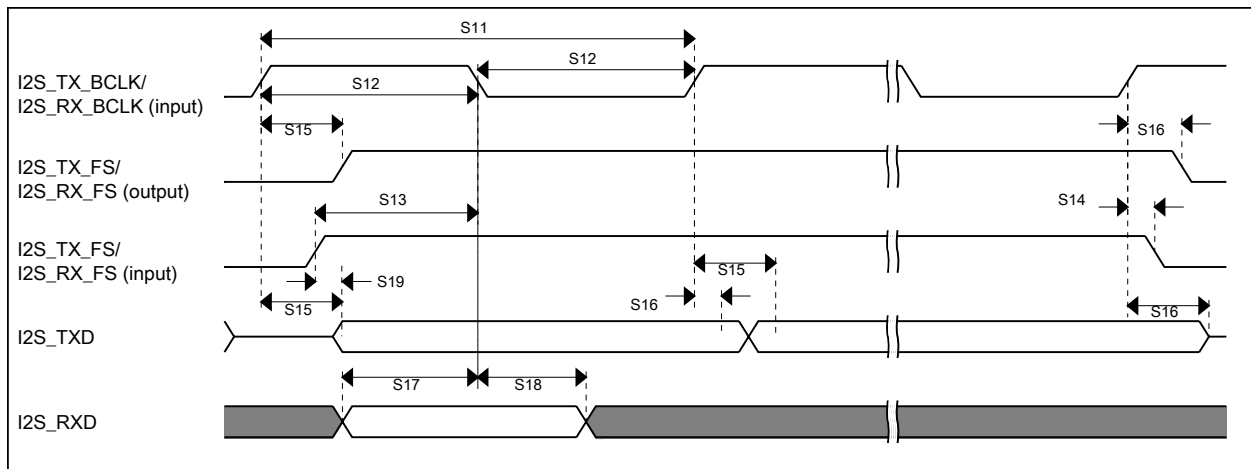


Figure 29. I2S/SAI timing — slave modes

3.8.9.2 VLPR, VLPW, and VLPS mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in VLPR, VLPW, and VLPS modes.

Table 46. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	62.5	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	250	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	45	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	-1	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	45	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	45	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

Peripheral operating requirements and behaviors

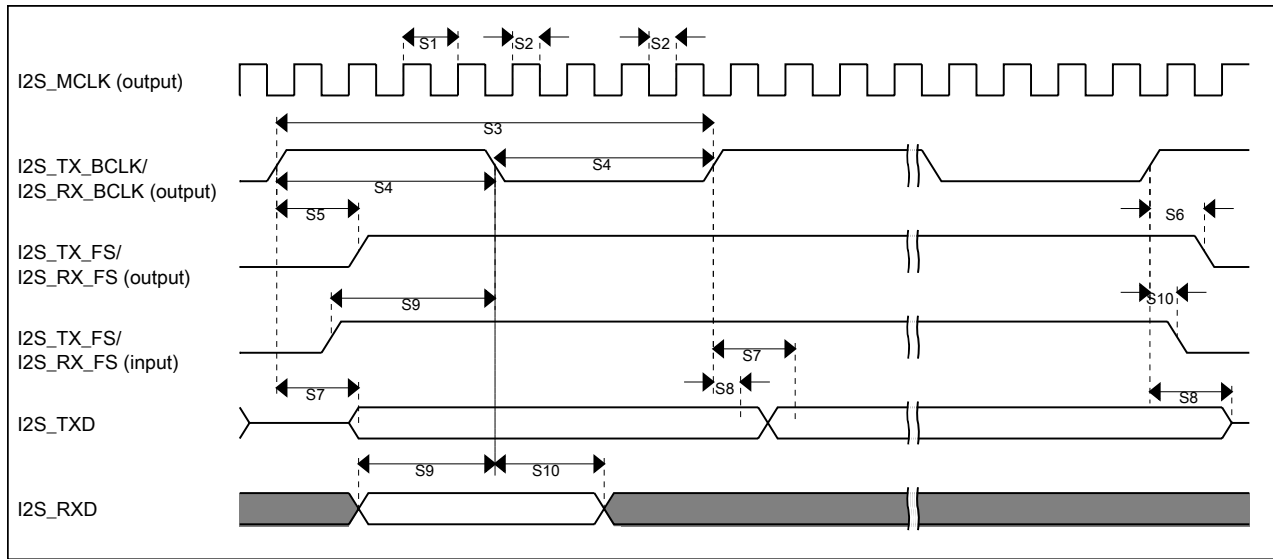


Figure 30. I2S/SAI timing — master modes

Table 47. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	250	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	30	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	3	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	63	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	30	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid ¹	—	72	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

Peripheral operating requirements and behaviors

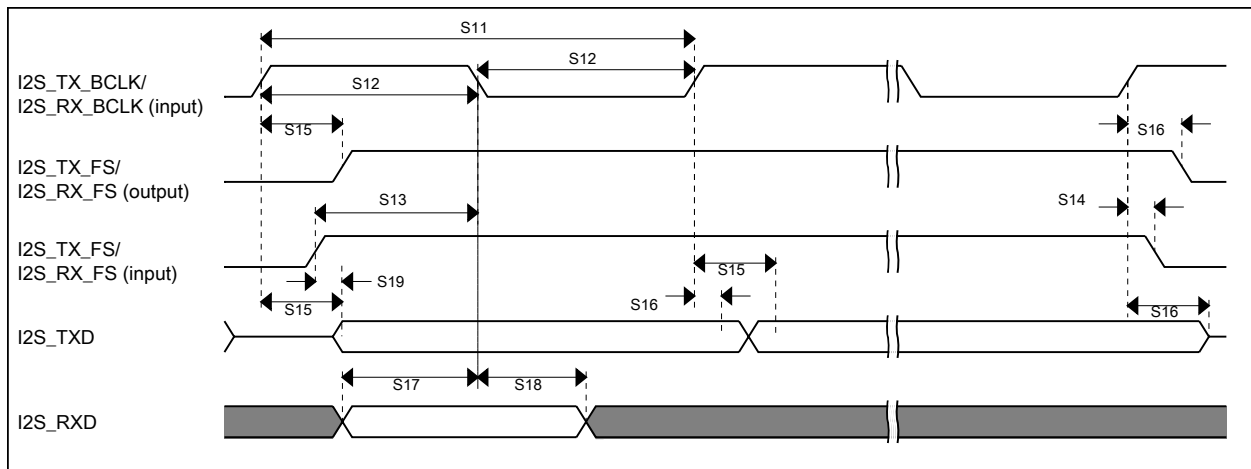


Figure 31. I2S/SAI timing — slave modes

3.8.9.3 Ordering parts

3.8.9.3.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to freescale.com and perform a part number search for the following device numbers: PK22 and MK22

3.8.9.4 Part identification

3.8.9.4.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

3.8.9.4.2 Format

Part numbers for this device have the following format:

Q K## A M FFF R T PP CC N

3.8.9.4.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Peripheral operating requirements and behaviors

Field	Description	Values
Q	Qualification status	- M = Fully qualified, general market flow - P = Prequalification
K##	Kinetis family	K22
A	Key attribute	- D = Cortex-M4 w/ DSP - F = Cortex-M4 w/ DSP and FPU
M	Flash memory type	- N = Program flash only - X = Program flash and FlexMemory
FFF	Program flash memory size	32 = 32 KB 64 = 64 KB 128 = 128 KB 256 = 256 KB 512 = 512 KB 1M0 = 1 MB 2M0 = 2 MB
R	Silicon revision	- Z = Initial (Blank) = Main - A = Revision after main
T	Temperature range (°C)	- V = -40 to 105 - C = -40 to 85
PP	Package identifier	- FM = 32 QFN (5 mm x 5 mm) - FT = 48 QFN (7 mm x 7 mm) - LF = 48 LQFP (7 mm x 7 mm) - LH = 64 LQFP (10 mm x 10 mm) - MP = 64 MAPBGA (5 mm x 5 mm) - LK = 80 LQFP (12 mm x 12 mm) - LL = 100 LQFP (14 mm x 14 mm) - MC = 121 MAPBGA (8 mm x 8 mm) - DC = 121 XFBGA (8 mm x 8 mm x 0.5 mm) - LQ = 144 LQFP (20 mm x 20 mm) - MD = 144 MAPBGA (13 mm x 13 mm)
CC	Maximum CPU frequency (MHz)	5 = 50 MHz 7 = 72 MHz 10 = 100 MHz 12 = 120 MHz 15 = 150 MHz 16 = 168 MHz 18 = 180 MHz
N	Packaging type	- R = Tape and reel (Blank) = Trays

3.8.9.4.4 Example

This is an example part number:

MK22FN1M0VLH10

Peripheral operating requirements and behaviors

3.8.9.4.5 Small package marking

In an effort to save space, small package devices use special marking on the chip. These markings have the following format:

Q ## C F T PP

This table lists the possible values for each field in the part number for small packages (not all combinations are valid):

Field	Description	Values
Q	Qualification status	- M = Fully qualified, general market flow - P = Prequalification
##	Kinetis family	2# = K21/K22
C	Speed	H = 120 MHz
F	Flash memory configuration	- K = 512 KB + Flex 1 = 1 MB
T	Temperature range (°C)	V = -40 to 105
PP	Package identifier	- LL = 100 LQFP - MC = 121 MAPBGA - LQ = 144 LQFP - MD = 144 MAPBGA - DC = 121 XFBGA

This tables lists some examples of small package marking along with the original part numbers:

Original part number	Alternate part number
MK22FX512VLH12	M22HKVLH

3.8.9.5 Terminology and guidelines

3.8.9.5.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

3.8.9.5.1.1 Example

This is an example of an operating requirement:

Peripheral operating requirements and behaviors

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

3.8.9.5.2 Definition: Operating behavior

Unless otherwise specified, an *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

3.8.9.5.2.1 Example

This is an example of an operating behavior:

Symbol	Description	Min.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	130	μA

3.8.9.5.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

3.8.9.5.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
C_{IN_D}	Input capacitance: digital pins	—	7	pF

3.8.9.5.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

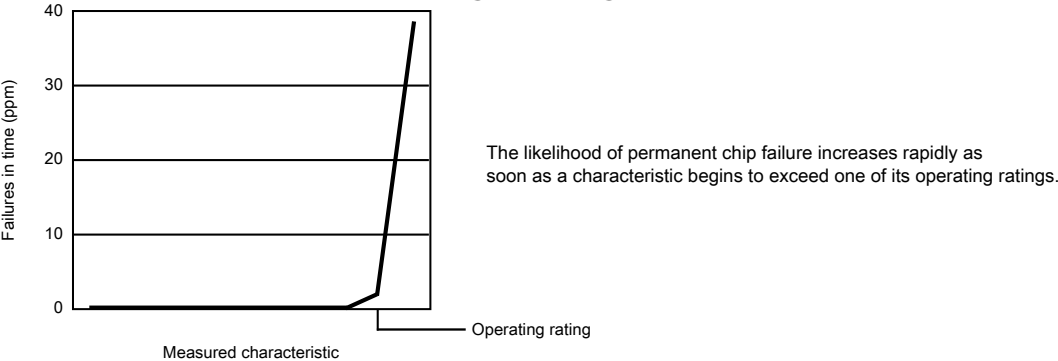
Peripheral operating requirements and behaviors

3.8.9.5.4.1 Example

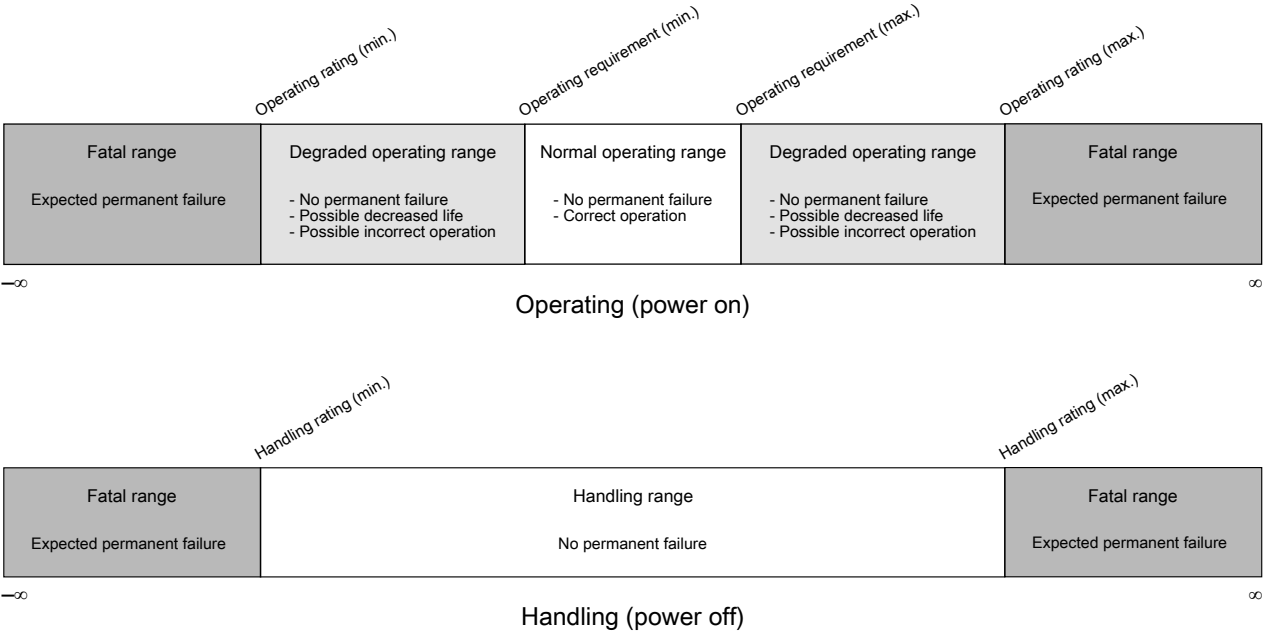
This is an example of an operating rating:

Symbol	Description	Min.	Max.	Unit
V _{DD}	1.0 V core supply voltage	−0.3	1.2	V

3.8.9.5.5 Result of exceeding a rating



3.8.9.5.6 Relationship between ratings and operating requirements



3.8.9.5.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.

Peripheral operating requirements and behaviors

- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

3.8.9.5.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

3.8.9.5.8.1 Example 1

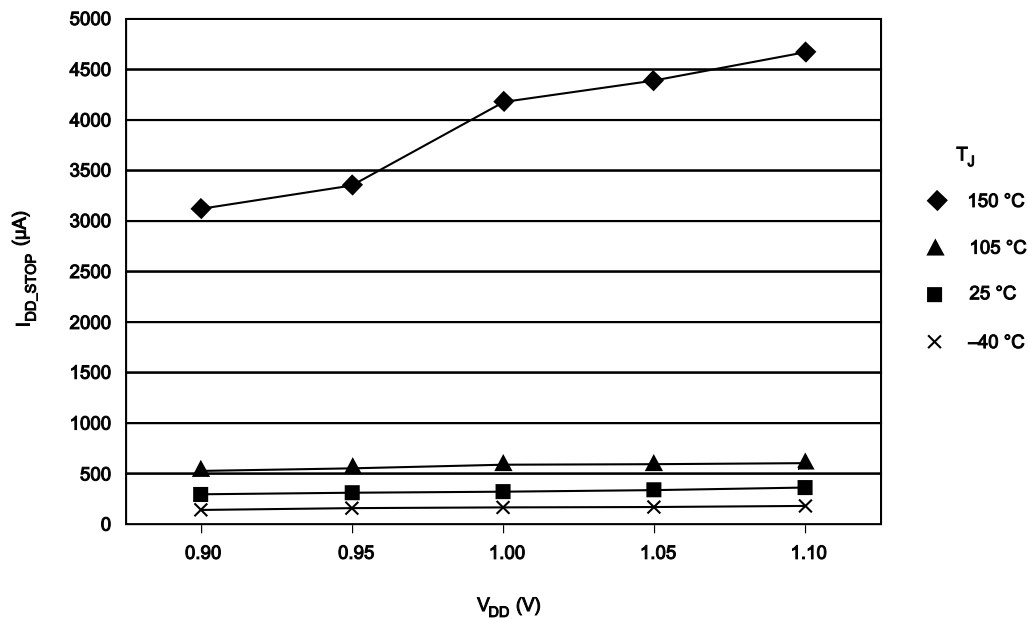
This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	μA

3.8.9.5.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:

Dimensions



3.8.9.5.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T _A	Ambient temperature	25	°C
V _{DD}	3.3 V supply voltage	3.3	V

4 Dimensions

4.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to freescale.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
64-pin LQFP	98ASS23234W

Table continues on the next page...

Pinout

If you want the drawing for this package	Then use this document number
64-pin MAPBGA	98ASA00420D
169-pin MAPBGA	98ASA00628D

5 Pinout

5.1 K22 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

NOTE

- The analog input signals ADC0_DP2 and ADC0_DM2 on PTE2 and PTE3 are available only for K21 and K22 devices and are not present on K10 and K20 devices.
- The TRACE signals on PTE0, PTE1, PTE2, PTE3, and PTE4 are available only for K11, K12, K21, and K22 devices and are not present on K10 and K20 devices.
- If the VBAT pin is not used, the VBAT pin should be left floating. Do not connect VBAT pin to VSS.
- The FTM_CLKIN signals on PTB16 and PTB17 are available only for K11, K12, K21, and K22 devices and is not present on K10 and K20 devices. For K22D devices this signal is on ALT7, and for K22F devices, this signal is on ALT4.
- The FTM0_CH2 signal on PTC5/LLWU_P9 is available only for K11, K12, K21, and K22 devices and is not present on K10 and K20 devices.
- The I2C0_SCL signal on PTD2/LLWU_P13 and I2C0_SDA signal on PTD3 are available only for K11, K12, K21, and K22 devices and are not present on K10 and K20 devices.

64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
1	PTE0	ADC1_SE4a	ADC1_SE4a	PTE0		UART1_TX		TRACE_CLKOUT	I2C1_SDA	RTC_CLKOUT	

Pinout

64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
2	PTE1/LLWU_P0	ADC1_SE5a	ADC1_SE5a	PTE1/LLWU_P0		UART1_RX		TRACE_D3	I2C1_SCL		
3	VDD	VDD	VDD								
4	VSS	VSS	VSS								
5	USB0_DP	USB0_DP	USB0_DP								
6	USB0_DM	USB0_DM	USB0_DM								
7	VOUT33	VOUT33	VOUT33								
8	VREGIN	VREGIN	VREGIN								
9	ADC0_DP0/ADC1_DP3	ADC0_DP0/ADC1_DP3	ADC0_DP0/ADC1_DP3								
10	ADC0_DM0/ADC1_DM3	ADC0_DM0/ADC1_DM3	ADC0_DM0/ADC1_DM3								
11	ADC1_DP0/ADC0_DP3	ADC1_DP0/ADC0_DP3	ADC1_DP0/ADC0_DP3								
12	ADC1_DM0/ADC0_DM3	ADC1_DM0/ADC0_DM3	ADC1_DM0/ADC0_DM3								
13	VDDA	VDDA	VDDA								
14	VREFH	VREFH	VREFH								
15	VREFL	VREFL	VREFL								
16	VSSA	VSSA	VSSA								
17	VREF_OUT/CMP1_IN5/CMP0_IN5/ADC1_SE18	VREF_OUT/CMP1_IN5/CMP0_IN5/ADC1_SE18	VREF_OUT/CMP1_IN5/CMP0_IN5/ADC1_SE18								
18	DAC0_OUT/CMP1_IN3/ADC0_SE23	DAC0_OUT/CMP1_IN3/ADC0_SE23	DAC0_OUT/CMP1_IN3/ADC0_SE23								
19	XTAL32	XTAL32	XTAL32								
20	EXTAL32	EXTAL32	EXTAL32								
21	VBAT	VBAT	VBAT								
22	PTA0	JTAG_TCLK/SWD_CLK/EZP_CLK		PTA0	UART0_CTS_b	FTM0_CH5				JTAG_TCLK/SWD_CLK	EZP_CLK
23	PTA1	JTAG_TDI/EZP_DI		PTA1	UART0_RX	FTM0_CH6				JTAG_TDI	EZP_DI
24	PTA2	JTAG_TDO/TRACE_SWO/EZP_DO		PTA2	UART0_TX	FTM0_CH7				JTAG_TDO/TRACE_SWO	EZP_DO
25	PTA3	JTAG_TMS/SWD_DIO		PTA3	UART0_RTS_b	FTM0_CH0				JTAG_TMS/SWD_DIO	
26	PTA4/LLWU_P3	NMI_b/EZP_CS_b		PTA4/LLWU_P3		FTM0_CH1				NMI_b	EZP_CS_b
27	PTA5	DISABLED		PTA5	USB_CLKIN	FTM0_CH2		CMP2_OUT	I2S0_TX_BCLK	JTAG_TRST_b	

Pinout

64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
28	PTA12	CMP2_IN0	CMP2_IN0	PTA12	CAN0_TX	FTM1_CH0		I2C2_SCL	I2S0_TXD0	FTM1_QD_PHA	
29	PTA13/LLWU_P4	CMP2_IN1	CMP2_IN1	PTA13/LLWU_P4	CAN0_RX	FTM1_CH1		I2C2_SDA	I2S0_TX_FS	FTM1_QD_PHB	
30	VDD	VDD	VDD								
31	VSS	VSS	VSS								
32	PTA18	EXTAL0	EXTAL0	PTA18		FTM0_FLT2	FTM_CLKIN0				
33	PTA19	XTAL0	XTAL0	PTA19		FTM1_FLT0	FTM_CLKIN1		LPTMR0_ALT1		
34	RESET_b	RESET_b	RESET_b								
35	PTB0/LLWU_P5	ADC0_SE8/ADC1_SE8	ADC0_SE8/ADC1_SE8	PTB0/LLWU_P5	I2C0_SCL	FTM1_CH0			FTM1_QD_PHA		
36	PTB1	ADC0_SE9/ADC1_SE9	ADC0_SE9/ADC1_SE9	PTB1	I2C0_SDA	FTM1_CH1			FTM1_QD_PHB		
37	PTB2	ADC0_SE12	ADC0_SE12	PTB2	I2C0_SCL	UART0_RTS_b			FTM0_FLT3		
38	PTB3	ADC0_SE13	ADC0_SE13	PTB3	I2C0_SDA	UART0_CTS_b			FTM0_FLT0		
39	PTB16	DISABLED		PTB16		UART0_RX	FTM_CLKIN0	FB_AD17	EWM_IN		
40	PTB17	DISABLED		PTB17		UART0_TX	FTM_CLKIN1	FB_AD16	EWM_OUT_b		
41	PTB18	DISABLED		PTB18	CAN0_TX	FTM2_CH0	I2S0_TX_BCLK	FB_AD15	FTM2_QD_PHA		
42	PTB19	DISABLED		PTB19	CAN0_RX	FTM2_CH1	I2S0_TX_FS	FB_OE_b	FTM2_QD_PHB		
43	PTC0	ADC0_SE14	ADC0_SE14	PTC0	SPI0_PCS4	PDB0_EXTRG		FB_AD14	I2S0_TXD1		
44	PTC1/LLWU_P6	ADC0_SE15	ADC0_SE15	PTC1/LLWU_P6	SPI0_PCS3	UART1_RTS_b	FTM0_CH0	FB_AD13	I2S0_TXD0		
45	PTC2	ADC0_SE4b/CMP1_IN0	ADC0_SE4b/CMP1_IN0	PTC2	SPI0_PCS2	UART1_CTS_b	FTM0_CH1	FB_AD12	I2S0_TX_FS		
46	PTC3/LLWU_P7	CMP1_IN1	CMP1_IN1	PTC3/LLWU_P7	SPI0_PCS1	UART1_RX	FTM0_CH2	CLKOUT	I2S0_TX_BCLK		
47	VSS	VSS	VSS								
48	VDD	VDD	VDD								
49	PTC4/LLWU_P8	DISABLED		PTC4/LLWU_P8	SPI0_PCS0	UART1_TX	FTM0_CH3	FB_AD11	CMP1_OUT		
50	PTC5/LLWU_P9	DISABLED		PTC5/LLWU_P9	SPI0_SCK	LPTMR0_ALT2	I2S0_RXD0	FB_AD10	CMP0_OUT	FTM0_CH2	
51	PTC6/LLWU_P10	CMP0_IN0	CMP0_IN0	PTC6/LLWU_P10	SPI0_SOUT	PDB0_EXTRG	I2S0_RX_BCLK	FB_AD9	I2S0_MCLK		
52	PTC7	CMP0_IN1	CMP0_IN1	PTC7	SPI0_SIN	USB_SOF_OUT	I2S0_RX_FS	FB_AD8			
53	PTC8	ADC1_SE4b/CMP0_IN2	ADC1_SE4b/CMP0_IN2	PTC8		FTM3_CH4	I2S0_MCLK	FB_AD7			

Pinout

64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
54	PTC9	ADC1_SE5b/ CMP0_IN3	ADC1_SE5b/ CMP0_IN3	PTC9		FTM3_CH5	I2S0_RX_ BCLK	FB_AD6	FTM2_FLT0		
55	PTC10	ADC1_SE6b	ADC1_SE6b	PTC10	I2C1_SCL	FTM3_CH6	I2S0_RX_FS	FB_AD5			
56	PTC11/ LLWU_P11	ADC1_SE7b	ADC1_SE7b	PTC11/ LLWU_P11	I2C1_SDA	FTM3_CH7	I2S0_RXD1	FB_RW_b			
57	PTD0/ LLWU_P12	DISABLED		PTD0/ LLWU_P12	SPI0_PCS0	UART2_RTS_ b	FTM3_CH0	FB_ALE/ FB_CS1_b/ FB_TS_b			
58	PTD1	ADC0_SE5b	ADC0_SE5b	PTD1	SPI0_SCK	UART2_CTS_ b	FTM3_CH1	FB_CS0_b			
59	PTD2/ LLWU_P13	DISABLED		PTD2/ LLWU_P13	SPI0_SOUT	UART2_RX	FTM3_CH2	FB_AD4		I2C0_SCL	
60	PTD3	DISABLED		PTD3	SPI0_SIN	UART2_TX	FTM3_CH3	FB_AD3		I2C0_SDA	
61	PTD4/ LLWU_P14	DISABLED		PTD4/ LLWU_P14	SPI0_PCS1	UART0_RTS_ b	FTM0_CH4	FB_AD2	EWM_IN		
62	PTD5	ADC0_SE6b	ADC0_SE6b	PTD5	SPI0_PCS2	UART0_CTS_ b	FTM0_CH5	FB_AD1	EWM_OUT_b		
63	PTD6/ LLWU_P15	ADC0_SE7b	ADC0_SE7b	PTD6/ LLWU_P15	SPI0_PCS3	UART0_RX	FTM0_CH6	FB_AD0	FTM0_FLT0		
64	PTD7	DISABLED		PTD7	CMT_IRO	UART0_TX	FTM0_CH7		FTM0_FLT1		

5.2 K22 Pinouts

The below figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.

Revision History

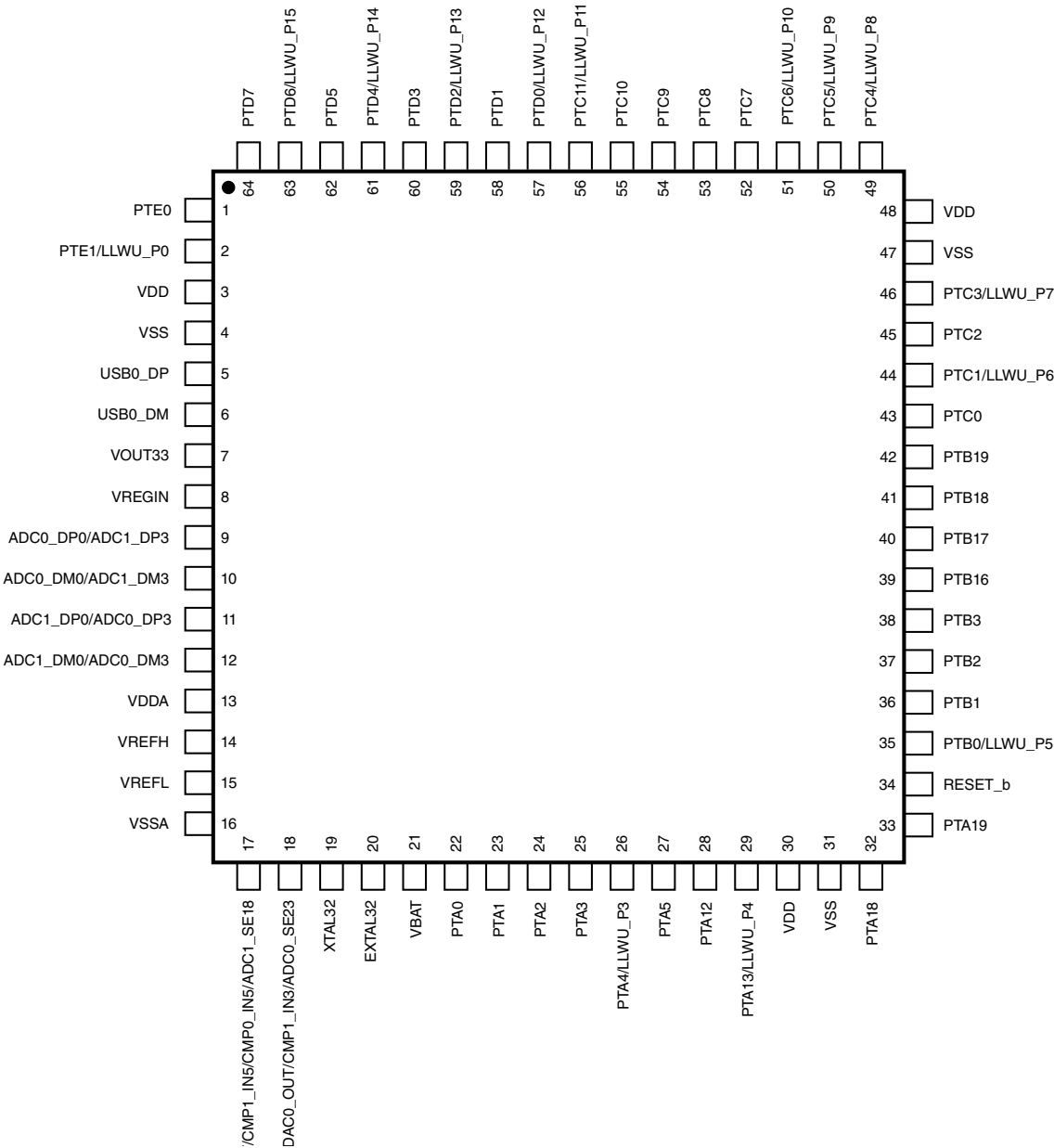


Figure 32. K22 64 LQFP Pinout Diagram

6 Revision History

The following table provides a revision history for this document.

Revision History

Table 48. Revision History

Rev. No.	Date	Substantial Changes
1	11/2012	Alpha customer release
2	5/2013	- Updated supported part numbers and document number - Updated section "Voltage and current operating behaviors" - Added the following figures: - Run mode supply current vs. core frequency - VLPR mode supply current vs. core frequency - Updated section "Device clock specifications" - Updated section "Power consumption operating behaviors" - Updated section "Power mode transition operating behaviors" - Updated section "JTAG limited voltage range electricals" - Updated section "MCG specifications" - Updated section "Oscillator DC electrical specifications" - Updated section "16-bit ADC operating conditions" - Updated the pinouts - Added section "Alternate part numbers for small packages"
3	8/2013	- Updated section "Power consumption operating behaviors" - Updated the "Run mode supply current vs. core frequency" figure in section "Diagram: Typical IDD_RUN operating behavior"
4	11/2014	- Updated the table "Voltage and current operating behavior" - Format changes
5	03/2015	- Updated supported part numbers - Updated document number - Updated the table "I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range)" - Updated the table "I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range)"

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