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[PI74AVC+16345A](#)

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## PI74AVC+16345

### 2.5V, Registered 1-Bit to 4-Bit Address Driver w/3-State Outputs

#### Product Features

- PI74AVC+16345 is designed for low-voltage operation,  $V_{CC} = 1.65V$  to  $3.6V$
- True  $\pm 24mA$  Balanced Drive @ $3.3V$
- $I_{OFF}$  supports partial power down operation
- I/O Tolerant to  $3.6V$
- All outputs contain a patented DDC (Dynamic DriveControl) circuit that reduces noise without degrading propagation delay.
- Industrial operation:  $-40^{\circ}C$  to  $+85^{\circ}C$
- Available Packages:
  - 56-pin 240 mil wide plastic TSSOP (A)
  - 56-pin 173 mil wide plastic TVSOP (K)

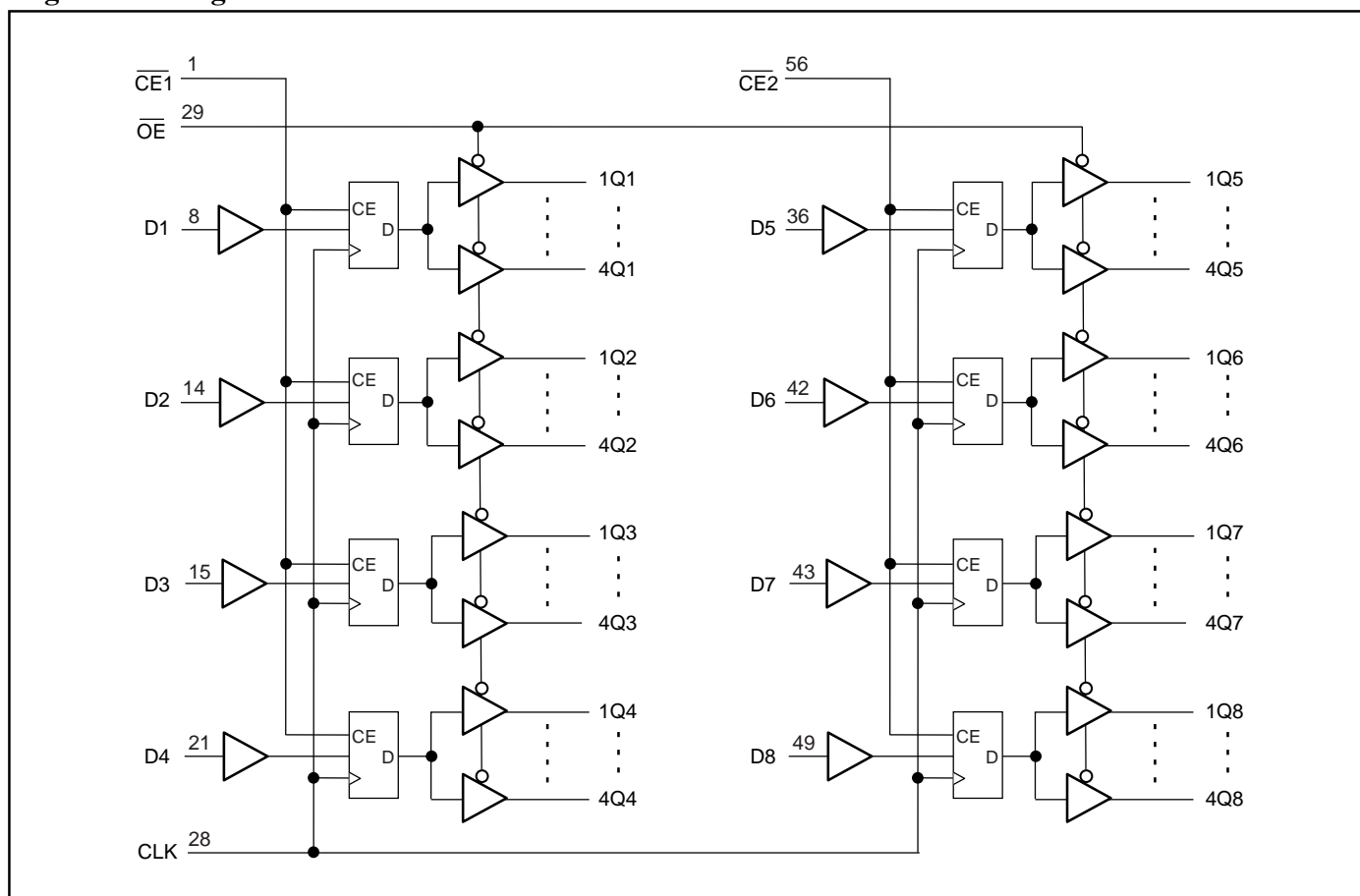
#### Product Description

Pericom Semiconductor's PI74AVC+ series of logic circuits are produced using the Company's advanced submicron CMOS technology, achieving industry leading speed.

The PI74AVC+16345 is ideal for driving memory modules in systems where multiple memory modules are used. One each of the four output banks drive a different module; modules can be added or removed without affecting the signal integrity of the other modules in the system. Dual clock enables ( $CE_x$ ) allow use of the device in high-speed memory interleaving applications where the clock can be alternately enabled and disabled, allowing the address to be held for additional cycles during memory access.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current sinking capability of the driver.

#### Logic Block Diagram





**PI74AVC+16345**  
**2.5V, Registered 1-Bit to 4-Bit Address**  
**Driver with 3-State Outputs**

**Pin Description**

Pin Name	Description
$\overline{OE}$	3-State Output Enable Inputs (Active LOW)
CLK	Clock Input
$\overline{CEx}$	Clock Enable Inputs (Active Low)
Dx	Data Inputs
xQx	3-State Outputs
GND	Ground
Vcc	Power

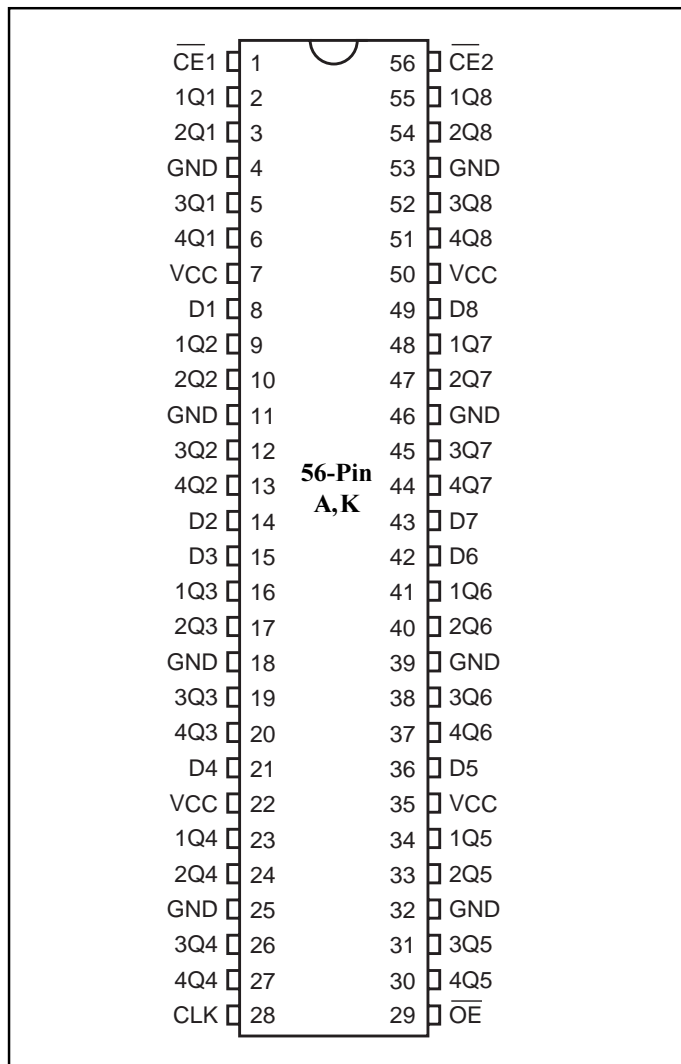
**Truth Table<sup>(1)</sup>**

Inputs				Outputs
$\overline{CEx}$	$\overline{OE}$	CLK	Dx	xQx
H	L	X	X	B0
X	L	L	X	B0
L	L	↑	L	L
L	L	↑	H	H
X	H	X	X	Z

**Note:**

- H = High Signal Level  
 L = Low Signal Level  
 X = Irrelevant  
 Z = High Impedance  
 ↑ = LOW-to-HIGH Transition  
 B0 = Previous State

**Pin Configuration**





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**Maximum Ratings**

(Above which useful life may be impaired.  
 For user guidelines, not tested.)

Supply voltage range, $V_{CC}$ .....	-0.5V to +4.6V
Input voltage range, $V_I$ .....	-0.5V to +4.6V
Voltage range applied to any output in the high-impedance or power-off state, $V_O^{(1)}$ .....	-0.5V to +4.6V
Voltage range applied to any output in the high or low state, $V_O^{(1,2)}$ .....	-0.5V to $V_{CC}+0.5V$
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-50mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	-50mA
Continuous output current, $I_O$ .....	$\pm 50mA$
Continuous current through each $V_{CC}$ or GND .....	$\pm 100mA$
Package thermal impedance, $\theta_{JA}^{(3)}$ : package A .....	64°C/W
package K .....	48°C/W
Storage Temperature range, $T_{stg}$ .....	-65°C to 150°C

**Note:**

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Notes:**

1. Input & output negative-voltage ratings may be exceeded if the input and output current rating are observed.
2. Output positive-voltage rating may be exceeded up to 4.6V maximum if the output current rating is observed.
3. The package thermal impedance is calculated in accordance with JEDEC51.

**Recommended Operating Conditions<sup>(1)</sup>**

		Min.	Max.	Units
$V_{CC}$ Supply Voltage	Operating	1.65	3.6	V
	Data retention only	1.2		
$V_{IH}$ High-level Input Voltage	$V_{CC} = 1.2V$	$V_{CC}$		
	$V_{CC} = 1.65V$ to $1.95V$	$0.65 \times V_{CC}$		
	$V_{CC} = 2.3V$ to $2.7V$	1.7		
	$V_{CC} = 3V$ to $3.6V$	2		
$V_{IL}$ Low-level Input Voltage	$V_{CC} = 1.2V$		Gnd	
	$V_{CC} = 1.65V$ to $1.95V$		$0.35 \times V_{CC}$	
	$V_{CC} = 2.3V$ to $2.7V$		0.7	
	$V_{CC} = 3V$ to $3.6V$		0.8	
$V_I$ Input Voltage		0	3.6	
$V_O$ Output Voltage	Active State	0	$V_{CC}$	
	3-State	0	3.6	
$I_{OH}$ High-level output current	$V_{CC} = 1.65V$ to $1.95V$		-6	mA
	$V_{CC} = 2.3V$ to $2.7V$		-12	
	$V_{CC} = 3V$ to $3.6V$		-24	
$I_{OL}$ Low-level output current	$V_{CC} = 1.65V$ to $1.95V$		6	
	$V_{CC} = 2.3V$ to $2.7V$		12	
	$V_{CC} = 3V$ to $3.6V$		24	
$\Delta t \Delta v$ Input transition rise or fall rate	$V_{CC} = 1.65V$ to $3.6V$		5	ns/V
$T_A$ Operating free-air temperature		-40	85	°C

**Notes:**

1. All unused inputs must be held at  $V_{CC}$  or GND to ensure proper device operation.



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**Driver with 3-State Outputs**

**DC Electrical Characteristics (Over the Operating Range,  $T_A = -40^{\circ}\text{C} + 85^{\circ}\text{C}$ )**

Parameters		Test Conditions <sup>(1)</sup>	V <sub>CC</sub>	Min.	Typ.	Max.	Units
V <sub>OH</sub>		I <sub>OH</sub> = -100μA	1.65V to 3.6V	V <sub>CC</sub> - 0.2V			V
		I <sub>OH</sub> = -6mA    V <sub>IH</sub> = 1.07V	1.65V	1.2			
		I <sub>OH</sub> = -12mA    V <sub>IH</sub> = 1.7V	2.3V	1.75			
		I <sub>OH</sub> = -24mA    V <sub>IH</sub> = 2V	3V	2.0			
V <sub>OL</sub>		I <sub>OL</sub> = 100μA	1.65V to 3.6V			0.2	V
		I <sub>OL</sub> = 6mA    V <sub>IH</sub> = 0.57V	1.65V			0.45	
		I <sub>OL</sub> = 12mA    V <sub>IH</sub> = 0.7V	2.3V			0.55	
		I <sub>OL</sub> = 24mA    V <sub>IH</sub> = 0.8V	3V			0.8	
I <sub>I</sub>	Control Inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	3.6V			±2.5	μA
I <sub>OFF</sub>		V <sub>I</sub> or V <sub>O</sub> = 3.6V	0			±10	
I <sub>OZ</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND	3.6V			±10	
I <sub>CC</sub>		V <sub>O</sub> = V <sub>CC</sub> or GND    I <sub>O</sub> = 0	3.6V			40	
C <sub>I</sub>	Control Inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	2.5V		4		pF
			3.3V		4		
	Data Inputs		2.5V		6		
			3.3V		6		
C <sub>O</sub>	Outputs	V <sub>O</sub> = V <sub>CC</sub> or GND	2.5V		8		
			3.3V		8		

**Note:**

1. Typical values are measured at T<sub>A</sub> = 25°C.



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### Timing Requirements

(Over recommended operating free-air temperature range, unless otherwise noted, see Figures 1 thru 4)

	V <sub>CC</sub> = 1.2V		V <sub>CC</sub> = 1.5V ±0.1V		V <sub>CC</sub> = 1.8V ±0.15V		V <sub>CC</sub> = 2.5V ±0.2V		V <sub>CC</sub> = 3.3V ±0.3V		Units
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
f <sub>clock</sub> Clock Frequency						150		180		180	MHz
t <sub>w</sub> Pulse Width, CLK High or Low					6.0		3		3		ns
t <sub>SU</sub> Setup Time, $\overline{CEx}$ to CLK, High or Low					2.0		1.5		1.5		
t <sub>SU</sub> Setup Time, Dx to CLK, High or Low					2.0		1.5		1.5		
t <sub>H</sub> Hold Time, $\overline{CEx}$ to CLK, High or Low					0		0		0		
t <sub>H</sub> Hold Time, CLK to Dx, High or Low					0.5		0.5		0.5		

### Switching Characteristics

(Over recommended operating free-air temperature range, unless otherwise noted, see Figures 1 thru 4)

Parameters	From (Input)	To (Output)	V <sub>CC</sub> = 1.2V		V <sub>CC</sub> = 1.5V ±0.1V		V <sub>CC</sub> = 1.8V ±0.15V		V <sub>CC</sub> = 2.5V ±0.2V		V <sub>CC</sub> = 3.3V ±0.3V		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f <sub>max</sub>							150		180	—	180	—	ns
t <sub>pd</sub>	CLK	xQx					4.5	—	3.1	—	2.7		
t <sub>en</sub>	$\overline{OE}$	xQx					5.3	—	4.5	—	3.9		
t <sub>dis</sub>	$\overline{OE}$	xQx					5.6	—	3.6	—	3.4		
t <sub>SK(o)</sub> Output Skew <sup>(1)</sup>							0.5	—	0.5	—	0.5		
t <sub>SK(b)</sub> Output Skew <sup>(1)</sup>							0.3	—	0.3	—	0.3		

**Note:**

- This is the skew between any two outputs of the same package, and switching in the same direction.  
 For t<sub>SK(o)</sub> Output 1 and Output 2 are any two outputs. For t<sub>SK(b)</sub> Output 1 and Output 2 are in the same bank.

### Operating Characteristics, T<sub>A</sub> = 25°C

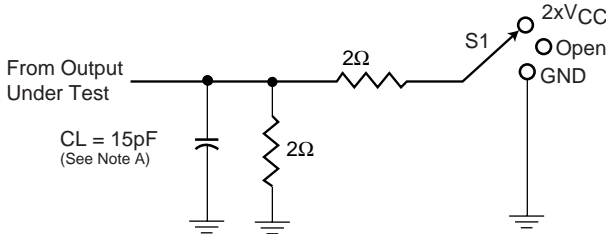
Parameters		Test Conditions	V <sub>CC</sub> = 1.8V ±0.15V	V <sub>CC</sub> = 2.5V ±0.2V	V <sub>CC</sub> = 3.3V ±0.3V	Units
			Typical	Typical	Typical	
C <sub>pd</sub> Power Dissipation Capacitance	Output Enabled	C <sub>L</sub> = 0pF, f = 10 MHz Four outputs switching	84	95	110	pF
	Outputs Disabled		48	55	63	



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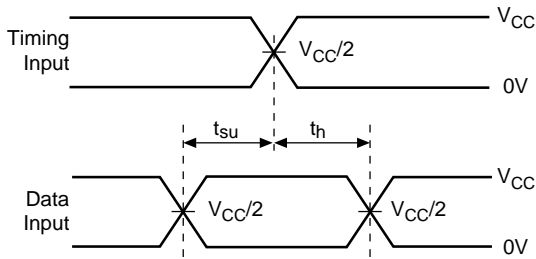
**PARAMETER MEASUREMENT INFORMATION**

$V_{CC} = 1.2V$  and  $1.5V \pm 0.1V$

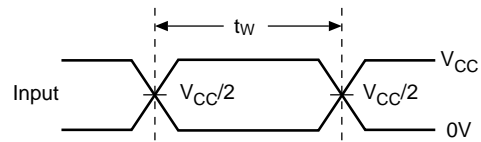


**Load Circuit**

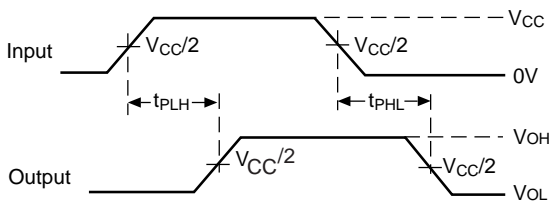
Test	S1
$t_{pd}$ $t_{PLZ}/t_{PZL}$ $t_{PHZ}/t_{PZH}$	Open $2 \times V_{CC}$ GND



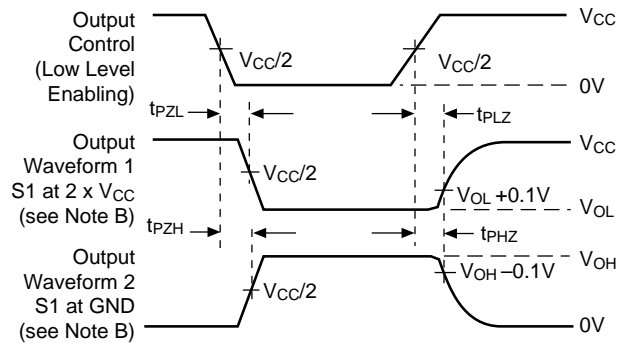
**Voltage Waveforms**  
**Setup and Hold Times**



**Voltage Waveforms**  
**Pulse Duration**



**Voltage Waveforms**  
**Propagation Delay Times**



**Voltage Waveforms**  
**Enable and Disable Times**

**Figure 1. Load Circuit and Voltage Waveforms**

**Notes:**

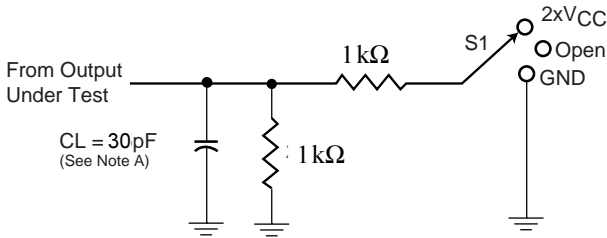
- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input impulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50\Omega$ ,  $t_R \leq 2.0ns$ ,  $t_F \leq 2.0ns$ .
- D. The outputs are measured one at a time with one transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$
- G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$



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**Driver with 3-State Outputs**

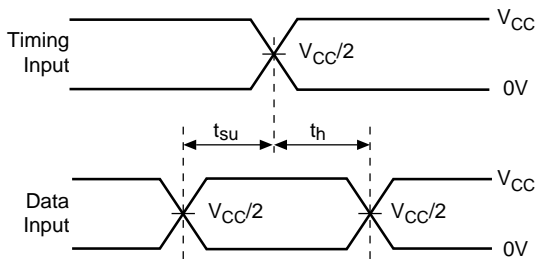
**PARAMETER MEASUREMENT INFORMATION**

**V<sub>CC</sub> = 1.8V ±0.15V**

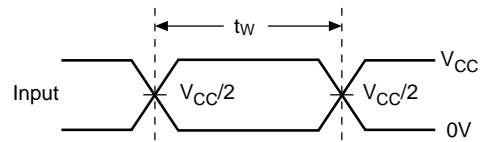


**Load Circuit**

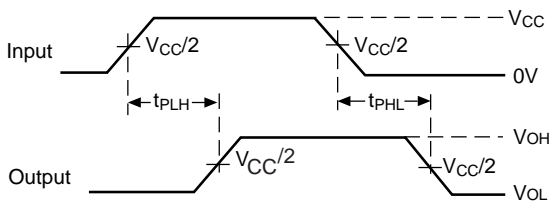
Test	S1
t <sub>pd</sub> t <sub>PLZ</sub> /t <sub>PZL</sub> t <sub>PHZ</sub> /t <sub>PZH</sub>	Open 2 x V <sub>CC</sub> GND



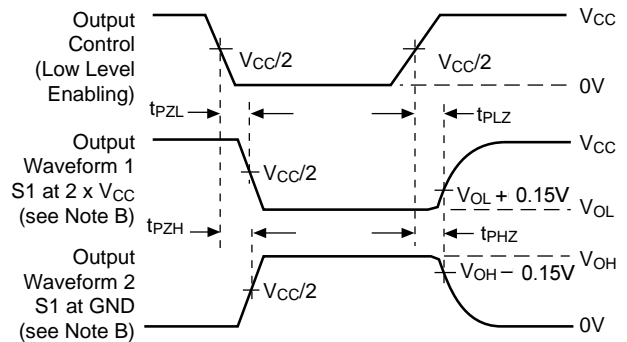
**Voltage Waveforms**  
**Setup and Hold Times**



**Voltage Waveforms**  
**Pulse Duration**



**Voltage Waveforms**  
**Propagation Delay Times**



**Voltage Waveforms**  
**Enable and Disable Times**

**Figure 2. Load Circuit and Voltage Waveforms**

**Notes:**

- A. C<sub>L</sub> includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input impulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50Ω, t<sub>R</sub> ≤ 2.0ns, t<sub>F</sub> ≤ 2.0ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>
- F. t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>
- G. t<sub>PLH</sub> and t<sub>PHL</sub> are the same as t<sub>pd</sub>

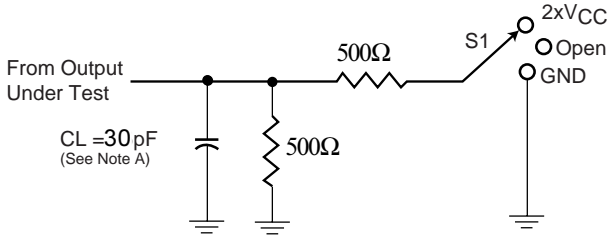




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**Driver with 3-State Outputs**

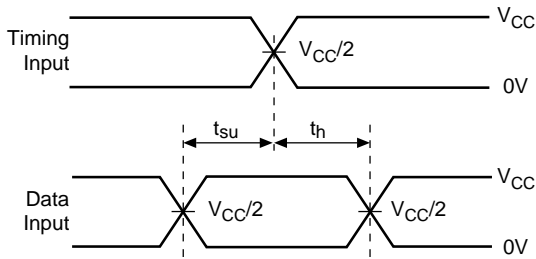
**PARAMETER MEASUREMENT INFORMATION**

$V_{CC} = 2.5V \pm 0.2V$

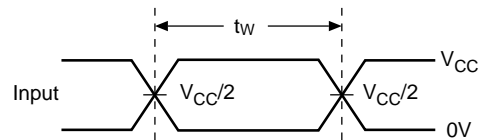


**Load Circuit**

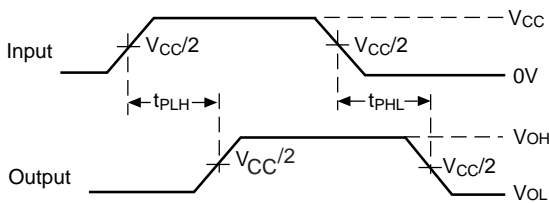
Test	S1
$t_{pd}$ $t_{PLZ}/t_{PZL}$ $t_{PHZ}/t_{PHL}$	Open $2 \times V_{CC}$ GND



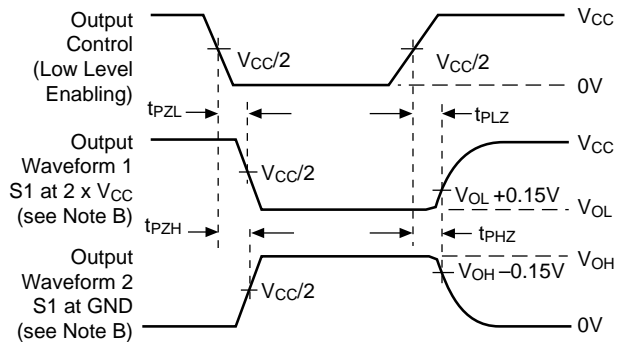
**Voltage Waveforms**  
**Setup and Hold Times**



**Voltage Waveforms**  
**Pulse Duration**



**Voltage Waveforms**  
**Propagation Delay Times**



**Voltage Waveforms**  
**Enable and Disable Times**

**Figure 3. Load Circuit and Voltage Waveforms**

**Notes:**

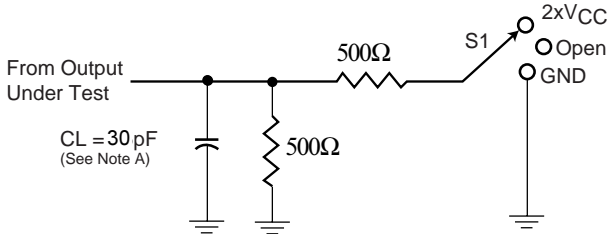
- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input impulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50\Omega$ ,  $t_R \leq 2.0\text{ns}$ ,  $t_F \leq 2.0\text{ns}$ .
- D. The outputs are measured one at a time with one transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$
- G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$



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**Driver with 3-State Outputs**

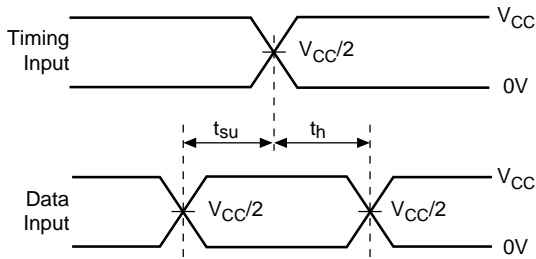
**PARAMETER MEASUREMENT INFORMATION**

$V_{CC} = 3.3V \pm 0.3V$

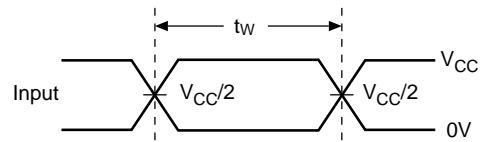


**Load Circuit**

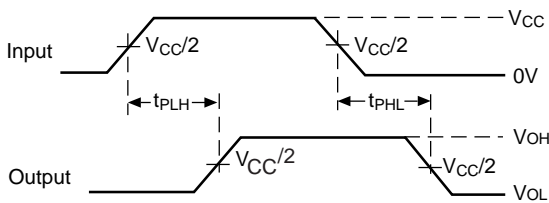
Test	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



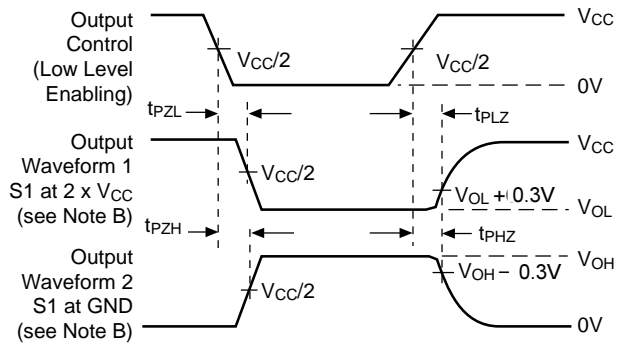
**Voltage Waveforms**  
**Setup and Hold Times**



**Voltage Waveforms**  
**Pulse Duration**



**Voltage Waveforms**  
**Propagation Delay Times**



**Voltage Waveforms**  
**Enable and Disable Times**

**Figure 4. Load Circuit and Voltage Waveforms**

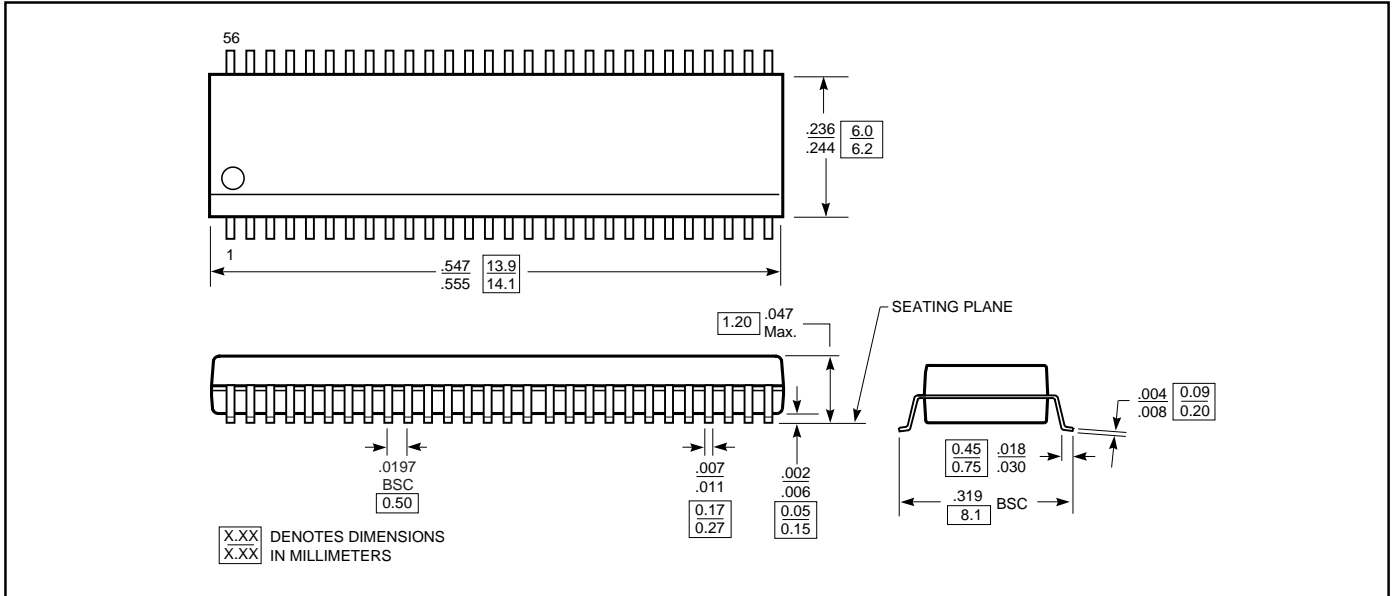
**Notes:**

- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input impulses are supplied by generators having the following characteristics: PRR  $\leq 10$  MHz,  $Z_O = 50\Omega$ ,  $t_R \leq 2.0ns$ ,  $t_F \leq 2.0ns$ .
- D. The outputs are measured one at a time with one transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$
- G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$

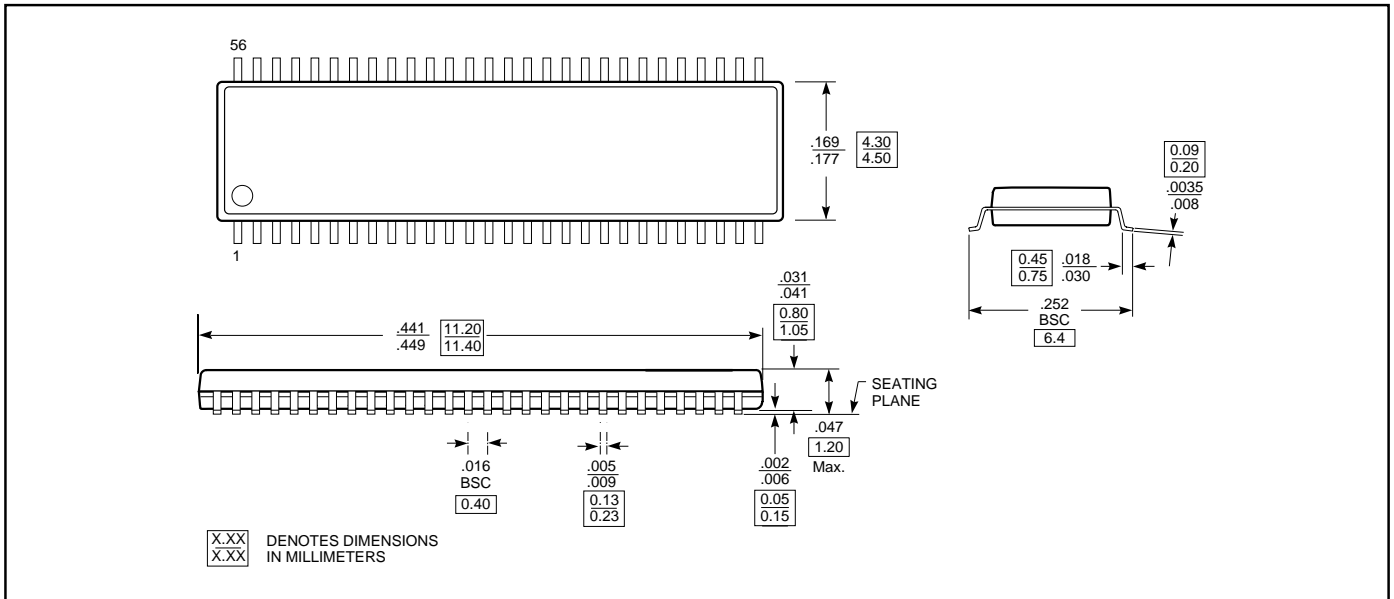


**PI74AVC+16345**  
**2.5V, Registered 1-Bit to 4-Bit Address**  
**Driver with 3-State Outputs**

**56-pin TSSOP (A) Package**



**56-pin TVSOP (K) Package**



**Ordering Information**

Ordering Data	Description
PI74AVC+16345A	56-pin, 240-mil wide plastic TSSOP
PI74AVC+16345K	56-pin, 173-mil wide plastic TVSOP

**Pericom Semiconductor Corporation**

2380 Bering Drive • San Jose, CA 95131 • 1-800-435-2336 • Fax (408) 435-1100 • http://www.pericom.com