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[Microchip Technology](#)
[MX575ABD100M000](#)

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sales@integrated-circuit.com



MX575ABD100M000

Ultra-low Jitter 100MHz HCSL XO

ClockWorks™ FUSION

General Description

The MX575ABD100M000 is an ultra-low phase jitter XO with HCSL output optimized for high line rate applications.

Applications

- PCI-Express
- Storage

Absolute Maximum Ratings

Supply Voltage (VIN).....	+3.6V
Lead Temperature (soldering, 10s).....	260°C
Storage Temperature (T _s).....	125°C
ESD Rating (HBM).....	2kV

Electrical Characteristics

VDD = 2.5V ±5% or 3.3V ±10%, -40°C to +85°C, outputs terminated with 50 Ohms to VSS.¹

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
IDD	Supply Current				95	mA
F0	Center Frequency			100		MHz
	Frequency Stability	Note 2			±50	ppm
∅j	Phase Noise	Integration Range (12kHz to 20MHz) Integration Range (1.875MHz to 20MHz)		220 100		fsRMS
Tstart	Start-Up Time				20	ms
TR/TF	Rise/Fall time		300			ps
	Duty Cycle		45		55	%
VOH	Output High Voltage	HCSL output levels	640	700	850	mV
VOL	Output Low Voltage	HCSL output levels	-150	0		mV
VOVS	Max Output Including Overshoot				VOH + 0.3	V
VUDS	Min Output Including Undershoot		VOL - 0.3			V
VRB	Ringback Voltage		0.2			V
VOX	Absolute Crossing Point		250	450	550	mV
Vswing	Peak to Peak Output Voltage Swing		640	700	950	mV

Notes:

1. Guaranteed after thermal equilibrium.
2. Inclusive of initial accuracy, temperature drift, aging, shock, vibration from -40°C to +85°C.

ClockWorks is a registered trademark of Micrel, Inc

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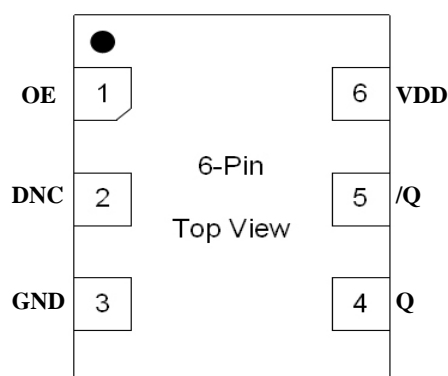
MX575ABD100M000

Ordering Information

Ordering Part Number	Marking Line 1	Marking Line 3	Shipping	Package
MX575ABD100M000	MX575AB	D100M000	Tube	6-Pin 7mm x 5mm LGA
MX575ABD100M000 TR	MX575AB	D100M000	Tape and Reel	6-Pin 7mm x 5mm LGA

Devices are Green and RoHS compliant. Sample material may have only a partial top mark.

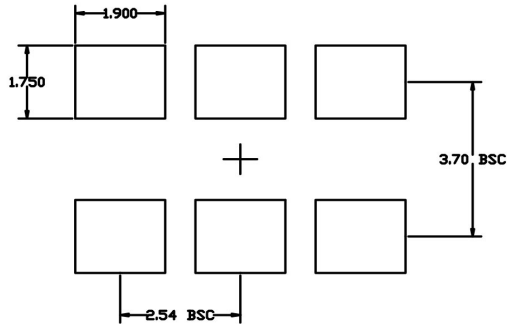
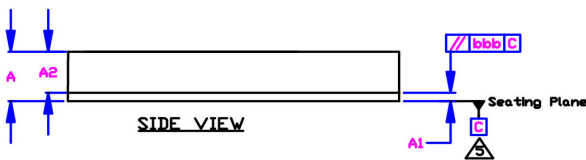
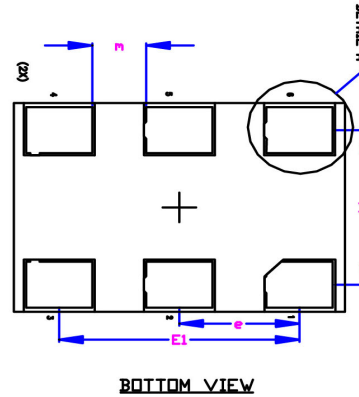
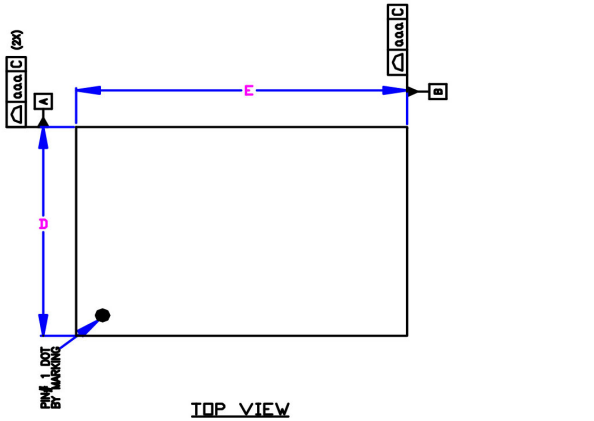
Pin Configuration



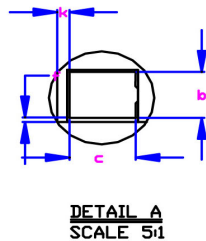
Pin Description

Pin Number	Pin Name	Pin Type	Pin Level	Pin Function
1	OE	I, SE	LVC MOS	Output Enable, disables output to tri-state, 0 = Disabled, 1 = Enabled, 50k Ohms Pull-Up
2	DNC			Make no connection, leave floating.
3	GND	PWR		Power Supply Ground
4, 5	Q, /Q	O, Diff	HCSL	Clock Output Frequency = 100MHz
6	VDD	PWR		Power Supply

Package Information and Recommended Land Pattern for 6-Pin LGA³



Dimensional Tol.	
aaa	0.10
bbb	0.17
Dimensional Ref.	
REF	Min. Nom. Max.
A	1.26 1.33 1.40
A1	0.19 0.23 0.27
A2	1.07 1.10 1.13
D	4.9 5.0 5.1
D1	3.7 BSC
E	6.9 7.0 7.1
E1	5.0 BSC
b	1.05 1.1 1.15
c	1.35 1.4 1.45
e	2.54 BSC
f	0.15 0.18 0.15
k	0.21 0.26 0.31
m	1.09 1.14 1.19
n	36



- Notes**
1. Dimensioning and Tolerancing per ASME Y14.5M-1994.
 2. Dimensions are in millimeters.
 3. 'e' represents the basic LGA pitch
 4. 'n' is the maximum no. of Land for a specified Package.
 5. Package warp shall be 0.151 max.
 6. Substrate base is BT Resin
 7. The Pin#1 corner must be identified on top side only.
 8. Reference Jeced Spec M1-221
 9. Land pattern tolerance is 0.15mm unless otherwise specified

6-Pin LGA (7x5mm)

Note:

3. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

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