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LM5025DMTCX/NOPB

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Datasheet of LM5025DMTCX/NOPB - IC REG CTRLR PWM VM 16TSSOP
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LM5025D Active Clamp Voltage Mode PWM Controller

1 Features

- Internal Start-Up Bias Regulator
- 3-A Compound Main Gate Driver
- Programmable Line Under-Voltage Lockout (UVLO) with Adjustable Hysteresis
- Voltage Mode Control with Feed-Forward
- Adjustable Dual Mode Over-Current Protection
- Programmable Overlap or Deadtime Between the Main and Active Clamp Outputs
- Volt x Second Clamp
- Programmable Soft-Start
- Leading Edge Blanking
- Single Resistor Programmable Oscillator
- Oscillator Up and Down Sync Capability
- Precision 5-V Reference
- Thermal Shutdown

2 Applications

- Server Power Supplies
- 48-V Telecom Power Supplies
- 42-V Automotive Applications
- High-Efficiency DC-to-DC Power Supplies

3 Description

The LM5025D is a functional variant of the LM5025 active clamp PWM controller. The functional differences of the LM5025D are:

- The CS1 and CS2 absolute maximum ratings have been increased to 7 V.
- The CS1 and CS2 current limit thresholds have been increased to 0.5 V.
- The internal CS2 filter discharge device has been disabled and no longer operates each clock cycle.
- The internal V_{CC} and V_{REF} regulators continue to operate when the line UVLO pin is below threshold.

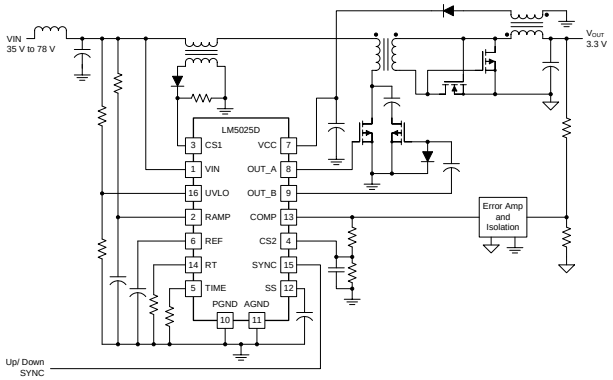
The LM5025D PWM controller contains all of the features necessary to implement power converters utilizing the Active Clamp and Reset technique. With the active clamp technique, higher efficiencies and greater power densities can be realized compared to conventional catch winding or RDC clamp and reset techniques. Two control outputs are provided, the main power switch control (OUT_A) and the active clamp switch control (OUT_B). The two internal compound gate drivers parallel both MOS and Bipolar devices, providing superior gate drive characteristics. This controller is designed for high-speed operation including an oscillator frequency range up to 1 MHz and total PWM and current sense propagation delays less than 100 ns. The LM5025D includes a high-voltage start-up regulator that operates over a wide input range of 13 V to 90 V. Additional features include: Line Under-Voltage Lockout (UVLO), softstart, oscillator UP and DOWN sync capability, precision reference and thermal shutdown.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM5025D	TSSOP (16)	6.60 mm x 5.10 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Diagram



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4 Revision History

DATE	REVISION	NOTES
June, 2015	*	Initial release.

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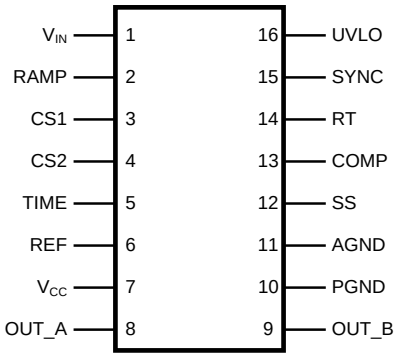
5 Pin Configuration and Functions

PW Package
16-Pin TSSOP
Top View



Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
AGND	11	G	Analog ground. Connect directly to power ground. For the PW package option the exposed pad is electrically connected to AGND.
COMP	13	I	Input to the pulse width modulator. An internal 5-kΩ resistor pull-up is provided on this pin. The external opto-coupler sinks current from COMP to control the PWM duty cycle.
CS1	3	I	Current sense input for cycle-by-cycle limiting. If CS1 exceeds 0.5 V the outputs will go into cycle-by-cycle current limit. CS1 is held low for 50 ns after OUT_A switches high providing leading edge blanking.
CS2	4	I	Current sense input for soft restart. If CS2 exceeds 0.5 V the outputs will be disabled and a softstart commenced. The soft-start capacitor will be fully discharged and then released with a pull-up current of 1 µA. After the first output pulse (when SS = 1 V), the SS charge current will revert back to 20 µA.
EP	-	-	Exposed pad, underside of the PW package option. Internally bonded to the die substrate. Connect to GND potential for low thermal impedance.
OUT_A	8	O	Main output driver. Output of the main switch PWM output gate driver. Output capability of 3-A peak sink current.
OUT_B	9	O	Active Clamp output driver. Output of the active clamp switch gate driver. Capable of 1.25-A peak sink current.
PGND	10	G	Power ground. Connect directly to analog ground.
RAMP	2	I	Modulator ramp signal. An external RC circuit from V_{IN} sets the ramp slope. This pin is discharged at the conclusion of every cycle by an internal FET, initiated by either the internal clock or the V x Sec clamp comparator.
REF	6	O	Precision 5-V reference output. Maximum output current: 10 mA locally decouple with a 0.1-µF capacitor. Reference stays low until the V_{CC} UV comparator is satisfied.
RT	14	I	Oscillator timing resistor pin. An external resistor connected from RT to ground sets the internal oscillator frequency.
SS	12	I	Soft-start control. An external capacitor and an internal 20-µA current source set the softstart ramp. The SS current source is reduced to 1 µA initially following a CS2 over-current event or an over temperature event.
SYNC	15	I	Oscillator UP/DOWN synchronization input. The internal oscillator can be synchronized to an external clock with a frequency 20% lower than the internal oscillator's free running frequency. There is no constraint on the maximum sync frequency.
TIME	5	I	Output overlap/deadtime control. An external resistor (R_{SET}) sets either the overlap time or dead time for the active clamp output. An R_{SET} resistor connected between TIME and GND produces in-phase OUT_A and OUT_B pulses with overlap. An R_{SET} resistor connected between TIME and REF produces out-of-phase OUT_A and OUT_B pulses with deadtime.
UVLO	16	I	Line Under-Voltage shutdown. An external voltage divider from the power source sets the shutdown comparator levels. The comparator threshold is 2.5 V. Hysteresis is set by an internal current source (20 µA) that is switched on or off as the UVLO pin potential crosses the 2.5 V threshold.
VCC	7	P	Output from the internal high voltage start-up regulator. The V_{CC} voltage is regulated to 7.6 V. If an auxiliary winding raises the voltage on this pin above the regulation setpoint, the internal start-up regulator will shutdown, reducing the device power dissipation.
VIN	1	I	Source input voltage. Input to start-up regulator. Input range 13 V to 90 V, with transient capability to 105 V.

(1) P = Power, G = Ground, I = Input, O = Output, I/O = Input/Output

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6 Specifications

6.1 Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)[2]

		MIN	MAX	UNIT
V_{IN} to GND		–0.3	105	V
V_{CC} to GND		–0.3	16	V
CS1, CS2 to GND		–0.3	7	V
All other inputs to GND		–0.3	7	V
Junction Temperature			150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(2) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge[1]	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[2]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[3]	±500	

(1) For detailed information on soldering plastic TSSOP package, refer to the Packaging Data Book.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input Voltage	13		90	V
	External Voltage Applied to V_{CC}	8		15	V
	Operating Junction Temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC[1]		TSSOP 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	95.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	27.0	
$R_{\theta JB}$	Junction-to-board thermal resistance	41.0	
ψ_{JT}	Junction-to-top characterization parameter	1.1	
ψ_{JB}	Junction-to-board characterization parameter	40.4	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Specifications with standard typeface are for T_J = 25°C, and all MIN and MAX values apply over full Operating Junction Temperature range. V_{IN} = 48V, V_{CC} = 10V, RT = 31.3kΩ, R_{SET} = 27.4kΩ) unless otherwise stated (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STARTUP REGULATOR						
V_{CC} Reg	V_{CC} regulation	No load	7.3	7.6	7.9	V
	V_{CC} current limit	(2)	20	25		mA
I-V_{IN}	Startup regulator leakage (external V_{CC} supply)	V_{IN} = 100 V		165	500	µA
V_{CC} SUPPLY						
	V_{CC} under-voltage lockout voltage (positive going V_{CC})		V_{CC} Reg – 220mV	V_{CC} Reg - 120mV		V
	V_{CC} under-voltage hysteresis		1.0	1.5	2.0	V
	V_{CC} supply current (I_{CC})	C_{GATE} = 0			4.2	mA
REFERENCE SUPPLY						
V_{REF}	REF voltage	I_{REF} = 0 mA	4.85	5	5.15	V
	REF voltage regulation	I_{REF} = 0 mA to 10 mA		25	50	mV
	REF current limit		10	20		mA
CURRENT LIMIT						
CS1 Prop	CS1 delay to output	CS1 step from 0 V to 0.6 V, Time to onset of OUT transition (90%), C_{GATE} = 0		40		ns
CS2 Prop	CS2 delay to output	CS2 step from 0 V to 0.6 V, Time to onset of OUT transition (90%), C_{GATE} = 0		50		ns
	Cycle-by-cycle threshold voltage (CS1)		0.45	0.5	0.55	V
	Cycle skip threshold voltage (CS2)	Resets SS capacitor; auto restart	0.45	0.5	0.55	V
	Leading edge blanking time (CS1)			50		ns
	CS1 sink impedance (clocked)	CS1 = 0.4 V		30	50	Ω
	CS1 sink impedance (post fault discharge)	CS1 = 0.6 V		15	30	Ω
	CS2 sink impedance (post fault discharge)	CS2 = 0.6 V		55	95	Ω
	CS1 and CS2 leakage current	CS = CS threshold – 100 mV			1	µA
SOFT-START						
	Soft-start current source normal		17	22	27	µA
	Soft-start current source following a CS2 event		0.5	1	1.5	µA
OSCILLATOR						
	Frequency1	T_A = 25°C, T_J = T_{LOW} to T_{HIGH}	180 175	200	220 225	kHz
	Frequency2	RT = 10.4 kΩ	510	580	650	kHz
	Sync threshold			2		V
	Min sync pulse width				100	ns
	Sync frequency range		160			kHz

(1) All electrical characteristics having room temperature limits are tested during production with T_A = T_J = 25°C. All hot and cold limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) Device thermal limitations may limit usable range.

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Electrical Characteristics (continued)

Specifications with standard typeface are for T_J = 25°C, and all MIN and MAX values apply over full Operating Junction Temperature range. V_{IN} = 48V, V_{CC} = 10V, RT = 31.3kΩ, R_{SET} = 27.4kΩ) unless otherwise stated (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PWM COMPARATOR						
	Delay to output	COMP step 5 V to 0 V, Time to onset of OUT_A transition low		40		ns
	Duty cycle range		0		80	%
	COMP to PWM offset		0.7	1	1.3	V
	COMP open circuit voltage		4.3		5.9	V
	COMP short circuit current	COMP = 0 V	0.6	1	1.4	mA
VOLT x SECOND CLAMP						
	Ramp clamp level	Delta RAMP measured from onset of OUT_A to ramp peak, COMP = 5 V	2.4	2.5	2.6	V
UVLO SHUTDOWN						
	Undervoltage shutdown threshold		2.44	2.5	2.56	V
	Undervoltage shutdown hysteresis		16	20	24	µA
OUTPUT SECTION						
	OUT_A high saturation	MOS device at I_{OUT} = –10 mA		5	10	Ω
	OUTPUT_A peak current sink	Bipolar device at Vcc/2		3		A
	OUT_A low saturation	MOS device at I_{OUT} = 10 mA		6	9	Ω
	OUTPUT_A rise time	C_{GATE} = 2.2 nF		20		ns
	OUTPUT_A fall time	C_{GATE} = 2.2 nF		15		ns
	OUT_B high saturation	MOS device at I_{OUT} = –10 mA		10	20	Ω
	OUTPUT_B peak current sink	Bipolar device at V_{CC}/2		1		A
	OUT_B low saturation	MOS device at I_{OUT} = 10 mA		12	18	Ω
	OUTPUT_B rise time	C_{GATE} = 1 nF		20		ns
	OUTPUT_B fall time	C_{GATE} = 1 nF		15		ns
OUTPUT TIMING CONTROL						
	Overlap time	R_{SET} = 38 kΩ connected to GND, 50% to 50% transitions	75	105	135	ns
	Deadtime	R_{SET} = 29.5 kΩ connected to REF, 50% to 50% transitions	75	105	135	ns
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown threshold			165		°C
	Thermal shutdown hysteresis			25		°C

6.6 Typical Performance Characteristics

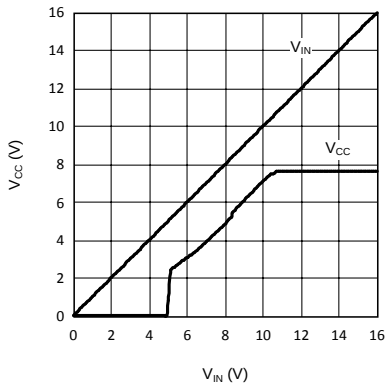

Figure 1. V_{CC} Regulator Start-up Characteristics, V_{CC} vs V_{IN}

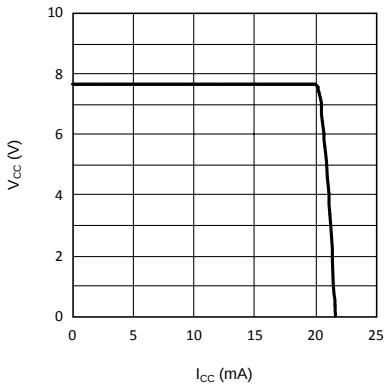

Figure 2. V_{CC} vs I_{CC}

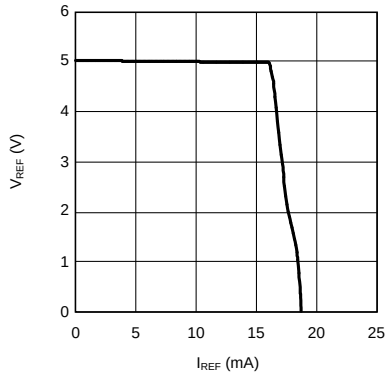

Figure 3. V_{REF} vs I_{REF}

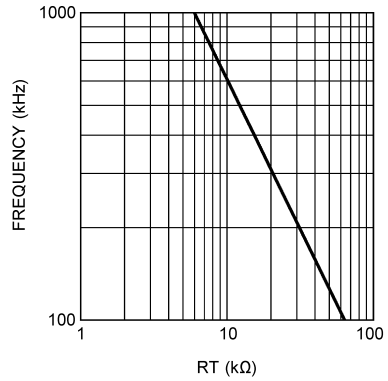

Figure 4. Oscillator Frequency vs RT

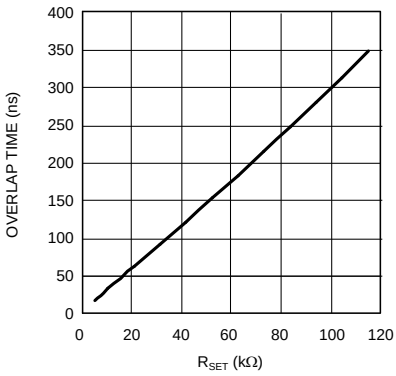

Figure 5. Overlap Time vs R_{SET}

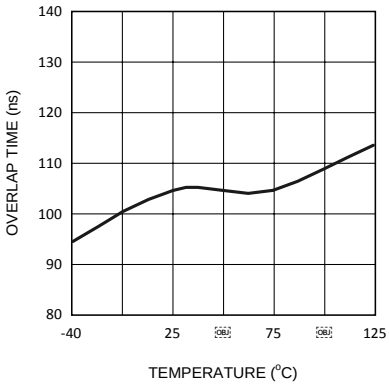

Figure 6. Overlap Time vs Temperature R_{SET} = 38 kΩ

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Typical Performance Characteristics (continued)

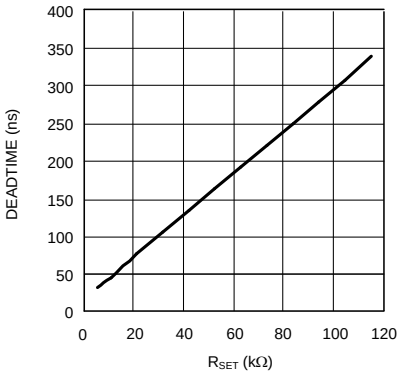

Figure 7. Dead Time vs R_{SET}

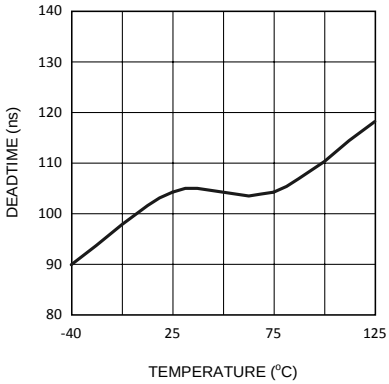

Figure 8. Dead Time vs Temperature R_{SET} = 29.5 kΩ

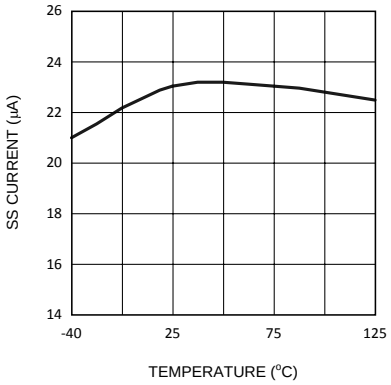

Figure 9. SS Pin Current vs Temperature

7 Detailed Description

7.1 Overview

The LM5025D is a functional variant of the LM5025 active clamp PWM controller. The functional differences of the LM5025D are:

- The CS1 and CS2 absolute maximum ratings have been increased to 7 V.
- The CS1 and CS2 current limit thresholds have been increased to 0.5 V.
- The internal CS2 filter discharge device has been disabled and no longer operates each clock cycle.
- The internal V_{CC} and V_{REF} regulators continue to operate when the line UVLO pin is below threshold.

The LM5025D PWM controller contains all of the features necessary to implement power converters utilizing the active clamp reset techniques. The device can be configured to control either a P-Channel clamp switch or an N-Channel clamp switch. With the active clamp technique higher efficiencies and greater power densities can be realized compared to conventional catch winding or RDC clamp / reset techniques. Two control outputs are provided, the main power switch control (OUT_A) and the active clamp switch control (OUT_B). The active clamp output can be configured for either a specified overlap time (for P-Channel switch applications) or a specified dead time (for N_Channel applications). The two internal compound gate drivers parallel both MOS and Bipolar devices, providing superior gate drive characteristics. This controller is designed for high-speed operation including an oscillator frequency range up to 1 MHz and total PWM and current sense propagation delays less than 100 ns. The LM5025D includes a high-voltage, start-up regulator that operates over a wide input range of 13 V to 90 V. Additional features include: Line Under-Voltage Lockout (UVLO), softstart, oscillator UP/DOWN sync capability, precision reference and thermal shutdown.

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7.2 Functional Block Diagram

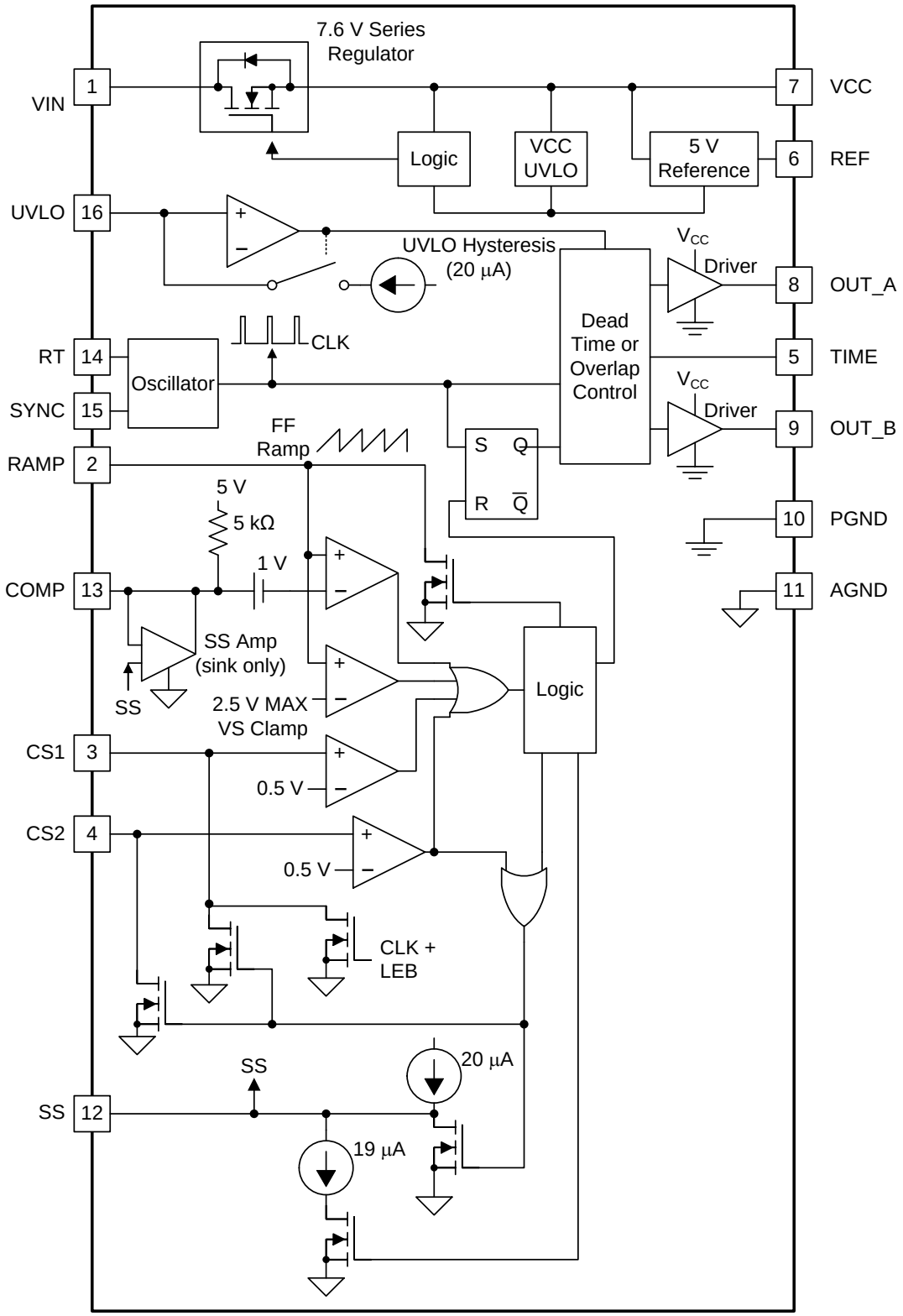

Figure 10. Simplified Block Diagram

7.3 Feature Description

7.3.1 High Voltage Start-Up Regulator

The LM5025D contains an internal high voltage start-up regulator that allows the input pin (V_{IN}) to be connected directly to the line voltage. The regulator output is internally current limited to 20 mA. When power is applied, the regulator is enabled and sources current into an external capacitor connected to the V_{CC} pin. The recommended capacitance range for the V_{CC} regulator is 0.1 µF to 100 µF. When the voltage on the V_{CC} pin reaches the regulation point of 7.6 V and the internal voltage reference (REF) reaches its regulation point of 5 V, the controller outputs are enabled. The outputs remain enabled until V_{CC} falls below 6.2 V or the line Under-Voltage Lock Out detector indicates that V_{IN} is out of range. In typical applications, an auxiliary transformer winding is connected through a diode to the V_{CC} pin. This winding must raise the V_{CC} voltage above 8 V to shut off the internal start-up regulator. Powering V_{CC} from an auxiliary winding improves efficiency while reducing the controller power dissipation.

When the converter auxiliary winding is inactive, external current draw on the V_{CC} line should be limited so the power dissipated in the start-up regulator does not exceed the maximum power dissipation of the controller.

An external start-up regulator or other bias rail can be used instead of the internal start-up regulator by connecting the V_{CC} and the V_{IN} pins together and feeding the external bias voltage into the two pins.

7.3.2 Line Under-Voltage Detector

The LM5025D contains a line Under-Voltage Lock Out (UVLO) circuit. An external set-point voltage divider from V_{IN} to GND, sets the operational range of the converter. The divider must be designed such that the voltage at the UVLO pin is greater than 2.5 V when V_{IN} is in the desired operating range. If the undervoltage threshold is not met, both outputs are disabled, all other functions of the controller remain active. UVLO hysteresis is accomplished with an internal 20-µA current source that is switched on or off into the impedance of the set-point divider. When the UVLO threshold is exceeded, the current source is activated to instantly raise the voltage at the UVLO pin. When the UVLO pin voltage falls below the 2.5 V threshold, the current source is turned off causing the voltage at the UVLO pin to fall. The UVLO pin can also be used to implement a remote enable / disable function. Pulling the UVLO pin below the 2.5 V threshold disables the PWM outputs.

7.3.3 PWM Outputs

The relative phase of the main (OUT_A) and active clamp outputs (OUT_B) can be configured for the specific application. For active clamp configurations utilizing a ground referenced P-Channel clamp switch, the two outputs should be in phase with the active clamp output overlapping the main output. For active clamp configurations utilizing a high-side, N-Channel switch, the active clamp output should be out of phase with main output and there should be a dead time between the two gate drive pulses. A distinguishing feature of the LM5025D is the ability to accurately configure either dead time (both off) or overlap time (both on) of the gate driver outputs. The overlap / deadtime magnitude is controlled by the resistor value connected to the TIME pin of the controller. The opposite end of the resistor can be connected to either REF for deadtime control or GND for overlap control. The internal configuration detector senses the connection and configures the phase relationship of the main and active clamp outputs.

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Feature Description (continued)

7.3.4 Compound Gate Drivers

The LM5025D contains two unique compound gate drivers, which parallel both MOS and Bipolar devices to provide high drive current throughout the entire switching event. The Bipolar device provides most of the drive current capability and provides a relatively constant sink current which is ideal for driving large power MOSFETs. As the switching event nears conclusion and the Bipolar device saturates, the internal MOS device continues to provide a low impedance to compete the switching event.

During turn-off at the Miller plateau region, typically around 2 V to 3 V, is where gate-driver current capability is needed most. The resistive characteristics of all MOS gate drivers are adequate for turn-on since the supply to output voltage differential is fairly large at the Miller region. During turn-off however, the voltage differential is small and the current source characteristic of the Bipolar gate driver is beneficial to provide fast drive capability.

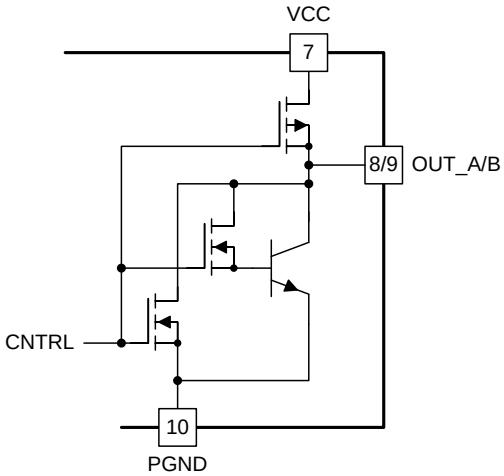

Figure 11. Compound Gate Drivers

7.3.5 PWM Comparator

The PWM comparator compares the ramp signal (RAMP) to the loop error signal (COMP). This comparator is optimized for speed in order to achieve minimum controllable duty cycles. The internal 5-kΩ pull-up resistor, connected between the internal 5-V reference and COMP, can be used as the pull-up for an optocoupler. The comparator polarity is such that 0 V on the COMP pin produces a zero duty cycle on both gate driver outputs.

7.3.6 Volt Second Clamp

The Volt x Second Clamp comparator compares the ramp signal (RAMP) to a fixed 2.5-V reference. By proper selection of RFF and CFF, the maximum ON time of the main switch can be set to the desired duration. The ON time set by Volt x Second Clamp varies inversely with the line voltage because the RAMP capacitor is charged by a resistor connected to V_{IN} while the threshold of the clamp is a fixed voltage (2.5 V).

The C_{FF} ramp capacitor is discharged at the conclusion of every cycle by an internal discharge switch controlled by either the internal clock or by the V x S Clamp comparator, whichever event occurs first.

Feature Description (continued)

7.3.7 Current Limit

The LM5025D contains two modes of over-current protection. If the sense voltage at the CS1 input exceeds 0.5 V the present power cycle is terminated (cycle-by-cycle current limit). If the sense voltage at the CS2 input exceeds 0.5 V, the controller terminates the present cycle, discharge the softstart capacitor and reduce the softstart current source to 1 µA. The softstart (SS) capacitor is released after being fully discharged and slowly charges with a 1-µA current source. When the voltage at the SS pin reaches approximately 1 V, the PWM comparator produces the first output pulse at OUT_A. After the first pulse occurs, the softstart current source reverts to the normal 20-µA level. Fully discharging and then slowly charging the SS capacitor protects a continuously over-loaded converter with a low duty-cycle hiccup mode.

These two modes of over-current protection allow the user great flexibility to configure the system behavior in over-load conditions. If it is desired for the system to act as a current source during an over-load, then the CS1 cycle-by-cycle current limiting should be used. In this case the current sense signal should be applied to the CS1 input and the CS2 input should be grounded. If during an overload condition it is desired for the system to briefly shutdown, followed by softstart retry, then the CS2 hiccup current limiting mode should be used. In this case the current sense signal should be applied to the CS2 input and the CS1 input should be grounded. This shutdown / soft-start retry repeats indefinitely while the over-load condition remains. The hiccup mode will greatly reduce the thermal stresses to the system during heavy overloads. The cycle-by-cycle mode has higher system thermal dissipations during heavy overloads, but provides the advantage of continuous operation for short duration overload conditions.

It is possible to utilize both over-current modes concurrently, whereby slight overload conditions activate the CS1 cycle-by-cycle mode while more severe overloading activates the CS2 hiccup mode. Generally the CS1 input is configured to monitor the main switch FET current of each cycle. The CS2 input can be configured in several different ways depending upon the system requirements.

- The CS2 input can also be set to monitor the main switch FET current except scaled to a higher threshold than CS1.
- An external over-current timer can be configured which trips after a pre-determined over-current time, driving the CS2 input high, initiating a hiccup event.
- In a closed loop voltage regulation system, the COMP input rises to saturation when the cycle-by-cycle current limit is active. An external filter/delay timer and voltage divider can be configured between the COMP pin and the CS2 pin to scale and delay the COMP voltage. If the CS2 pin voltage reaches 0.5 V a hiccup event initiates.

A small RC filter, located near the controller, is recommended for each of the CS pins. The CS1 input has an internal FET which discharges the current sense filter capacitor at the conclusion of every cycle, to improve dynamic performance. This same FET remains on an additional 50 ns at the start of each main switch cycle to attenuate the leading edge spike in the current sense signal. The CS2 discharge FET only operates following a CS2 event, UVLO and thermal shutdown.

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Feature Description (continued)

The LM5025D CS comparators are very fast and may respond to short duration noise pulses. Layout considerations are critical for the current sense filter and sense resistor. The capacitor associated with the CS filter must be placed very close to the device and connected directly to the pins of the device (CS and GND). If a current sense transformer is used, both leads of the transformer secondary should be routed to the filter network , which should be located close to the device. If a sense resistor in the source of the main switch MOSFET is used for current sensing, a low inductance type of resistor is required. When designing with a current sense resistor, all of the noise sensitive low power ground connections should be connected together near the device GND and a single connection should be made to the power ground (sense resistor ground point).

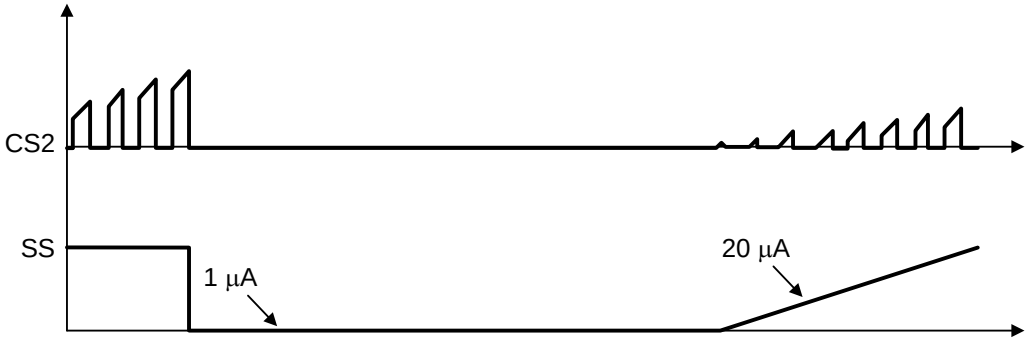

Figure 12. Current Limit

Feature Description (continued)

7.3.8 Oscillator and Sync Capability

The LM5025D oscillator is set by a single external resistor connected between the RT pin and GND. The RT resistor should be located very close to the device and connected directly to the pins of the device (RT and GND).

A unique feature of LM5025D is the ability to synchronize the oscillator to an external clock with a frequency that is either higher or lower than the frequency of the internal oscillator. The lower frequency sync frequency range is 80% of the free running internal oscillator frequency. There is no constraint on the maximum SYNC frequency. A minimum pulse width of 100 ns is required for the synchronization clock . If the synchronization feature is not required, the SYNC pin should be connected to GND to prevent any abnormal interference . The internal oscillator can be completely disabled by connecting the RT pin to REF. Once disabled, the sync signal acts directly as the master clock for the controller. Both the frequency and the maximum duty cycle of the PWM controller can be controlled by the SYNC signal (within the limitations of the Volt x Second Clamp). The maximum duty cycle (D) is (1-D) of the SYNC signal.

7.3.9 Feed-Forward Ramp

An external resistor (R_{FF}) and capacitor (C_{FF}) connected to V_{IN} and GND are required to create the PWM ramp signal. The slope of the signal at the RAMP pin varies in proportion to the input line voltage. This varying slope provides line feedforward information necessary to improve line transient response with voltage mode control. The RAMP signal is compared to the error signal at the COMP pin by the pulse width modulator comparator to control the duty cycle of the main switch output. The volt second clamp comparator also monitors the RAMP pin and if the ramp amplitude exceeds 2.5 V the present cycle is terminated. The ramp signal is reset to GND at the end of each cycle by either the internal clock or the volt second comparator, whichever occurs first.

7.3.10 Soft-Start

The softstart feature allows the power converter to gradually reach the initial steady state operating point, thus reducing start-up stresses and surges. At power on, a 20-µA current is sourced out of the softstart pin (SS) into an external capacitor. The capacitor voltage ramps up slowly and limits the COMP pin voltage and therefore the PWM duty cycle. In the event of a fault as determined by V_{CC} undervoltage, line undervoltage (UVLO) or second level current limit, the output gate drivers are disabled and the softstart capacitor is fully discharged. When the fault condition is no longer present a softstart sequence is initiated. Following a second level current limit detection (CS2), the softstart current source is reduced to 1 µA until the first output pulse is generated by the PWM comparator. The current source returns to the nominal 20 µA level after the first output pulse (~1 V at the SS pin).

7.3.11 Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event the maximum junction temperature is exceeded. When activated, typically at 165°C, the controller is forced into a low-power standby state with the output drivers and the bias regulator disabled. The device restarts after the thermal hysteresis (typically 25°C). During a restart after thermal shutdown, the softstart capacitor is fully discharged and then charged in the low current mode (1 µA) similar to a second level current limit event. The thermal protection feature is provided to prevent catastrophic failures from accidental device overheating.

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7.4 Device Functional Modes

The LM5025D active clamp voltage mode PWM controller has six functional modes. The modes transition diagram is shown below.

- UVLO Mode
- Soft-Start Mode
- Normal Operation Mode
- Cycle-by-Cycle Current Limit Mode
- Hiccup Mode
- Thermal Shut Down Mode

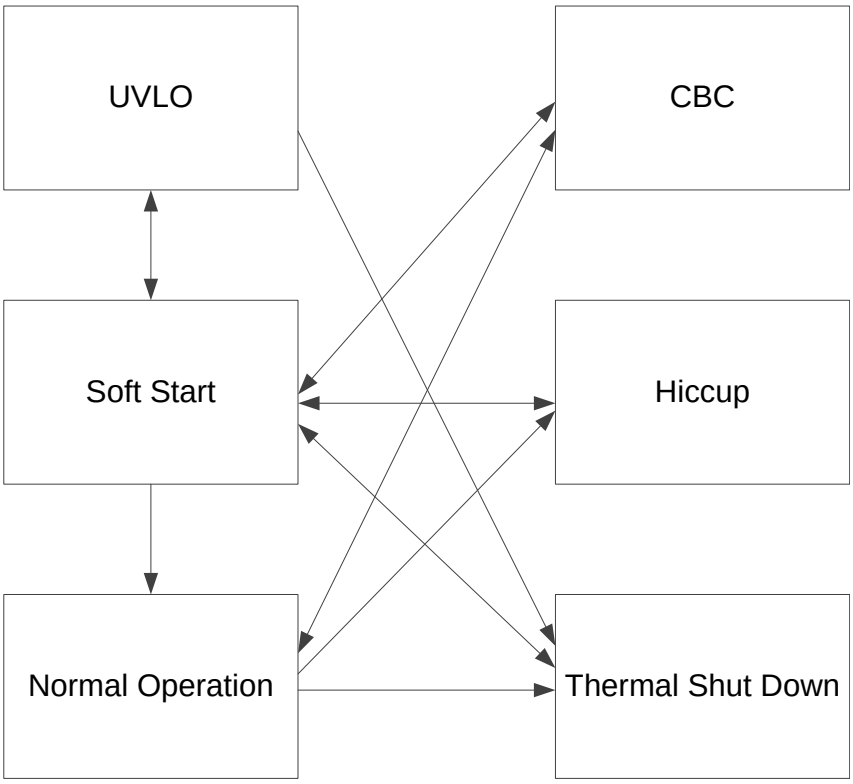

Figure 13. Functional Mode Transition Diagram

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM5025D PWM controller contains all of the features necessary to implement power converters utilizing the Active Clamp and Reset technique. This section provides design guidance for a typical active clamp forward converter design. Design requirements and detailed design procedure are described in Design Requirements and Application Curves. Application curves are given in Section 8.2.3. An actual application schematic of a 36-V to 78-V input, 3.3-V, 30-A output active clamp forward converter is also provided.

8.2 Typical Application

Figure 14 shows a simplified schematic of an active clamp forward power converter.

Power converters based on the Forward topology offer high efficiency and good power handling capability in applications up to several hundred Watts. The operation of the transformer in a forward topology does not inherently self-reset each power switching cycle, a mechanism to reset the transformer is required. The active clamp reset mechanism is presently finding extensive use in medium level power converters in the 50 W to 200 W range.

The Forward converter is derived from the Buck topology family, employing a single modulating power switch. The main difference between the topologies is the forward topology employs a transformer to provide input/output ground isolation and a step down or step up function.

Each cycle, the main primary switch turns on and applies the input voltage across the primary winding. The transformer turns the voltage to a lower level on the secondary side. The clamp capacitor along with the reset switch reverse biases the transformer primary each cycle when the main switch turns off. This reverse voltage resets the transformer. The clamp capacitor voltage is V_{IN} / (1-D).

The secondary rectification employs self-driven synchronous rectification to maintain high efficiency and ease of drive.

Feedback from the output is processed by an amplifier and reference, generating an error voltage, which is coupled back to the primary side control through an opto-coupler. The LM5025D voltage mode controller pulse width modulates the error signal with a ramp signal derived from the input voltage. Deriving the ramp signal slope from the input voltage provides line feed-forward, which improves line transient rejection. The LM5025D also provides a controlled delay necessary for the reset switch.

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Typical Application (continued)

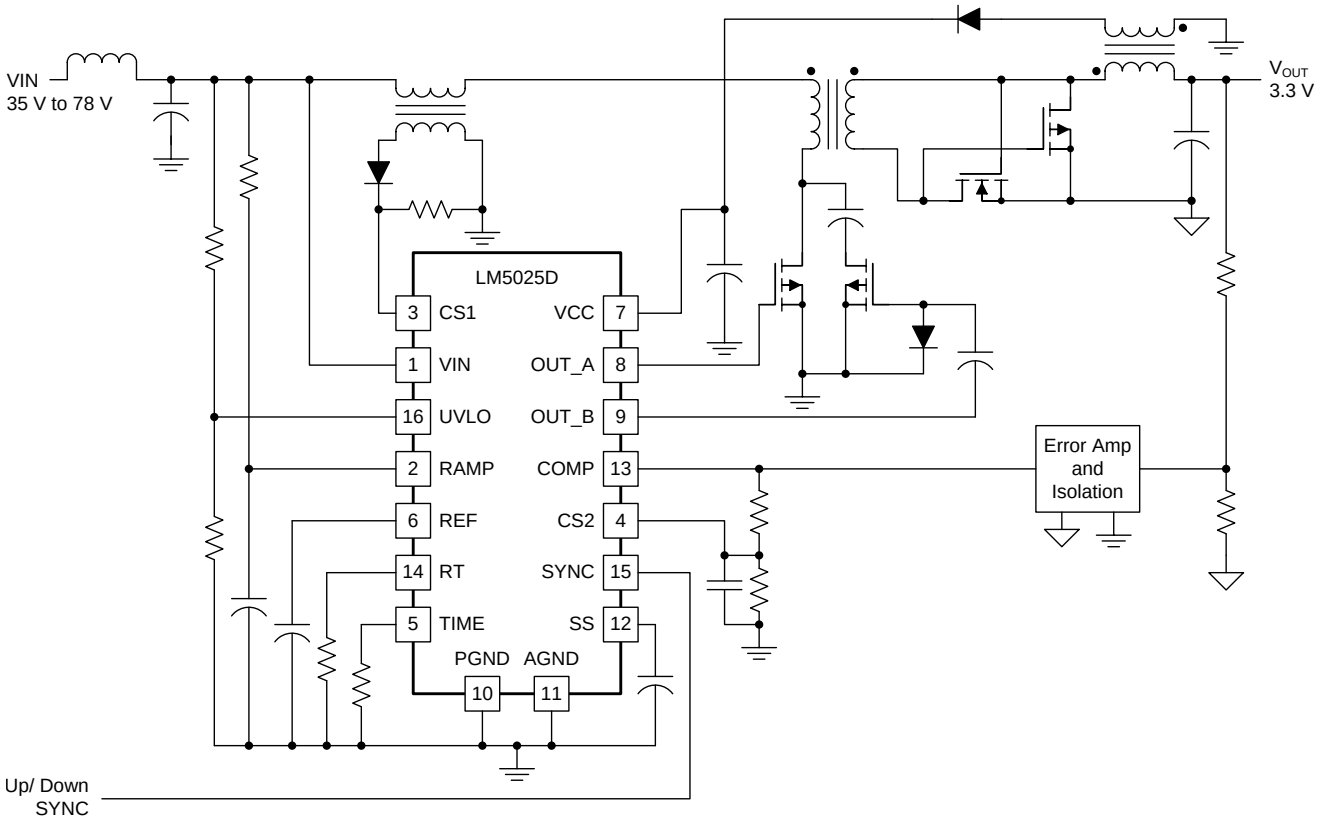

Figure 14. Simplified Active Clamp Forward Power Converter

Typical Application (continued)

8.2.1 Design Requirements

This typical application provides an example of a fully-functional power converter based on the Active Clamp Forward topology in an industry standard half-brick footprint.

The design requirements are:

- Input Range: 36 V to 78 V (100 V peak)
- Output Voltage: 3.3 V
- Output Current: 0 A to 30 A
- Measured Efficiency: 90.5% at 30 A, 92.5% at 15 A
- Frequency of Operation: 230 kHz
- Board Size: 2.3 x 2.4 x 0.5 inches
- Load Regulation: 1%
- Line Regulation: 0.1%
- Line UVLO, Hiccup Current Limit

8.2.2 Detailed Design Procedure

Before the controller design begins, the power stage design must be completed. This chapter describes the calculations needed to configure the LM5025D controller to meet the power stage design requirements.

8.2.2.1 Oscillator

The desired switching frequency F is set by a resistor connected between RT pin and ground. The resistance value R_T is calculated from:

$$R_T = (5725/F)^{1.026} \quad (1)$$

where

- F is in kHz and R_T in kΩ.

8.2.2.2 Soft-Start Ramp Time and Hiccup Interval

The soft-start ramp time and hiccup internal is programmed by a capacitor (C_{SS}) on the SS pin to ground. The soft-start ramp time is determined by comparing the SS pin voltage with COMP pin voltage. When the SS voltage is less than COMP voltage, the COMP voltage is clamped by SS voltage. The PWM duty is limited by the clamped COMP voltage, so that soft start can be achieved. The first PWM pulse is generated after COMP voltage reaches 1 V. So the soft-start ramp time of the output voltage can be estimated by:

$$T_{SS}\,(\text{ms}) = C_{SS}\,(\text{nF}) \times \frac{V_{SS} - 1\,\text{V}}{20\,\mu\text{A}} \quad (2)$$

where

- V_{SS} is the steady state COMP pin voltage. This voltage is determined by the output voltage, voltage divider, and the compensation network.

In hiccup mode, the SS current source is reduced to 1 µA. When the first PWM pulse is generated, the current source switches to 20 µA, and the power supply tries to start up again. The hiccup interval can be calculated by:

$$T_{hiccup}\,(\text{ms}) = C_{SS}\,(\text{nF}) \times \frac{1\,\text{V}}{1\,\mu\text{A}} \quad (3)$$

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Typical Application (continued)

8.2.2.3 Feed-Forward Ramp and Maximum On Time Clamp

An example illustrates the use of the Volt x Second Clamp comparator to achieve a 50% duty cycle limit, at 200bKHz, at a 48-V line input: A 50% duty cycle at a 200 KHz requires a 2.5 µs of ON time. At 48-V input the Volt x Second product is 120 V x µs (48 V x 2.5 µs). To achieve this clamp level:

$$R_{FF} \times C_{FF} = V_{IN} \times T_{ON} / 2.5V \quad (4)$$

$$48 \times 2.5\ \mu F / 2.5 = 48\ \mu F \quad (5)$$

Select C_{FF} = 470 pF

R_{FF} = 102 kΩ

The recommended capacitor value range for C_{FF} is 100 pF to 1000 pF.

8.2.2.4 Dead Times

The magnitude of the overlap/dead time can be calculated as follows:

Overlap Time (ns) = 2.8 x R_{SET} - 1.2

Dead Time (ns) = 2.9 x R_{SET} +20

R_{SET} in kΩ, Time in ns

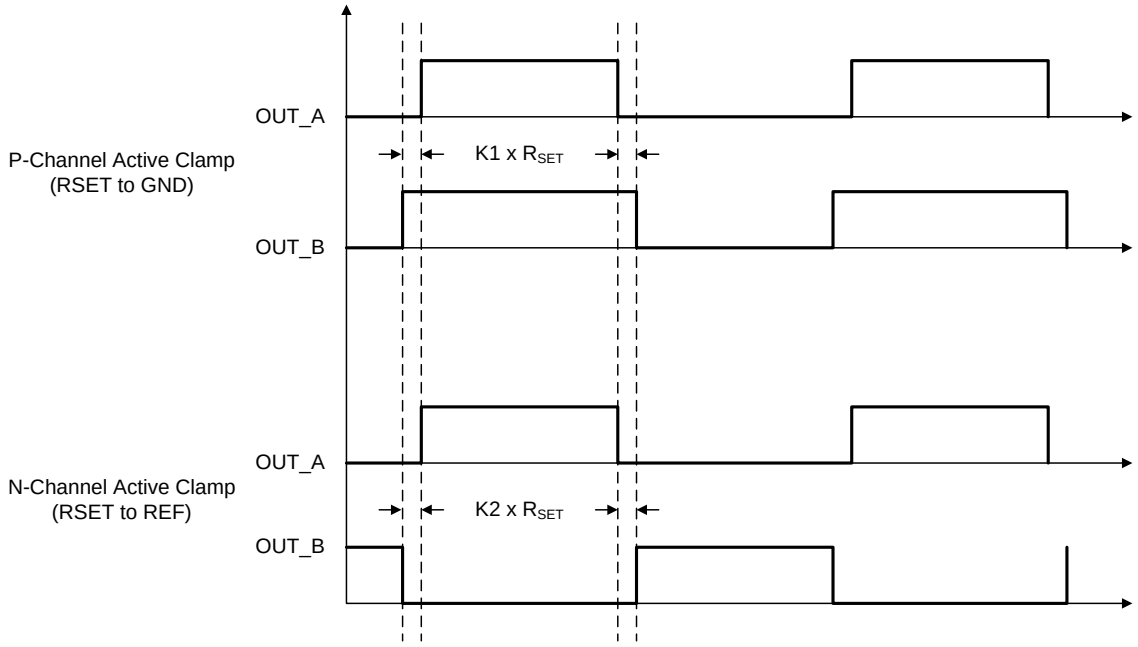
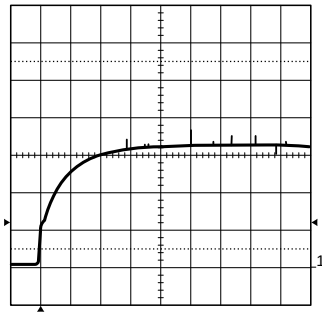


Figure 15. PWM Outputs

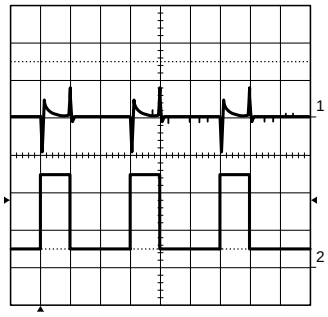
Typical Application (continued)

8.2.3 Application Curves



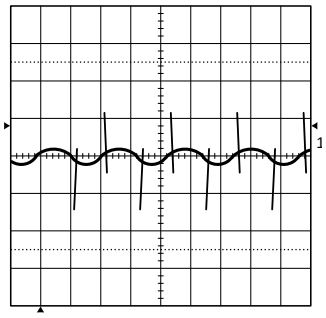
Conditions: Input Voltage = 48 VDC, Output Current = 5 A
Trace 1: Output Voltage Volts/div = 0.5 V
Horizontal Resolution = 1 msec/div

Figure 16. Output Voltage During Typical Startup



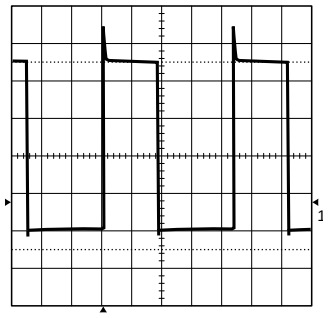
Conditions: Input Voltage = 48 VDC, Output Current = 5 A to 25 A
Trace 1: Output Voltage Volts/div = 0.5 V
Trace 2: Output Current, Amps/div = 10.0 A
Horizontal Resolution = 1 µs/div

Figure 17. Transient Response



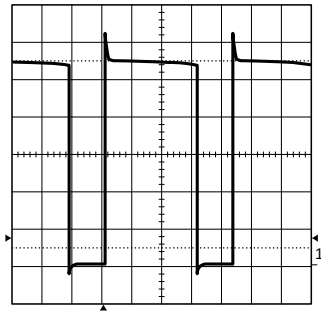
Conditions: Input Voltage = 48 VDC, Output Current = 30 A
Bandwidth Limit = 25 MHz
Trace 1: Output Ripple Voltage Volts/div = 50 mV
Horizontal Resolution = 2 µs/div

Figure 18. Output Ripple



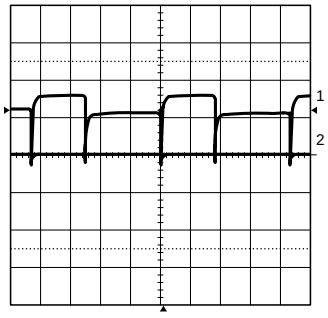
Conditions: Input Voltage = 38 VDC, Output Current = 25 A
Trace 1: Q1 drain voltage Volts/div = 20 V
Horizontal Resolution = 1 µs/div

Figure 19. Drain Voltage



Conditions: Input Voltage = 78 VDC, Output Current = 25 A
Trace 1: Q1 drain voltage Volts/div = 20 V
Horizontal Resolution = 1 µs/div

Figure 20. Drain Voltage



Conditions: Input Voltage = 48 VDC, Output Current = 5 A
Synchronous rectifier, Q3 gate Volts/div = 5 V
Trace 1: Synchronous rectifier, Q3 gate Volts/div = 5 V
Trace 2: Synchronous rectifier, Q5 gate Volts/div = 5 V
Horizontal Resolution = 1 µs/div

Figure 21. Gate Voltages of the Synchronous Rectifiers

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8.3 System Examples

Shown below is an application circuit with 36-V to 78-V input and 3.3-V, 30-A output capability.

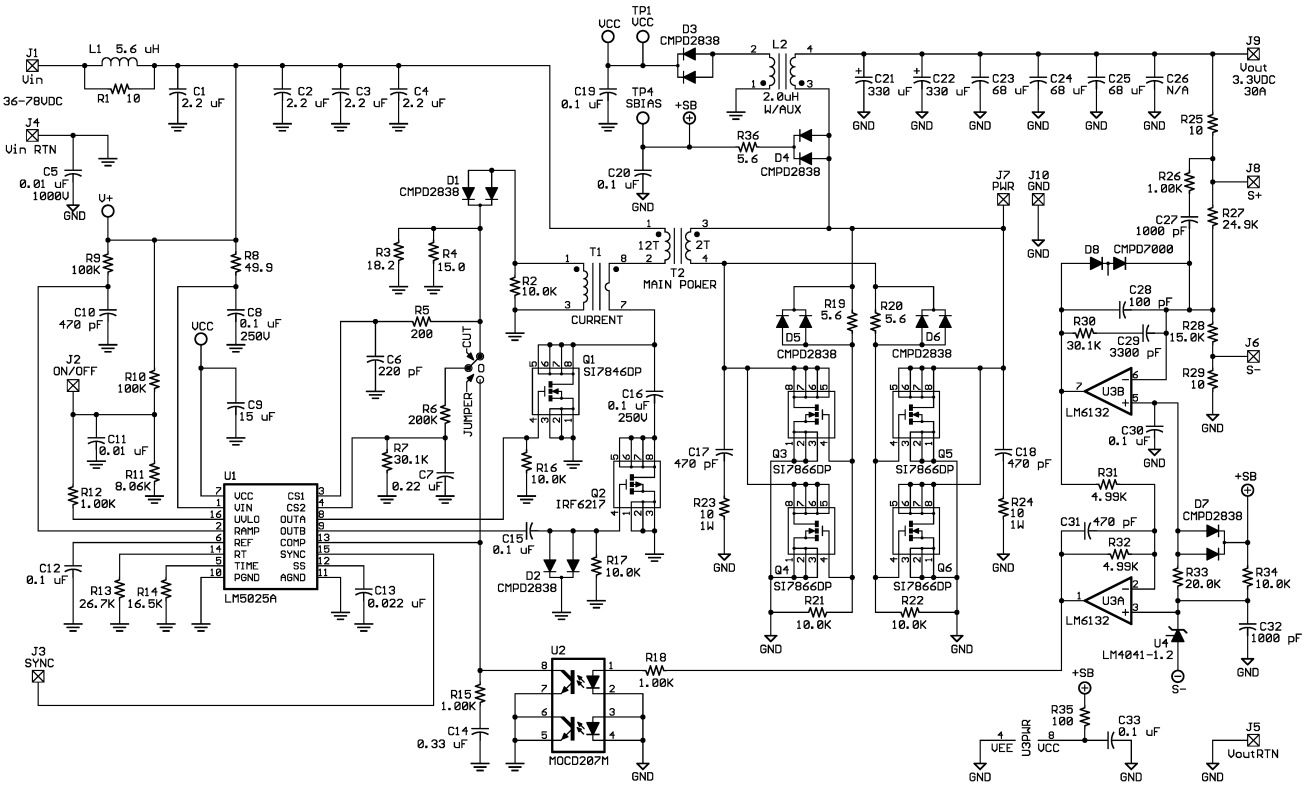

Figure 22. Application Circuit

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9 Power Supply Recommendations

V_{CC} pin is the power supply for the device. There should be a 0.1-µF~100-µF capacitor directly from V_{CC} to ground. REF pin should be by-passed to ground as close as possible to the device using a 0.1-µF capacitor.

10 Layout

10.1 Layout Guidelines

- Connect two grounds PGND (power ground) and AGND (analog ground) directly as device ground ICGND. The connection should be as close to the pins as possible.
- If there are multiple PCB layers and there is a inner ground layer, use two vias or one big via on GND and connect them to the inner ground layer (ICGND).
- The power stage ground PSGND should be separated with the ICGND. PSGND and ICGND should be connected at a single point close to the device.
- The bypass capacitors to the V_{CC} pin and REF pin should be as close as possible to the pins and ground (ICGND).
- The filtering capacitors connected to CS1 and CS2 pins should have connections as short as possible to ICGND; if an inner ground layer is available, use vias to connect the capacitors to the ground layer (ICGND).
- The resistors and capacitors connected to the timing configuration pins should be as close as possible to the pins and ground (ICGND).

10.2 Layout Example

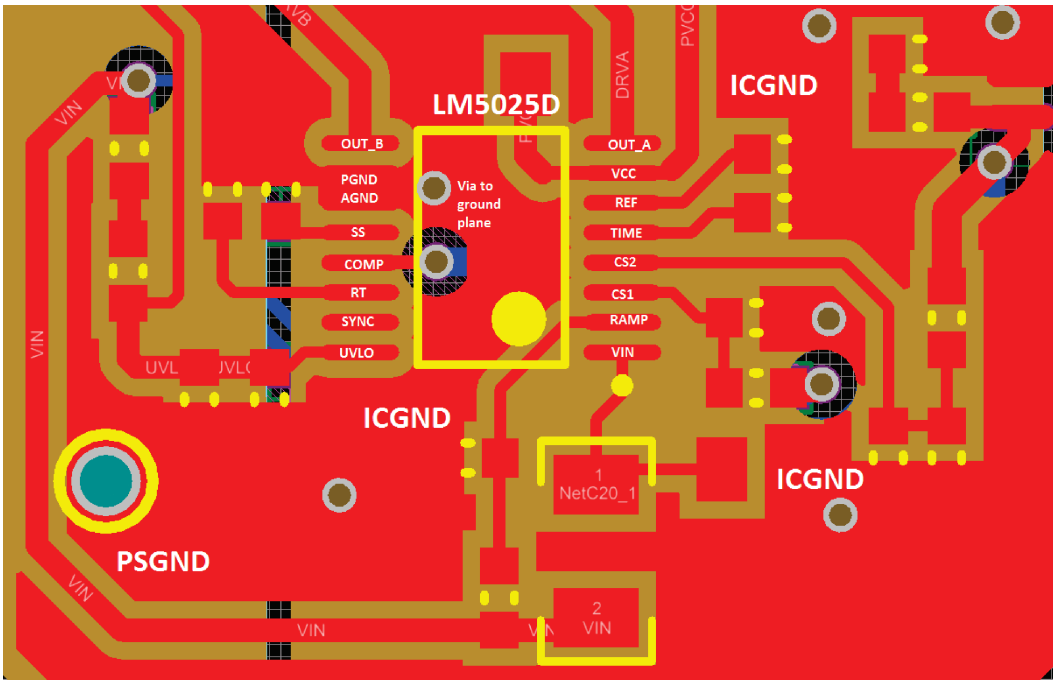

Figure 23. Layout Example

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11 Device and Documentation Support

11.1 Trademarks

All trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5025DMTC/NOPB	ACTIVE	TSSOP	PW	16	92	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	L5025D MTC	Samples
LM5025DMTCX/NOPB	ACTIVE	TSSOP	PW	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	L5025D MTC	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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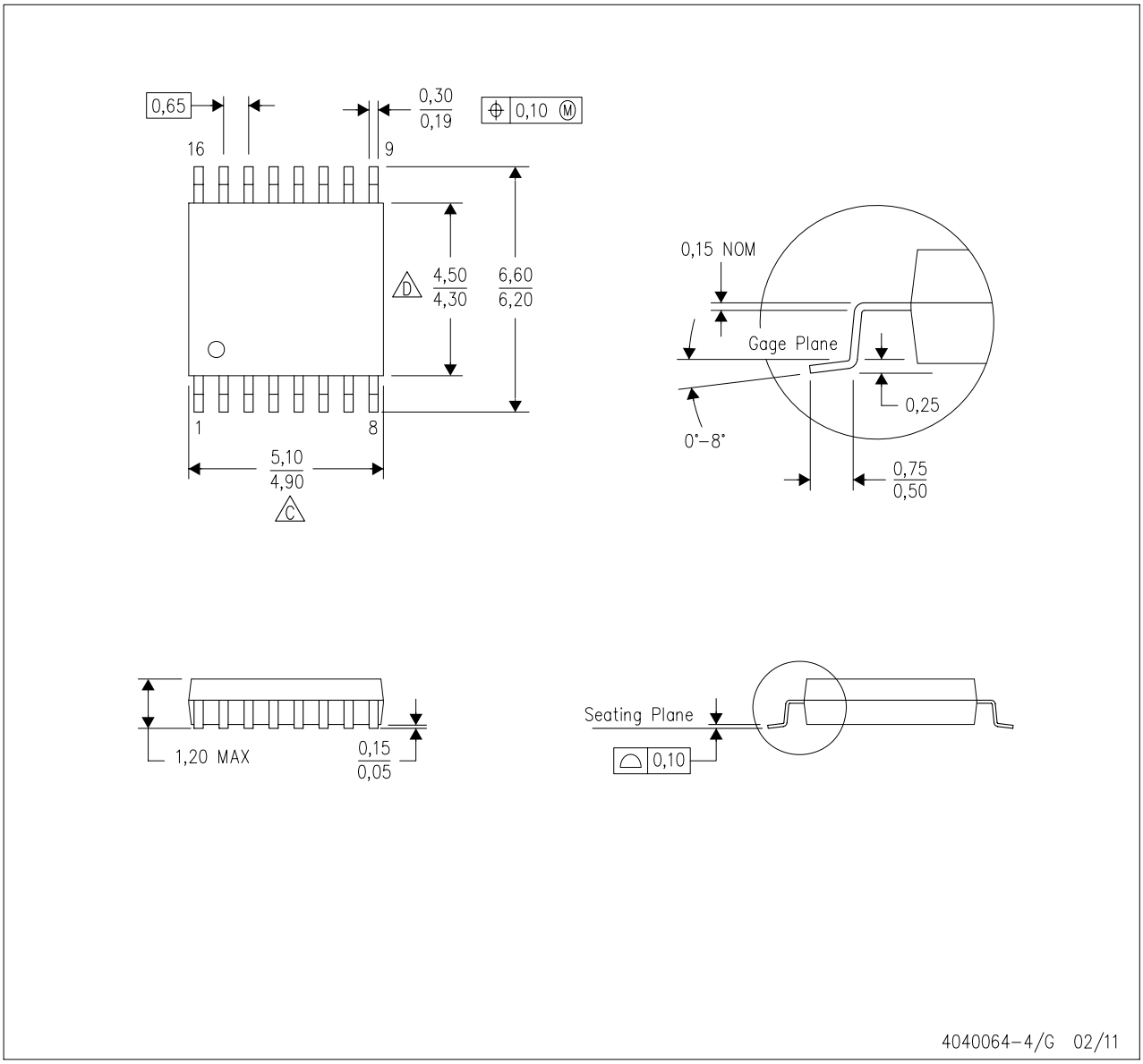
MECHANICAL DATA

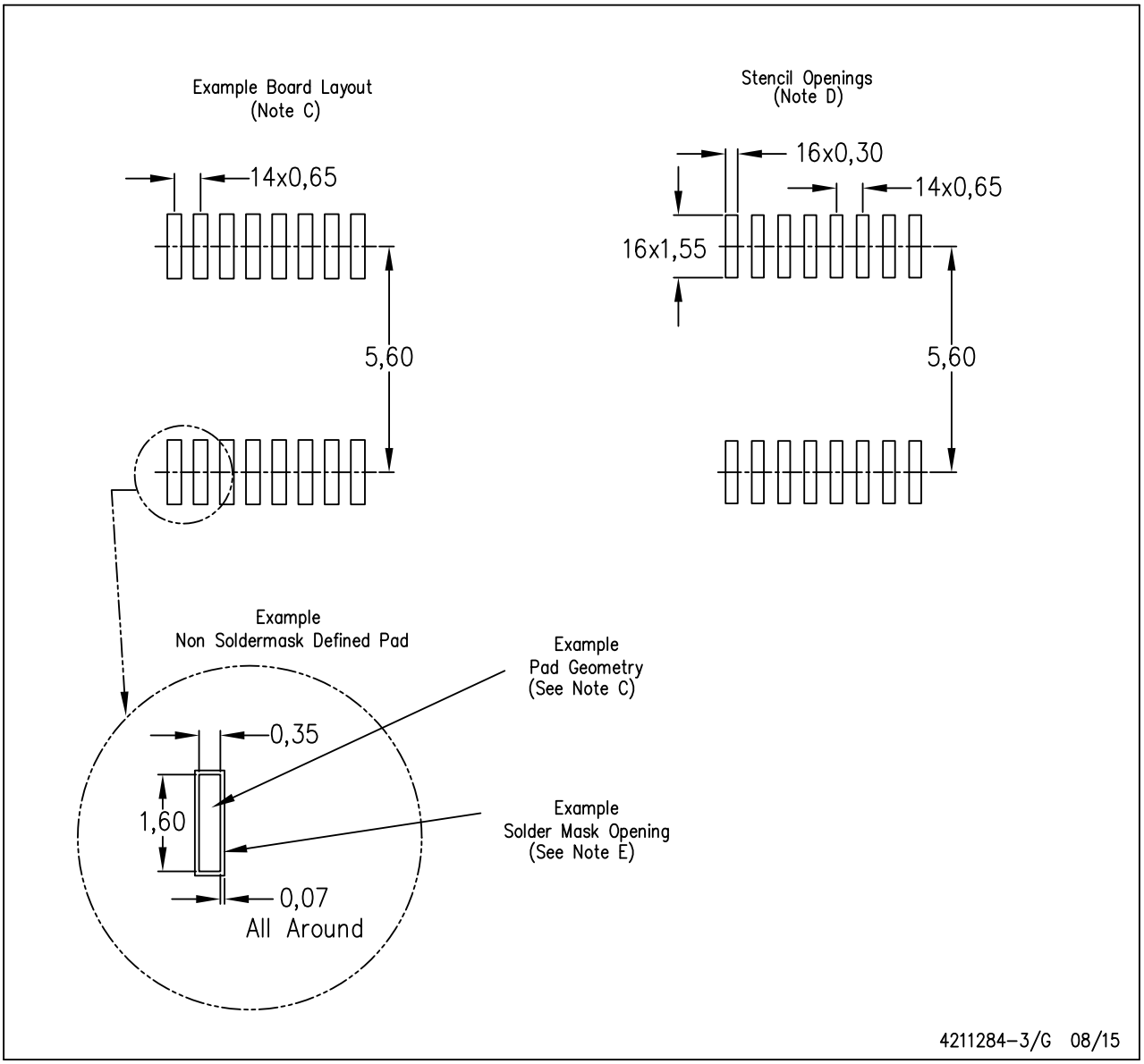
PW (R-PDSO-G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO-153

LAND PATTERN DATA

PW (R-PDSO-G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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