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LP2996M/NOPB

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LP2996-N DDR Termination Regulator

Check for Samples: LP2996-N

FEATURES

- **Source and Sink Current**
- **Low Output Voltage Offset**
- **No External Resistors Required**
- **Linear Topology**
- **Suspend to Ram (STR) Functionality**
- **Low External Component Count**
- **Thermal Shutdown**
- **Available in SOIC-8, SO PowerPAD-8 or WQFN-16 packages**

APPLICATIONS

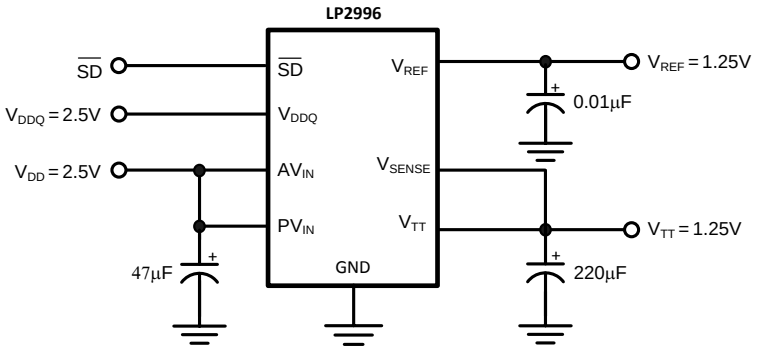
- **DDR-I and DDR-II Termination Voltage**
- **SSTL-2 and SSTL-3 Termination**
- **HSTL Termination**

DESCRIPTION

The LP2996-N linear regulator is designed to meet the JEDEC SSTL-2 specifications for termination of DDR-SDRAM. The device contains a high-speed operational amplifier to provide excellent response to load transients. The output stage prevents shoot through while delivering 1.5A continuous current and transient peaks up to 3A in the application as required for DDR-SDRAM termination. The LP2996-N also incorporates a V_{SENSE} pin to provide superior load regulation and a V_{REF} output as a reference for the chipset and DIMMs.

An additional feature found on the LP2996-N is an active low shutdown ($\overline{SD}$) pin that provides Suspend To RAM (STR) functionality. When $\overline{SD}$ is pulled low the V_{TT} output will tri-state providing a high impedance output, but, V_{REF} will remain active. A power savings advantage can be obtained in this mode through lower quiescent current.

Typical Application Circuit



Connection Diagram

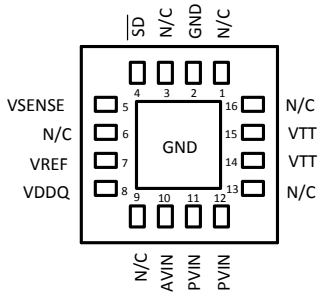


Figure 1. WQFN-16 Layout (Top View)

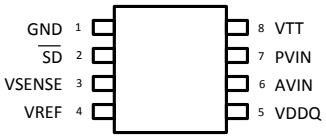


Figure 2. SOIC-8 Layout

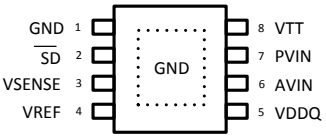


Figure 3. SO PowerPAD-8 Layout

PIN DESCRIPTIONS

SOIC-8 Pin or SO PowerPAD-8 Pin	WQFN Pin	Name	Function
1	2	GND	Ground
2	4	$\overline{SD}$	Shutdown
3	5	VSENSE	Feedback pin for regulating V_{TT}.
4	7	VREF	Buffered internal reference voltage of $V_{DDQ}/2$
5	8	VDDQ	Input for internal reference equal to $V_{DDQ}/2$
6	10	AVIN	Analog input pin
7	11, 12	PVIN	Power input pin
8	14, 15	VTT	Output voltage for connection to termination resistors
-	1, 3, 6, 9, 13, 16	NC	No internal connection
	EP	EP	Exposed pad thermal connection. Connect to Ground.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

AVIN to GND	−0.3V to +6V
PVIN to GND	-0.3V to AVIN
VDDQ(3)	−0.3V to +6V
Storage Temp. Range	−65°C to +150°C
Junction Temperature	150°C
SOIC-8 Thermal Resistance (θ_{JA})	151°C/W
SO PowerPAD-8 Thermal Resistance (θ_{JA})	43°C/W
WQFN-16 Thermal Resistance (θ_{JA})	51°C/W
Lead Temperature (Soldering, 10 sec)	260°C
ESD Rating(4)	1kV

(1) Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating range indicates conditions for which the device is intended to be functional, but does not ensure specific performance limits. For ensured specifications and test conditions see Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) VDDQ voltage must be less than 2 x (AVIN - 1) or 6V, whichever is smaller.
(4) The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.

Operating Range

Junction Temp. Range(1)	0°C to +125°C
AVIN to GND	2.2V to 5.5V
PVIN Supply Voltage	0 to AVIN
SD Input Voltage	0 to AVIN

(1) At elevated temperatures, devices must be derated based on thermal resistance. The device in the SOIC-8 package must be derated at θ_{JA} = 151.2° C/W junction to ambient with no heat sink.

Electrical Characteristics

Specifications with standard typeface are for T_J = 25°C and limits in **boldface type** apply over the full **Operating Temperature Range** (T_J = 0°C to +125°C)(1). Unless otherwise specified, AVIN = PVIN = 2.5V, VDDQ = 2.5V(2).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{REF}	V_{REF} Voltage	VIN = VDDQ = 2.3V VIN = VDDQ = 2.5V VIN = VDDQ = 2.7V	**1.135** **1.235** **1.335**	1.158 1.258 1.358	**1.185** **1.285** **1.385**	V
Z_{VREF}	V_{REF} Output Impedance	I_{REF} = -30 to +30 µA		2.5		kΩ
V_{TT}	V_{TT} Output Voltage	I_{OUT} = 0A VIN = VDDQ = 2.3V VIN = VDDQ = 2.5V VIN = VDDQ = 2.7V	 **1.125** **1.225** **1.325**	 1.159 1.259 1.359	 **1.190** **1.290** **1.390**	V
		I_{OUT} = ±1.5A(3) VIN = VDDQ = 2.3V VIN = VDDQ = 2.5V VIN = VDDQ = 2.7V	 **1.125** **1.225** **1.325**	 1.159 1.259 1.359	 **1.190** **1.290** **1.390**	
Vos_{TT}/V_{TT}	V_{TT} Output Voltage Offset (V_{REF}-V_{TT})	I_{OUT} = 0A I_{OUT} = -1.5A(3) I_{OUT} = +1.5A(3)	**-20** **-25** **-25**	0 0 0	**20** **25** **25**	mV
I_Q	Quiescent Current(4)	I_{OUT} = 0A(1)		320	**500**	µA
Z_{VDDQ}	VDDQ Input Impedance			100		kΩ
I_{SD}	Quiescent Current in Shutdown(4)	SD = 0V		115	**150**	µA
I_{Q_SD}	Shutdown Leakage Current	SD = 0V		2	**5**	µA
V_{IH}	Minimum Shutdown High Level		**1.9**			V
V_{IL}	Maximum Shutdown Low Level				**0.8**	V
I_V	V_{TT} Leakage Current in Shutdown	SD = 0V V_{TT} = 1.25V		1	**10**	µA
I_{SENSE}	V_{SENSE} Input Current			13		nA
T_{SD}	Thermal Shutdown	See(5)		165		Celcius
T_{SD_HYS}	Thermal Shutdown Hysteresis			10		Celcius

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate Texas Instruments' Average Outgoing Quality Level (AOQL).
(2) VIN is defined as VIN = AVIN = PVIN.
(3) V_{TT} load regulation is tested by using a 10 ms current pulse and measuring V_{TT}.
(4) Quiescent current defined as the current flow into AVIN.
(5) The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J(MAX)}$, the junction to ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. Exceeding the maximum allowable power dissipation will cause excessive die temperature and the regulator will go into thermal shutdown.

Typical Performance Characteristics

Iq vs AV_{IN} in SD

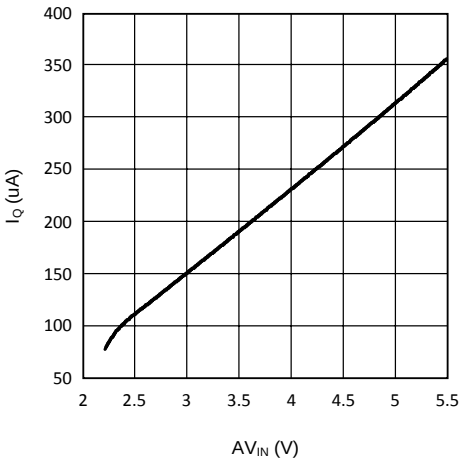


Figure 4.

Iq vs AV_{IN}

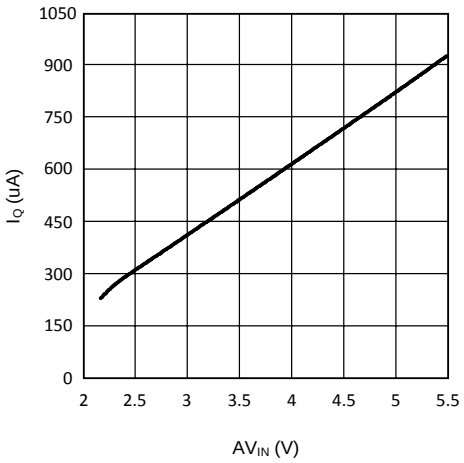


Figure 5.

V_{IH} and V_{IL}

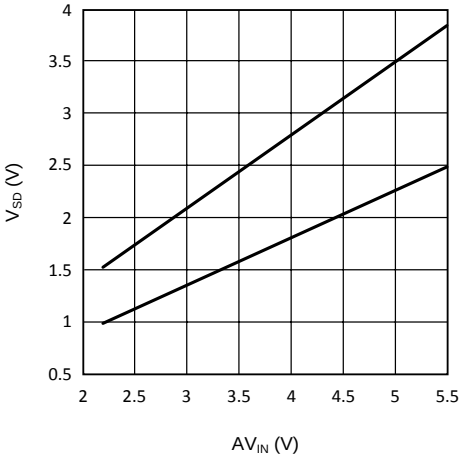


Figure 6.

V_{REF} vs I_{REF}

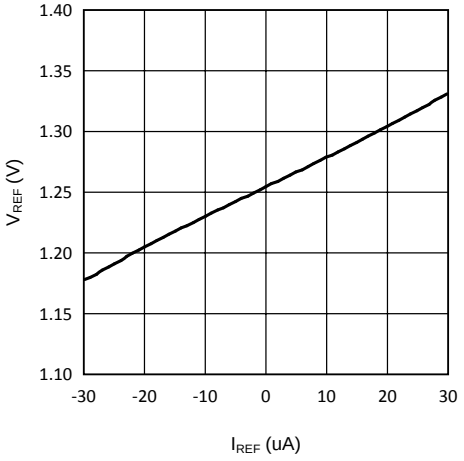


Figure 7.

V_{REF} vs V_{DDQ}

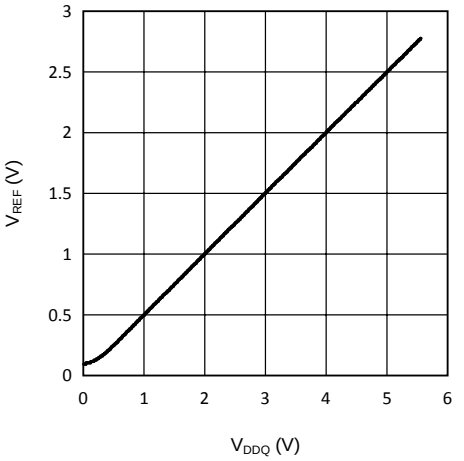


Figure 8.

V_{TT} vs I_{OUT}

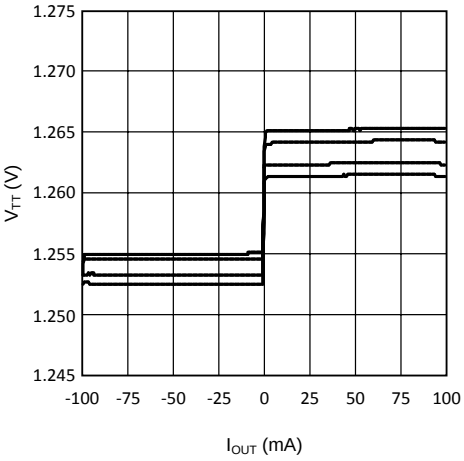


Figure 9.

Typical Performance Characteristics (continued)

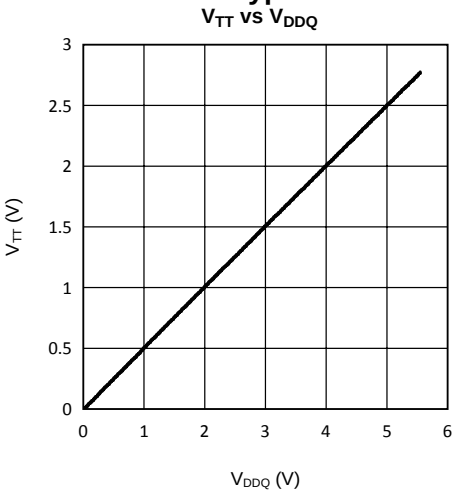


Figure 10.

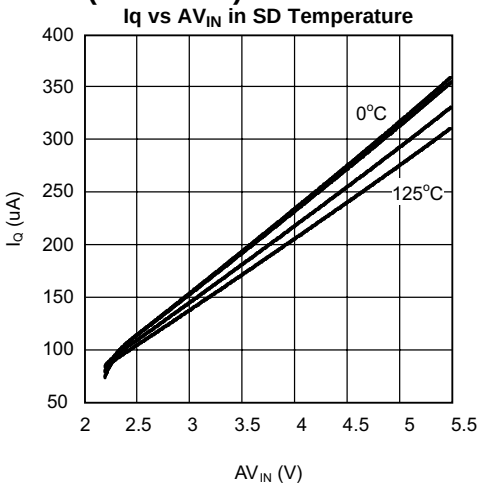


Figure 11.

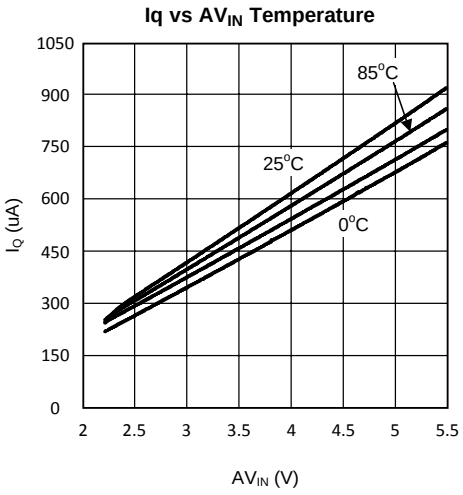


Figure 12.

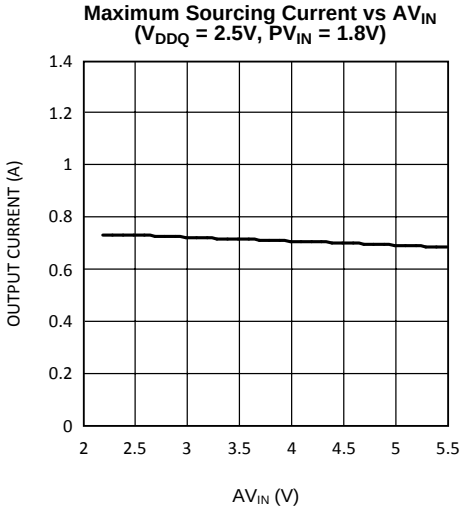


Figure 13.

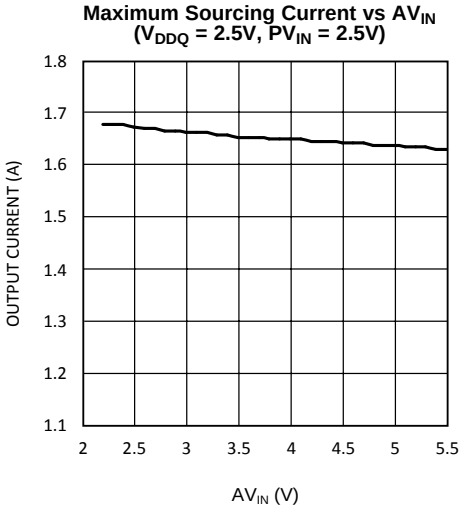


Figure 14.

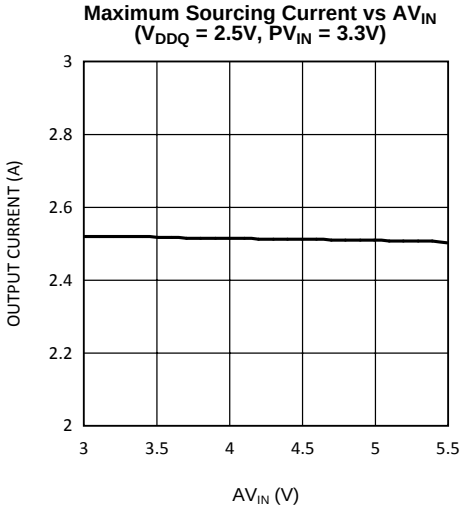


Figure 15.

Typical Performance Characteristics (continued)

Maximum Sinking Current vs AV_{IN} (V_{DDQ} = 2.5V)

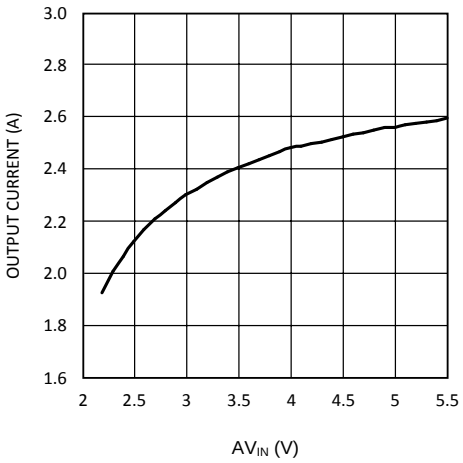


Figure 16.

Maximum Sourcing Current vs AV_{IN} (V_{DDQ} = 1.8V, PV_{IN} = 1.8V)

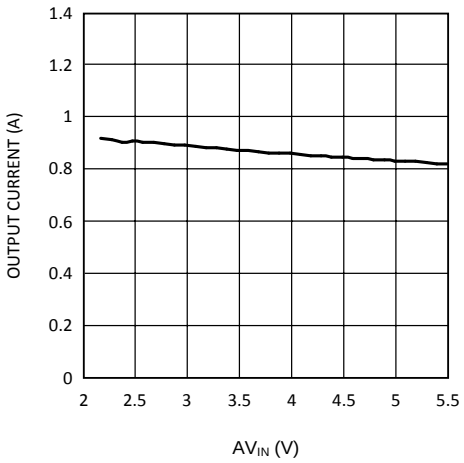


Figure 17.

Maximum Sinking Current vs AV_{IN} (V_{DDQ} = 1.8V)

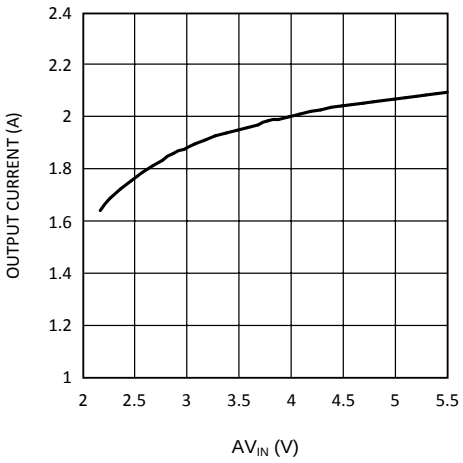


Figure 18.

Maximum Sourcing Current vs AV_{IN} (V_{DDQ} = 1.8V, PV_{IN} = 3.3V)

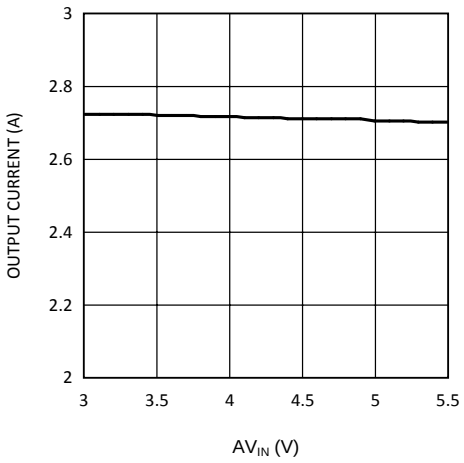
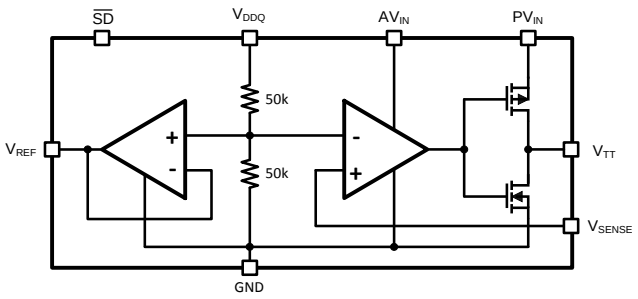


Figure 19.

BLOCK DIAGRAM



Description

The LP2996-N is a linear bus termination regulator designed to meet the JEDEC requirements of SSTL-2. The output, V_{TT} is capable of sinking and sourcing current while regulating the output voltage equal to VDDQ / 2. The output stage has been designed to maintain excellent load regulation while preventing shoot through. The LP2996-N also incorporates two distinct power rails that separates the analog circuitry from the power output stage. This allows a split rail approach to be utilized to decrease internal power dissipation. It also permits the LP2996-N to provide a termination solution for the next generation of DDR-SDRAM memory (DDRII). For new designs, the LP2997 or LP2998 is recommended for DDR-II applications. The LP2996-N can also be used to provide a termination voltage for other logic schemes such as SSTL-3 or HSTL.

Series Stub Termination Logic (SSTL) was created to improve signal integrity of the data transmission across the memory bus. This termination scheme is essential to prevent data error from signal reflections while transmitting at high frequencies encountered with DDR-SDRAM. The most common form of termination is Class II single parallel termination. This involves one R_S series resistor from the chipset to the memory and one R_T termination resistor. Typical values for R_S and R_T are 25 Ohms, although these can be changed to scale the current requirements from the LP2996-N. This implementation can be seen below in Figure 20.

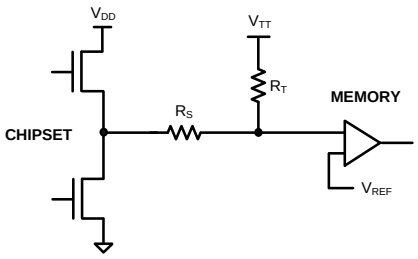


Figure 20. SSTL-Termination Scheme

PIN DESCRIPTIONS

AVIN AND PVIN

AVIN and PVIN are the input supply pins for the LP2996-N. AVIN is used to supply all the internal control circuitry. PVIN, however, is used exclusively to provide the rail voltage for the output stage used to create VTT. These pins have the capability to work off separate supplies depending on the application. Higher voltages on PVIN will increase the maximum continuous output current because of output RDSON limitations at voltages close to VTT. The disadvantage of high values of PVIN is that the internal power loss will also increase, thermally limiting the design. For SSTL-2 applications, a good compromise would be to connect the AVIN and PVIN directly together at 2.5V. This eliminates the need for bypassing the two supply pins separately. The only limitation on input voltage selection is that PVIN must be equal to or lower than AVIN. It is recommended to connect PVIN to voltage rails equal to or less than 3.3V to prevent the thermal limit from tripping because of excessive internal power dissipation. If the junction temperature exceeds the thermal shutdown than the part will enter a shutdown state identical to the manual shutdown where V_{TT} is tri-stated and V_{REF} remains active.

VDDQ

VDDQ is the input used to create the internal reference voltage for regulating V_{TT}. The reference voltage is generated from a resistor divider of two internal 50kΩ resistors. This ensures that V_{TT} will track VDDQ / 2 precisely. The optimal implementation of VDDQ is as a remote sense. This can be achieved by connecting VDDQ directly to the 2.5V rail at the DIMM instead of AVIN and PVIN. This ensures that the reference voltage tracks the DDR memory rails precisely without a large voltage drop from the power lines. For SSTL-2 applications VDDQ will be a 2.5V signal, which will create a 1.25V termination voltage at V_{TT} (See Electrical Characteristics Table for exact values of V_{TT} over temperature).

V_{SENSE}

The purpose of the sense pin is to provide improved remote load regulation. In most motherboard applications the termination resistors will connect to V_{TT} in a long plane. If the output voltage was regulated only at the output of the LP2996-N then the long trace will cause a significant IR drop resulting in a termination voltage lower at one end of the bus than the other. The V_{SENSE} pin can be used to improve this performance, by connecting it to the middle of the bus. This will provide a better distribution across the entire termination bus. If remote load regulation is not used then the V_{SENSE} pin must still be connected to V_{TT}. Care should be taken when a long V_{SENSE} trace is implemented in close proximity to the memory. Noise pickup in the V_{SENSE} trace can cause problems with precise regulation of V_{TT}. A small 0.1uF ceramic capacitor placed next to the V_{SENSE} pin can help filter any high frequency signals and preventing errors.

SHUTDOWN

The LP2996-N contains an active low shutdown pin that can be used to tri-state VTT. During shutdown V_{TT} should not be exposed to voltages that exceed AVIN. With the shutdown pin asserted low the quiescent current of the LP2996-N will drop, however, V_{DDQ} will always maintain its constant impedance of 100kΩ for generating the internal reference. Therefore to calculate the total power loss in shutdown both currents need to be considered. For more information refer to the Thermal Dissipation section. The shutdown pin also has an internal pull-up current, therefore to turn the part on the shutdown pin can either be connected to AVIN or left open.

V_{REF}

V_{REF} provides the buffered output of the internal reference voltage VDDQ / 2. This output should be used to provide the reference voltage for the Northbridge chipset and memory. Since these inputs are typically an extremely high impedance, there should be little current drawn from V_{REF}. For improved performance, an output bypass capacitor can be used, located close to the pin, to help with noise. A ceramic capacitor in the range of 0.1 µF to 0.01 µF is recommended. This output remains active during the shutdown state and thermal shutdown events for the suspend to RAM functionality.

V_{TT}

V_{TT} is the regulated output that is used to terminate the bus resistors. It is capable of sinking and sourcing current while regulating the output precisely to VDDQ / 2. The LP2996-N is designed to handle peak transient currents of up to ± 3A with a fast transient response. The maximum continuous current is a function of V_{IN} and can be viewed in the Typical Performance Characteristics section. If a transient is expected to last above the maximum continuous current rating for a significant amount of time then the output capacitor should be sized large enough to prevent an excessive voltage drop. Despite the fact that the LP2996-N is designed to handle large transient output currents it is not capable of handling these for long durations, under all conditions. The reason for this is the standard packages are not able to thermally dissipate the heat as a result of the internal power loss. If large currents are required for longer durations, then care should be taken to ensure that the maximum junction temperature is not exceeded. Proper thermal derating should always be used (please refer to the Thermal Dissipation section). If the junction temperature exceeds the thermal shutdown point than V_{TT} will tri-state until the part returns below the hysteretic trip-point.

COMPONENT SELECTIONS

INPUT CAPACITOR

The LP2996-N does not require a capacitor for input stability, but it is recommended for improved performance during large load transients to prevent the input rail from dropping. The input capacitor should be located as close as possible to the PVIN pin. Several recommendations exist dependent on the application required. A typical value recommended for AL electrolytic capacitors is 50 µF. Ceramic capacitors can also be used, a value in the range of 10 µF with X5R or better would be an ideal choice. The input capacitance can be reduced if the LP2996-N is placed close to the bulk capacitance from the output of the 2.5V DC-DC converter. If the two supply rails (AVIN and PVIN) are separated then the 47uF capacitor should be placed as close to possible to the PVIN rail. An additional 0.1uF ceramic capacitor can be placed on the AVIN rail to prevent excessive noise from coupling into the device.

OUTPUT CAPACITOR

The LP2996-N has been designed to be insensitive of output capacitor size or ESR (Equivalent Series Resistance). This allows the flexibility to use any capacitor desired. The choice for output capacitor will be determined solely on the application and the requirements for load transient response of V_{TT}. As a general recommendation the output capacitor should be sized above 100 µF with a low ESR for SSTL applications with DDR-SDRAM. The value of ESR should be determined by the maximum current spikes expected and the extent at which the output voltage is allowed to droop. Several capacitor options are available on the market and a few of these are highlighted below:

AL - It should be noted that many aluminum electrolytics only specify impedance at a frequency of 120 Hz, which indicates they have poor high frequency performance. Only aluminum electrolytics that have an impedance specified at a higher frequency (between 20 kHz and 100 kHz) should be used for the LP2996-N. To improve the ESR several AL electrolytics can be combined in parallel for an overall reduction. An important note to be aware of is the extent at which the ESR will change over temperature. Aluminum electrolytic capacitors can have their ESR rapidly increase at cold temperatures.

Ceramic - Ceramic capacitors typically have a low capacitance, in the range of 10 to 100 µF range, but they have excellent AC performance for bypassing noise because of very low ESR (typically less than 10 mΩ). However, some dielectric types do not have good capacitance characteristics as a function of voltage and temperature. Because of the typically low value of capacitance it is recommended to use ceramic capacitors in parallel with another capacitor such as an aluminum electrolytic. A dielectric of X5R or better is recommended for all ceramic capacitors.

Hybrid - Several hybrid capacitors such as OS-CON and SP are available from several manufacturers. These offer a large capacitance while maintaining a low ESR. These are the best solution when size and performance are critical, although their cost is typically higher than any other capacitor.

Thermal Dissipation

Since the LP2996-N is a linear regulator any current flow from V_{TT} will result in internal power dissipation generating heat. To prevent damaging the part from exceeding the maximum allowable junction temperature, care should be taken to derate the part dependent on the maximum expected ambient temperature and power dissipation. The maximum allowable internal temperature rise (T_{Rmax}) can be calculated given the maximum ambient temperature (T_{Amax}) of the application and the maximum allowable junction temperature (T_{Jmax}).

$$T_{Rmax} = T_{Jmax} - T_{Amax} \quad (1)$$

From this equation, the maximum power dissipation (P_{Dmax}) of the part can be calculated:

$$P_{Dmax} = T_{Rmax} / \theta_{JA} \quad (2)$$

The θ_{JA} of the LP2996-N will be dependent on several variables: the package used; the thickness of copper; the number of vias and the airflow. For instance, the θ_{JA} of the SOIC-8 is 163°C/W with the package mounted to a standard 8x4 2-layer board with 1oz. copper, no airflow, and 0.5W dissipation at room temperature. This value can be reduced to 151.2°C/W by changing to a 3x4 board with 2 oz. copper that is the JEDEC standard. Figure 21 shows how the θ_{JA} varies with airflow for the two boards mentioned.

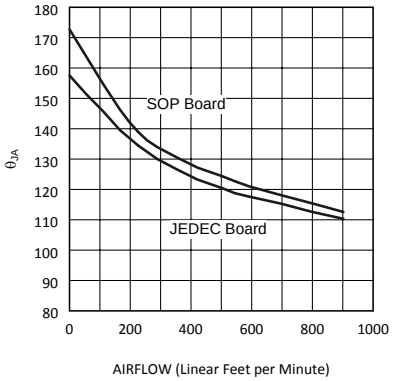


Figure 21. θ_{JA} vs Airflow (SOIC-8)

Additional improvements can be made by the judicious use of vias to connect the part and dissipate heat to an internal ground plane. Using larger traces and more copper on the top side of the board can also help. With careful layout it is possible to reduce the θ_{JA} further than the nominal values shown in Figure 21

Layout is also extremely critical to maximize the output current with the WQFN package. By simply placing vias under the DAP the θ_{JA} can be lowered significantly. Figure 22 shows the WQFN thermal data when placed on a 4-layer JEDEC board with copper thickness of 0.5/1/1/0.5 oz. The number of vias, with a pitch of 1.27 mm, has been increased to the maximum of 4 where a θ_{JA} of 50.41°C/W can be obtained. Via wall thickness for this calculation is 0.036 mm for 1oz. Copper.

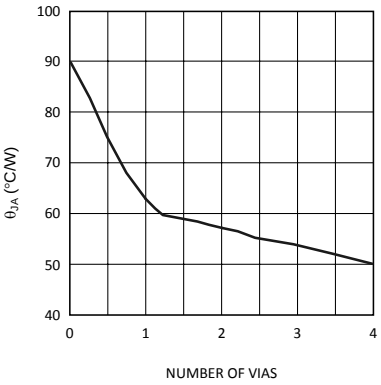


Figure 22. WQFN-16 θ_{JA} vs # of Vias (4 Layer JEDEC Board))

Additional improvements in lowering the θ_{JA} can also be achieved with a constant airflow across the package. Maintaining the same conditions as above and utilizing the 2x2 via array, Figure 23 shows how the θ_{JA} varies with airflow.

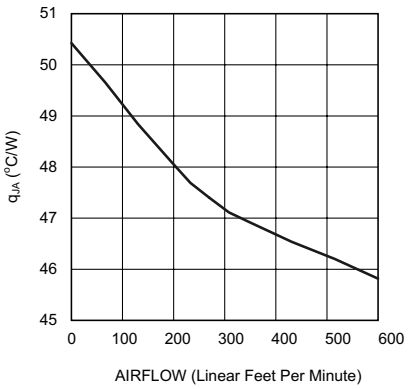


Figure 23. θ_{JA} vs Airflow Speed (JEDEC Board with 4 Vias)

Optimizing the θ_{JA} and placing the LP2996-N in a section of a board exposed to lower ambient temperature allows the part to operate with higher power dissipation. The internal power dissipation can be calculated by summing the three main sources of loss: output current at V_{TT}, either sinking or sourcing, and quiescent current at AVIN and VDDQ. During the active state (when shutdown is not held low) the total internal power dissipation can be calculated from the following equations:

$$P_D = P_{AVIN} + P_{VDDQ} + P_{VTT}$$

where (3)

$$P_{AVIN} = I_{AVIN} * V_{AVIN} \quad (4)$$

$$P_{VDDQ} = V_{VDDQ} * I_{VDDQ} = V_{VDDQ2} \times R_{VDDQ} \quad (5)$$

To calculate the maximum power dissipation at V_{TT} both conditions at V_{TT} need to be examined, sinking and sourcing current. Although only one equation will add into the total, V_{TT} cannot source and sink current simultaneously.

$$P_{VTT} = V_{VTT} \times I_{LOAD} \text{ (Sinking) or} \quad (6)$$

$$P_{VTT} = (V_{PVIN} - V_{VTT}) \times I_{LOAD} \text{ (Sourcing} \quad (7)$$

The power dissipation of the LP2996-N can also be calculated during the shutdown state. During this condition the output V_{TT} will tri-state, therefore that term in the power equation will disappear as it cannot sink or source any current (leakage is negligible). The only losses during shutdown will be the reduced quiescent current at AVIN and the constant impedance that is seen at the VDDQ pin.

$$P_D = P_{AVIN} + P_{VDDQ} \quad (8)$$

$$P_{AVIN} = I_{AVIN} \times V_{AVIN} \quad (9)$$

$$P_{VDDQ} = V_{VDDQ} * I_{VDDQ} = V_{VDDQ2} \times R_{VDDQ} \quad (10)$$

Typical Application Circuits

Several different application circuits have been shown in Figure 24 through Figure 33 to illustrate some of the options that are possible in configuring the LP2996-N. Graphs of the individual circuit performance can be found in the Typical Performance Characteristics section in the beginning of the datasheet. These curves illustrate how the maximum output current is affected by changes in AVIN and PVIN.

SSTL-2 APPLICATIONS

For the majority of applications that implement the SSTL-2 termination scheme it is recommended to connect all the input rails to the 2.5V rail. This provides an optimal trade-off between power dissipation and component count and selection. An example of this circuit can be seen in Figure 24.

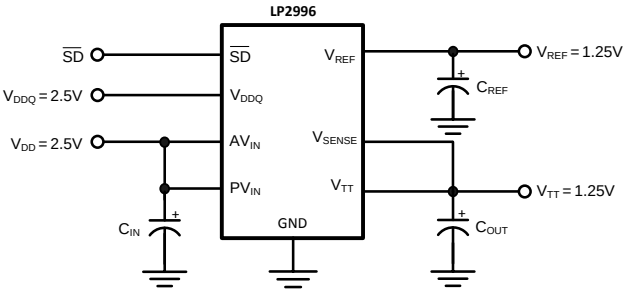


Figure 24. Recommended SSTL-2 Implementation

If power dissipation or efficiency is a major concern then the LP2996-N has the ability to operate on split power rails. The output stage (PVIN) can be operated on a lower rail such as 1.8V and the analog circuitry (AVIN) can be connected to a higher rail such as 2.5V, 3.3V or 5V. This allows the internal power dissipation to be lowered when sourcing current from V_{TT}. The disadvantage of this circuit is that the maximum continuous current is reduced because of the lower rail voltage, although it is adequate for all motherboard SSTL-2 applications. Increasing the output capacitance can also help if periods of large load transients will be encountered.

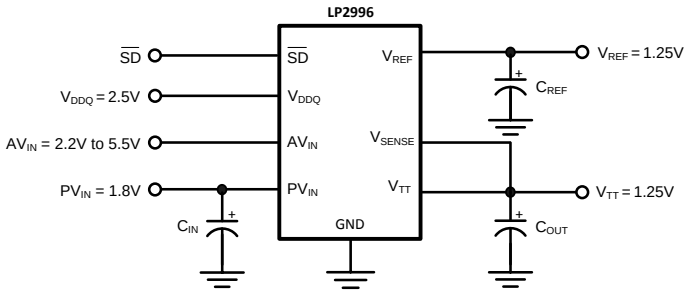


Figure 25. Lower Power Dissipation SSTL-2 Implementation

The third option for SSTL-2 applications in the situation that a 1.8V rail is not available and it is not desirable to use 2.5V, is to connect the LP2996-N power rail to 3.3V. In this situation AVIN will be limited to operation on the 3.3V or 5V rail as PVIN can never exceed AVIN. This configuration has the ability to provide the maximum continuous output current at the downside of higher thermal dissipation. Care should be taken to prevent the LP2996-N from experiencing large current levels which cause the junction temperature to exceed the maximum. Because of this risk it is not recommended to supply the output stage with a voltage higher than a nominal 3.3V rail.

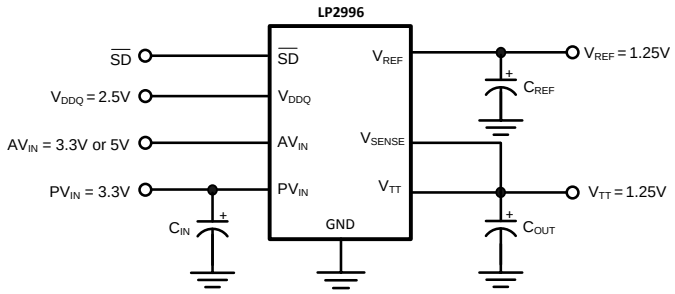


Figure 26. SSTL-2 Implementation with higher voltage rails

DDR-II APPLICATIONS

With the separate VDDQ pin and an internal resistor divider it is possible to use the LP2996-N in applications utilizing DDR-II memory. Figure 25 and Figure 26 show several implementations of recommended circuits with output curves displayed in the Typical Performance Characteristics. Figure 25 shows the recommended circuit configuration for DDR-II applications. The output stage is connected to the 1.8V rail and the AVIN pin can be connected to either a 3.3V or 5V rail. For new designs, the LP2997 or LP2998 is recommended for DDR-II applications.

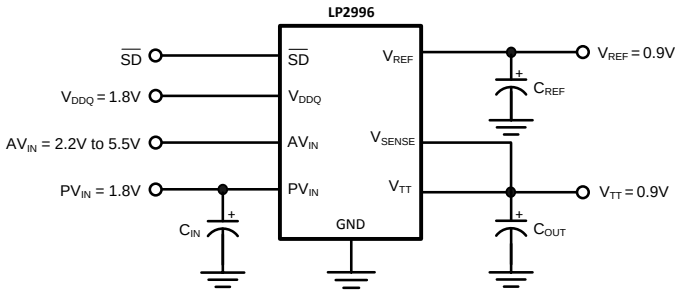


Figure 27. Recommended DDR-II Termination

If it is not desirable to use the 1.8V rail it is possible to connect the output stage to a 3.3V rail. Care should be taken to not exceed the maximum junction temperature as the thermal dissipation increases with lower V_{TT} output voltages. For this reason it is not recommended to power PVIN off a rail higher than the nominal 3.3V. The advantage of this configuration is that it has the ability to source and sink a higher maximum continuous current.

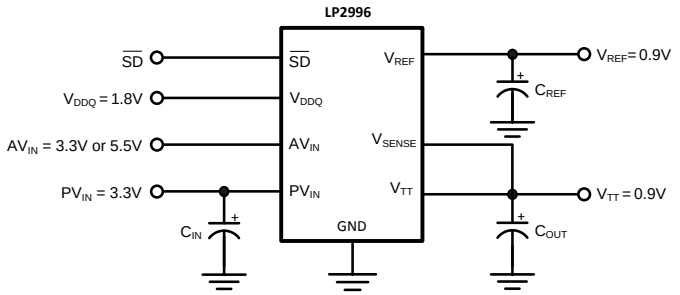


Figure 28. DDR-II Termination with higher voltage rails

LEVEL SHIFTING

If standards other than SSTL-2 are required, such as SSTL-3, it may be necessary to use a different scaling factor than 0.5 times V_{DDQ} for regulating the output voltage. Several options are available to scale the output to any voltage required. One method is to level shift the output by using feedback resistors from V_{TT} to the V_{SENSE} pin. This has been illustrated in Figure 29 and Figure 30. Figure 29 shows how to use two resistors to level shift V_{TT} above the internal reference voltage of VDDQ/2. To calculate the exact voltage at V_{TT} the following equation can be used.

$$V_{TT} = VDDQ/2 \ (1 + R1/R2) \quad (11)$$

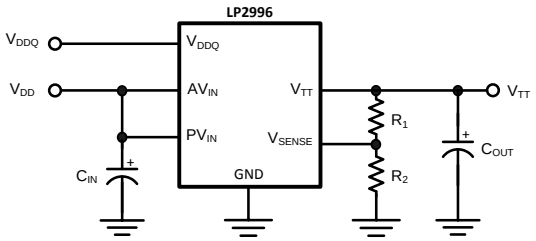


Figure 29. Increasing VTT by Level Shifting

Conversely, the R2 resistor can be placed between V_{SENSE} and V_{DDQ} to shift the V_{TT} output lower than the internal reference voltage of VDDQ/2. The equations relating VTT and the resistors can be seen below:

$$V_{TT} = VDDQ/2\ (1 - R1/R2) \quad (12)$$

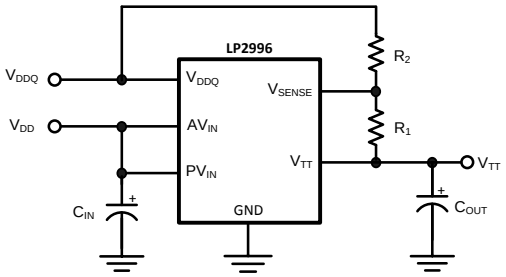


Figure 30. Decreasing VTT by Level Shifting

HSTL APPLICATIONS

The LP2996-N can be easily adapted for HSTL applications by connecting V_{DDQ} to the 1.5V rail. This will produce a V_{TT} and V_{REF} voltage of approximately 0.75V for the termination resistors. AVIN and PVIN should be connected to a 2.5V rail for optimal performance.

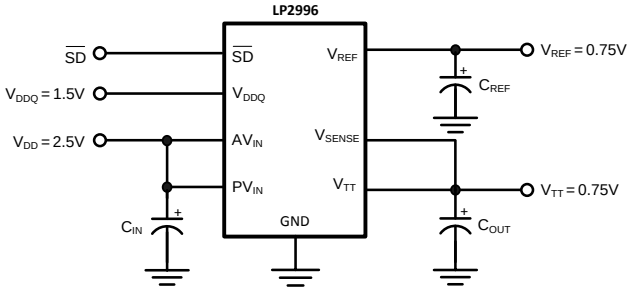


Figure 31. HSTL Application

QDR APPLICATIONS

Quad data rate (QDR) applications utilize multiple channels for improved memory performance. However, this increase in bus lines has the effect of increasing the current levels required for termination. The recommended approach in terminating multiple channels is to use a dedicated LP2996-N for each channel. This simplifies layout and reduces the internal power dissipation for each regulator. Separate V_{REF} signals can be used for each DIMM bank from the corresponding regulator with the chipset reference provided by a local resistor divider or one of the LP2996-N signals. Because V_{REF} and V_{TT} are expected to track and the part to part variations are minor, there should be little difference between the reference signals of each LP2996-N.

OUTPUT CAPACITOR SELECTION

For applications utilizing the LP2996-N to terminate SSTL-2 I/O signals the typical application circuit shown in Figure 30 can be implemented.

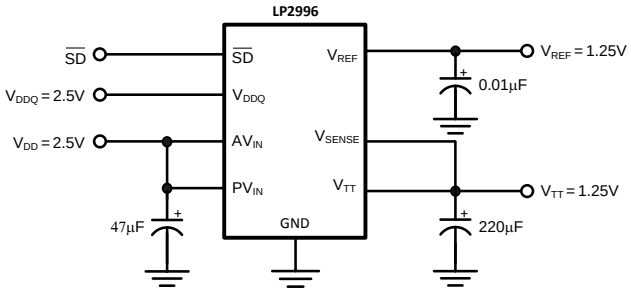


Figure 32. Typical SSTL-2 Application Circuit

This circuit permits termination in a minimum amount of board space and component count. Capacitor selection can be varied depending on the number of lines terminated and the maximum load transient. However, with motherboards and other applications where V_{TT} is distributed across a long plane it is advisable to use multiple bulk capacitors and addition to high frequency decoupling. Figure 31 shown below depicts an example circuit where 2 bulk output capacitors could be situated at both ends of the V_{TT} plane for optimal placement. Large aluminum electrolytic capacitors are used for their low ESR and low cost.

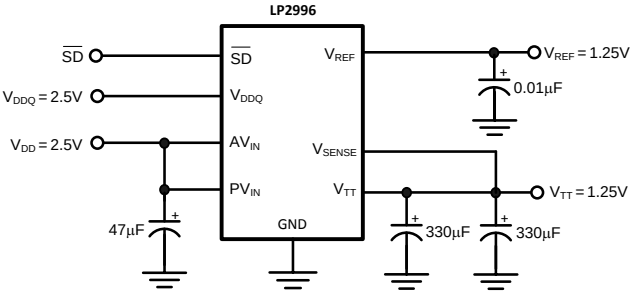


Figure 33. Typical SSTL-2 Application Circuit for Motherboards

In most PC applications an extensive amount of decoupling is required because of the long interconnects encountered with the DDR-SDRAM DIMMs mounted on modules. As a result bulk aluminum electrolytic capacitors in the range of 1000uF are typically used.

PCB Layout Considerations

1. The input capacitor for the power rail should be placed as close as possible to the PVIN pin.
2. V_{SENSE} should be connected to the V_{TT} termination bus at the point where regulation is required. For motherboard applications an ideal location would be at the center of the termination bus.
3. V_{DDQ} can be connected remotely to the V_{DDQ} rail input at either the DIMM or the Chipset. This provides the most accurate point for creating the reference voltage.
4. For improved thermal performance excessive top side copper should be used to dissipate heat from the package. Numerous vias from the ground connection to the internal ground plane will help. Additionally these can be located underneath the package if manufacturing standards permit.
5. Care should be taken when routing the V_{SENSE} trace to avoid noise pickup from switching I/O signals. A 0.1uF ceramic capacitor located close to the $_{SENSE}$ can also be used to filter any unwanted high frequency signal. This can be an issue especially if long $_{SENSE}$ traces are used.
6. V_{REF} should be bypassed with a 0.01 µF or 0.1 µF ceramic capacitor for improved performance. This capacitor should be located as close as possible to the V_{REF} pin.

REVISION HISTORY

Changes from Revision I (March 2013) to Revision J	Page
• Changed layout of National Data Sheet to TI format	15

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP2996LQ/NOPB	ACTIVE	WQFN	NHP	16	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	0 to 125	L00006B	Samples
LP2996LQX/NOPB	ACTIVE	WQFN	NHP	16	4500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	0 to 125	L00006B	Samples
LP2996M	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	0 to 125	2996M	
LP2996M/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 125	2996M	Samples
LP2996MR	NRND	SO PowerPAD	DDA	8	95	TBD	Call TI	Call TI	0 to 125	LP2996	
LP2996MR/NOPB	ACTIVE	SO PowerPAD	DDA	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	0 to 125	LP2996	Samples
LP2996MRX	NRND	SO PowerPAD	DDA	8	2500	TBD	Call TI	Call TI	0 to 125	LP2996	
LP2996MRX/NOPB	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	0 to 125	LP2996	Samples
LP2996MX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 125	2996M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

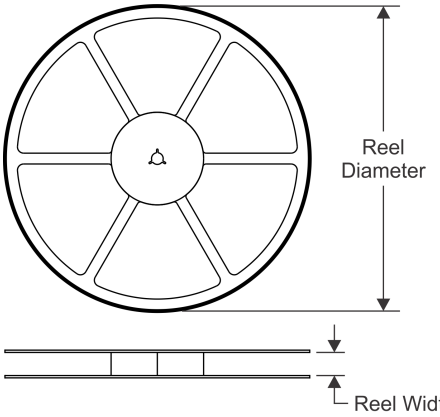
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

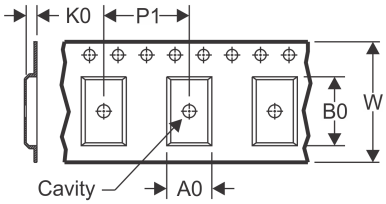
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

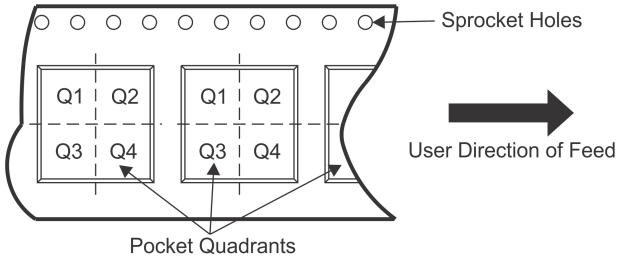


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

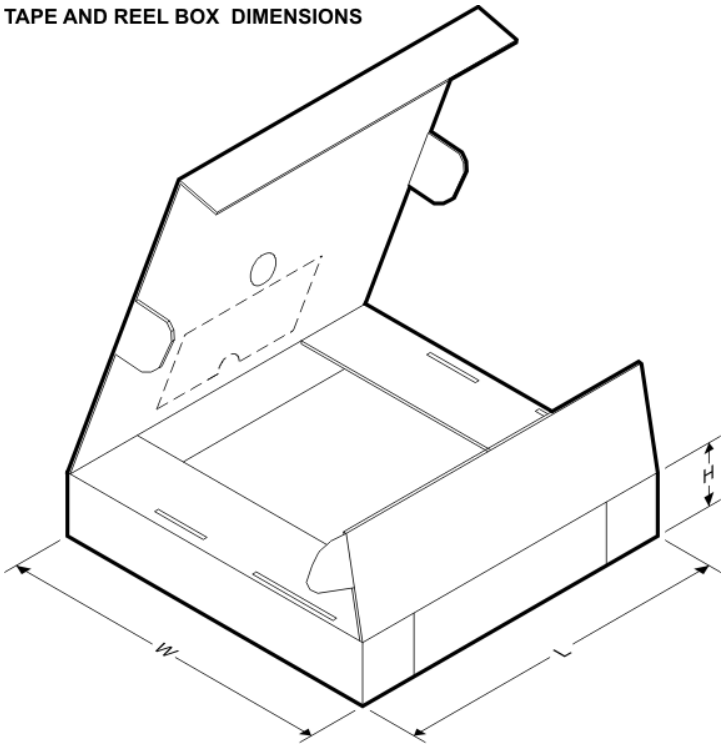


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2996LQ/NOPB	WQFN	NHP	16	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP2996LQX/NOPB	WQFN	NHP	16	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP2996MRX	SO Power PAD	DDA	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LP2996MRX/NOPB	SO Power PAD	DDA	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LP2996MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2996LQ/NOPB	WQFN	NHP	16	1000	213.0	191.0	55.0
LP2996LQX/NOPB	WQFN	NHP	16	4500	367.0	367.0	35.0
LP2996MRX	SO PowerPAD	DDA	8	2500	367.0	367.0	35.0
LP2996MRX/NOPB	SO PowerPAD	DDA	8	2500	367.0	367.0	35.0
LP2996MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

THERMAL PAD MECHANICAL DATA

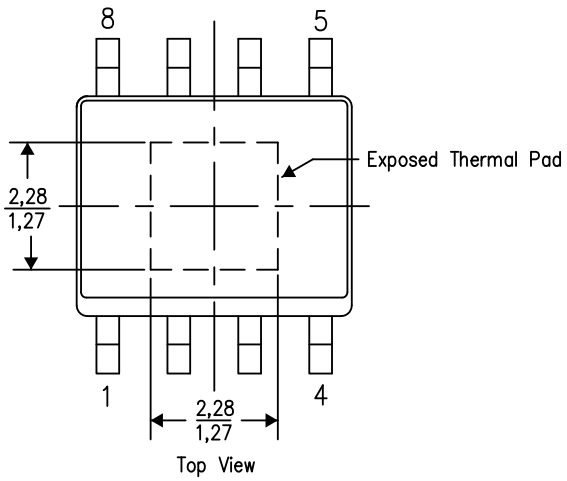
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

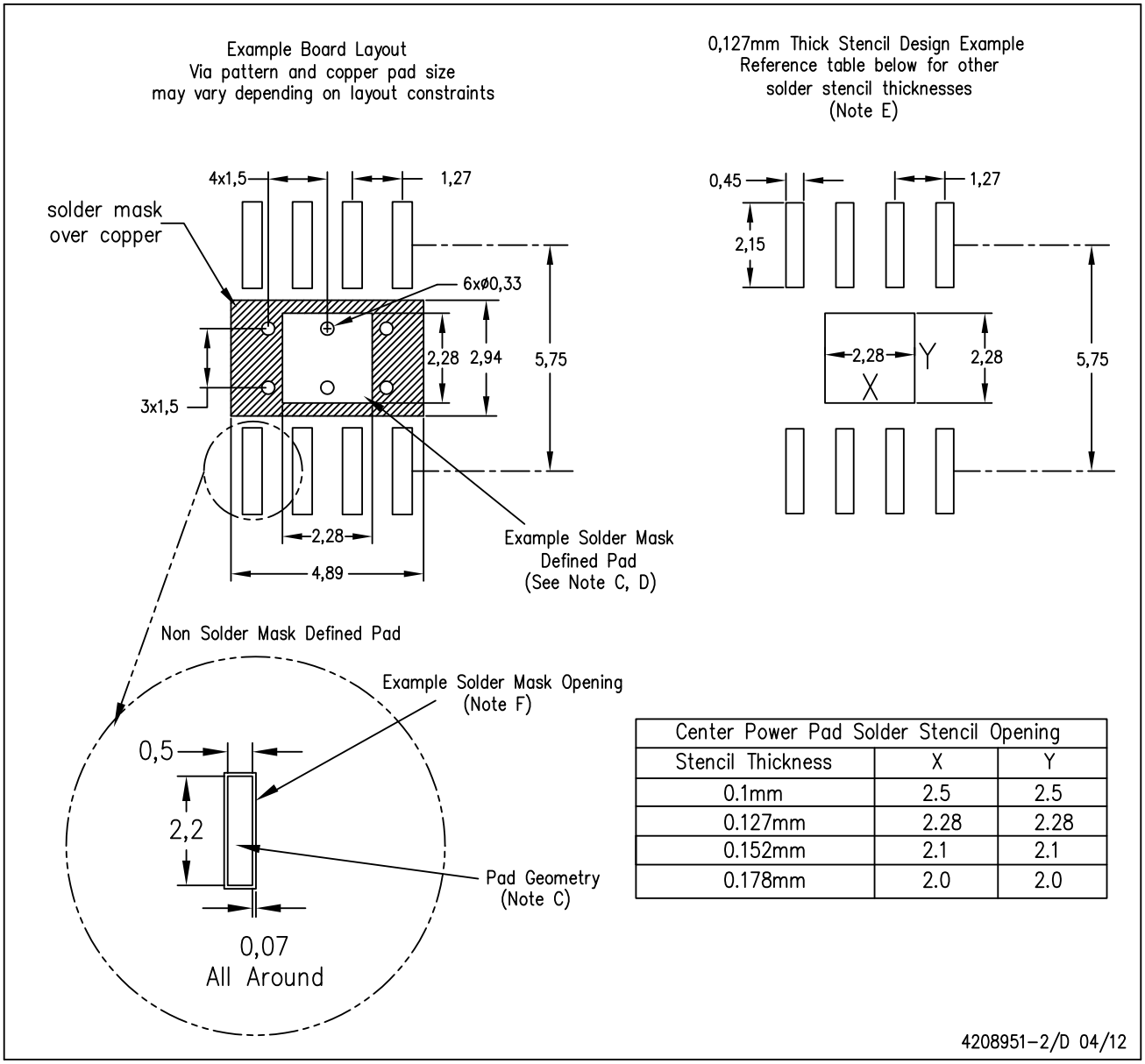
4206322–2/L 05/12

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

LAND PATTERN DATA

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



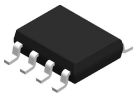
Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.5	2.5
0.127mm	2.28	2.28
0.152mm	2.1	2.1
0.178mm	2.0	2.0

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments.

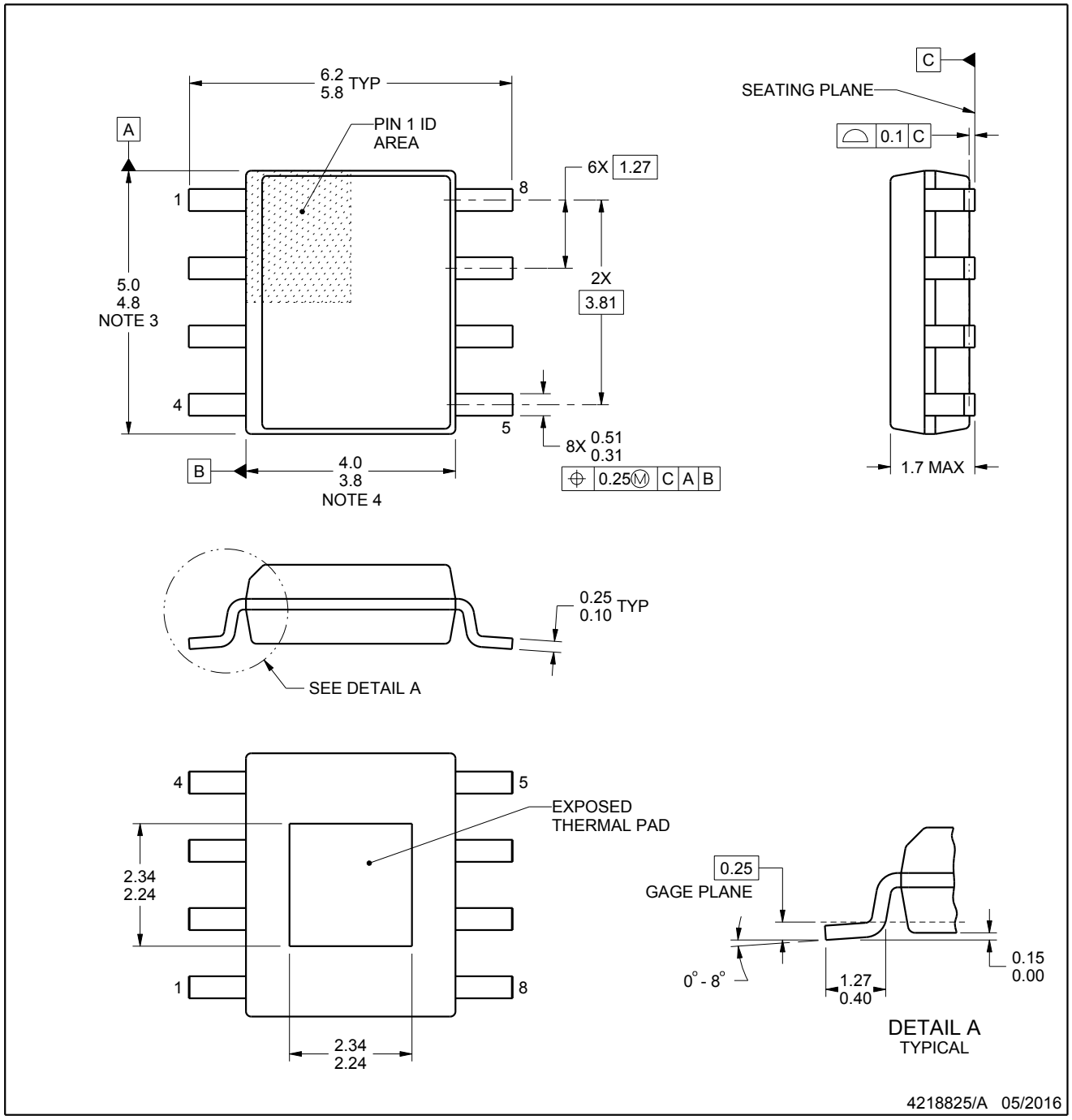
PACKAGE OUTLINE

DDA0008A



PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



PowerPAD is a trademark of Texas Instruments.

NOTES:

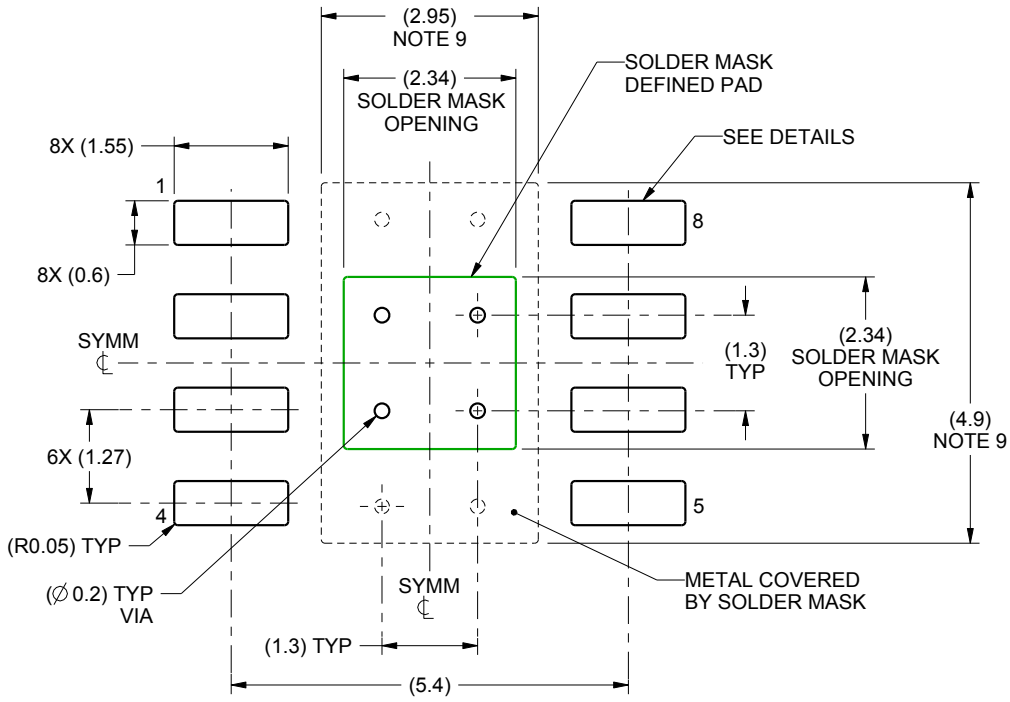
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.

EXAMPLE BOARD LAYOUT

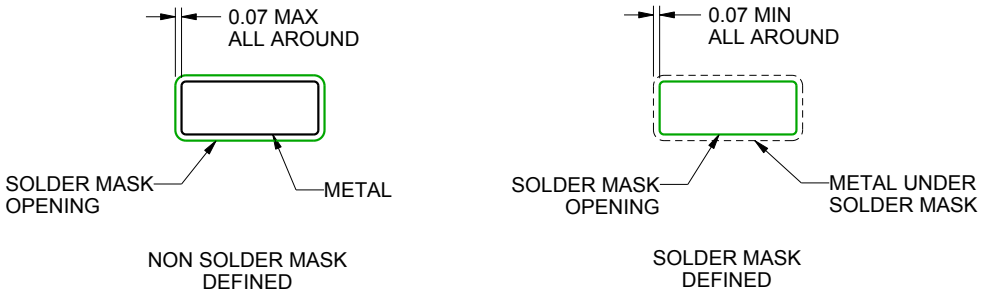
DDA0008A

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS

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NOTES: (continued)

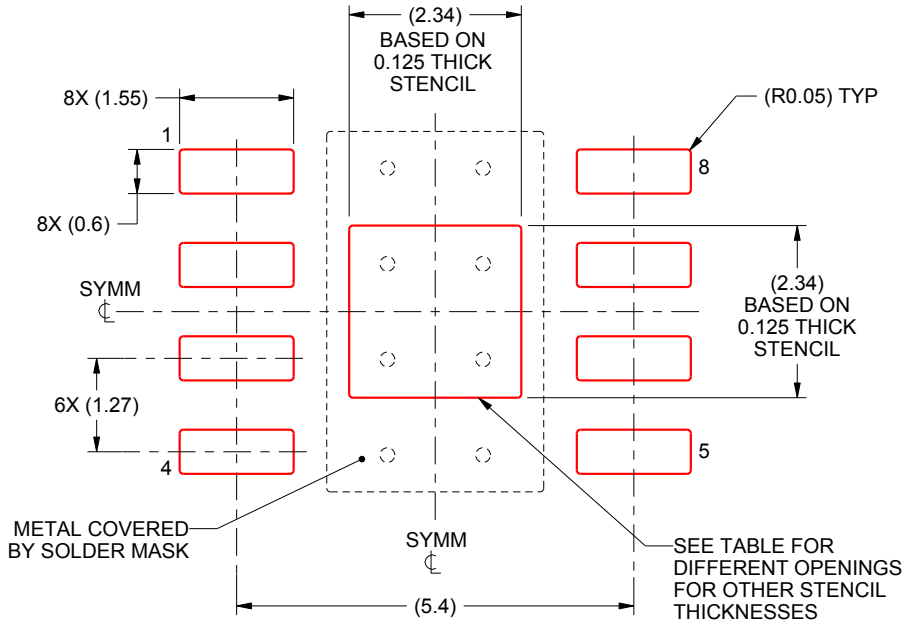
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DDA0008A

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.62 X 2.62
0.125	2.34 X 2.34 (SHOWN)
0.150	2.14 X 2.14
0.175	1.98 X 1.98

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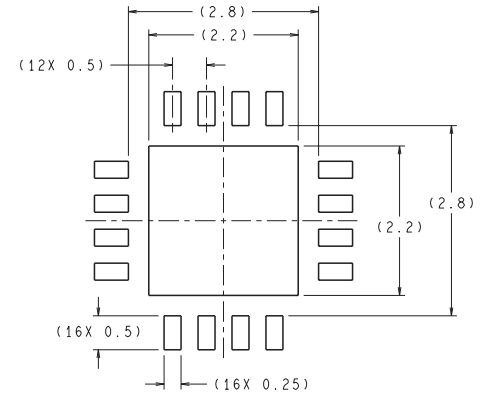
NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

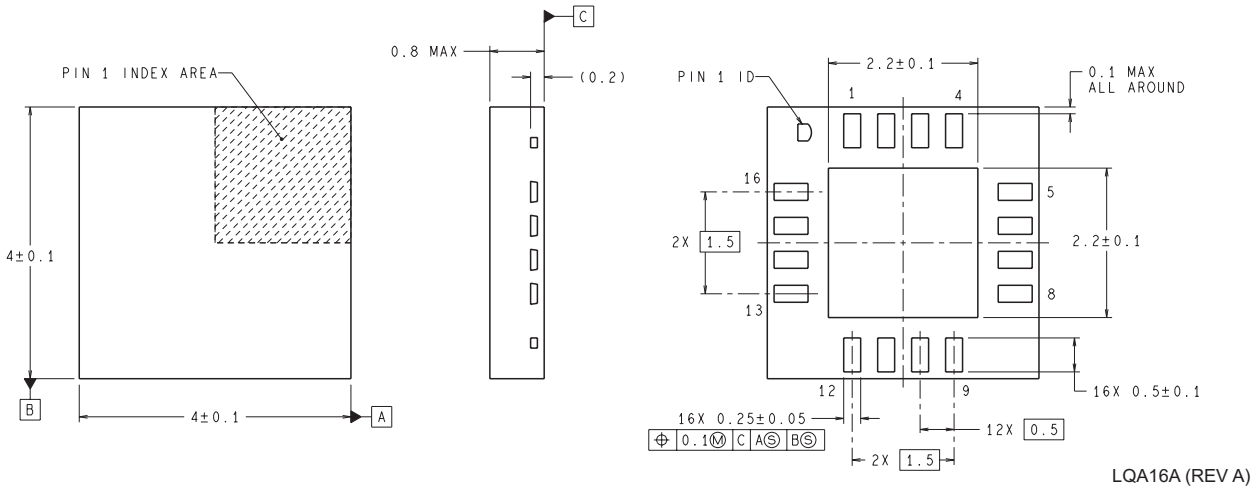
MECHANICAL DATA

NHP0016A



RECOMMENDED LAND PATTERN
1:1 RATION WITH PKG SOLDER PADS

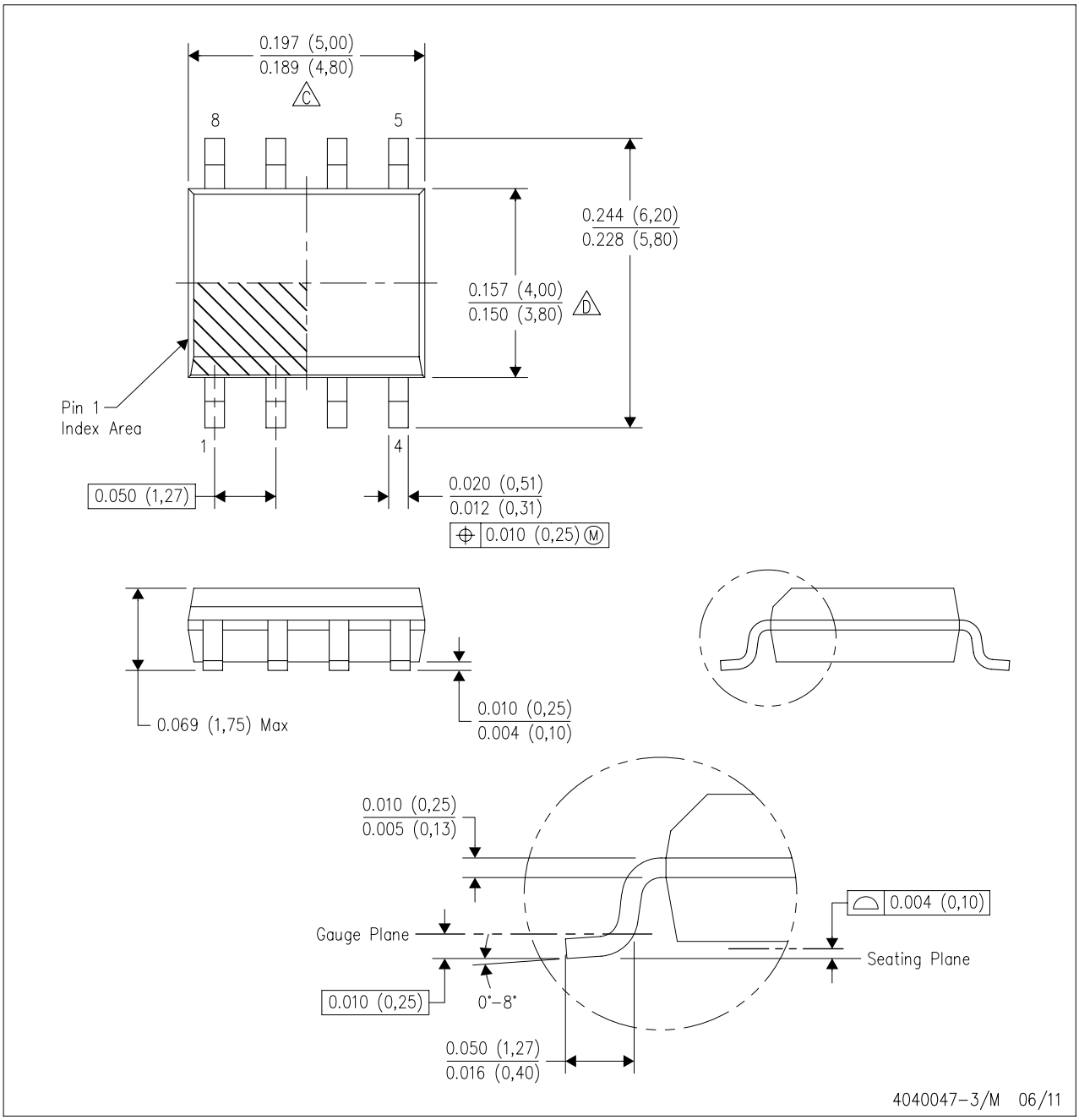
DIMENSIONS ARE IN MILLIMETERS



LQA16A (REV A)

MECHANICAL DATA

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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