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STMicroelectronics
HCF4067M013TR

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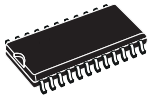
# HCF4067B

## ANALOG SINGLE 16 CHANNEL MULTIPLEXER/DEMULTIPLEXER

- LOW ON RESISTANCE : 125Ω (Typ.) OVER 15V p-p SIGNAL INPUT RANGE FOR $V_{DD}$ - $V_{SS}$ = 15V
- HIGH OFF RESISTANCE : CHANNEL LEAKAGE OF 10pA (Typ.) at $V_{DD}$ - $V_{SS}$ = 10V
- MATCHED SWITCH CHARACTERISTICS : $\Delta R_{ON}$ = 5Ω (Typ.) FOR $V_{DD}$ - $V_{SS}$ =15V
- VERY LOW QUIESCENT POWER DISSIPATION UNDER A DIGITAL CONTROL INPUT AND SUPPLY CONDITIONS : 0.2μW (Typ.) at $V_{DD}$ - $V_{SS}$ = 10V
- BINARY ADDRESS DECODING ON CHIP
- QUIESCENT CURRENT SPECIFIED UP TO 20V
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT LEAKAGE CURRENT $I_I$ = 100nA (MAX) AT $V_{DD}$ = 18V $T_A$ = 25°C
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B "STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"



SOP

### ORDER CODES

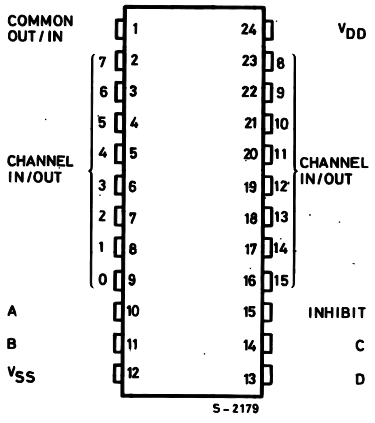
| PACKAGE | TUBE | T & R |
|---|---|---|
| SOP | HCF4067BM1 | HCF4067M013TR |

HCF4067B, analog multiplexer/demultiplexer CMOS, is a digitally controlled analog switches device having low ON impedance, low OFF leakage current and internal address decoding. In addition, the ON resistance is relatively constant over the full input-signal range.
HCF4067B ia a 16-channel multiplexer with four binary control inputs A, B, C, D, and an inhibit input, arranged so that any combination of the inputs selects one switch.

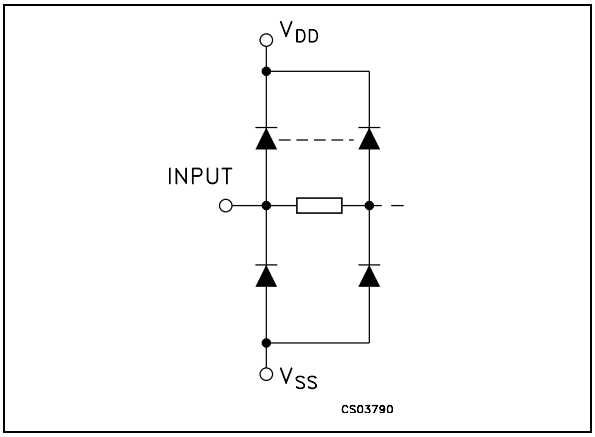
### DESCRIPTION

HCF4067B is monolithic integrated circuits fabricated in Metal Oxide Semiconductor technology available in SOP package.

### PIN CONNECTION



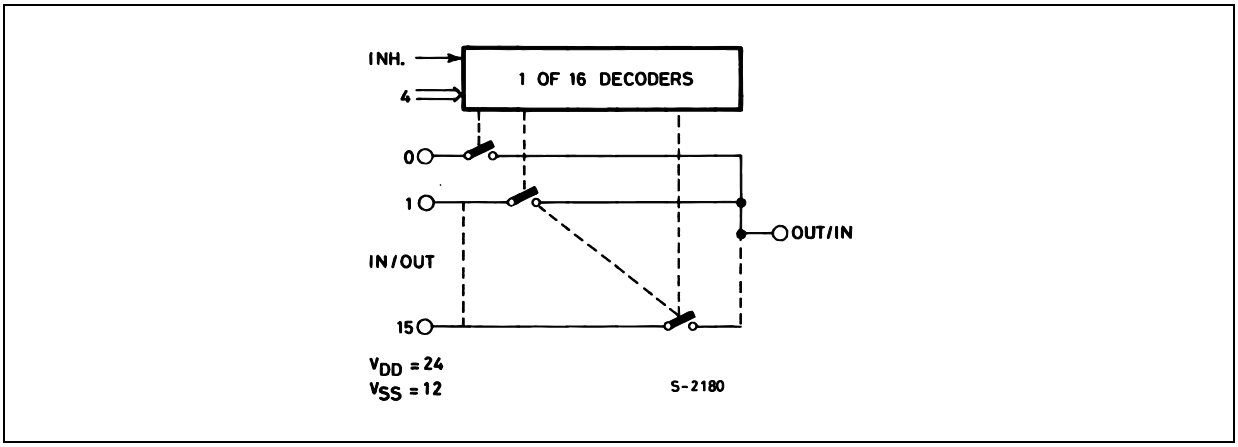
## INPUT EQUIVALENT CIRCUIT




## PIN DESCRIPTION

| PIN No | SYMBOL | NAME AND FUNCTION |
|---|---|---|
| 10, 11, 14, 13 | A, B, C, D | Binary Control Inputs |
| 1 | COMMON OUT/IN | Common Out/In |
| 15 | INHIBIT | Inhibit Input |
| 9, 8, 7, 6, 5, 4, 3, 2, 23, 22, 21, 20, 19, 18, 17, 16 | 0 to 15 CHANNEL IN/OUT | 16 channel In/Out |
| 12 | $V_{SS}$ | Negative Supply Voltage |
| 24 | $V_{DD}$ | Positive Supply Voltage |

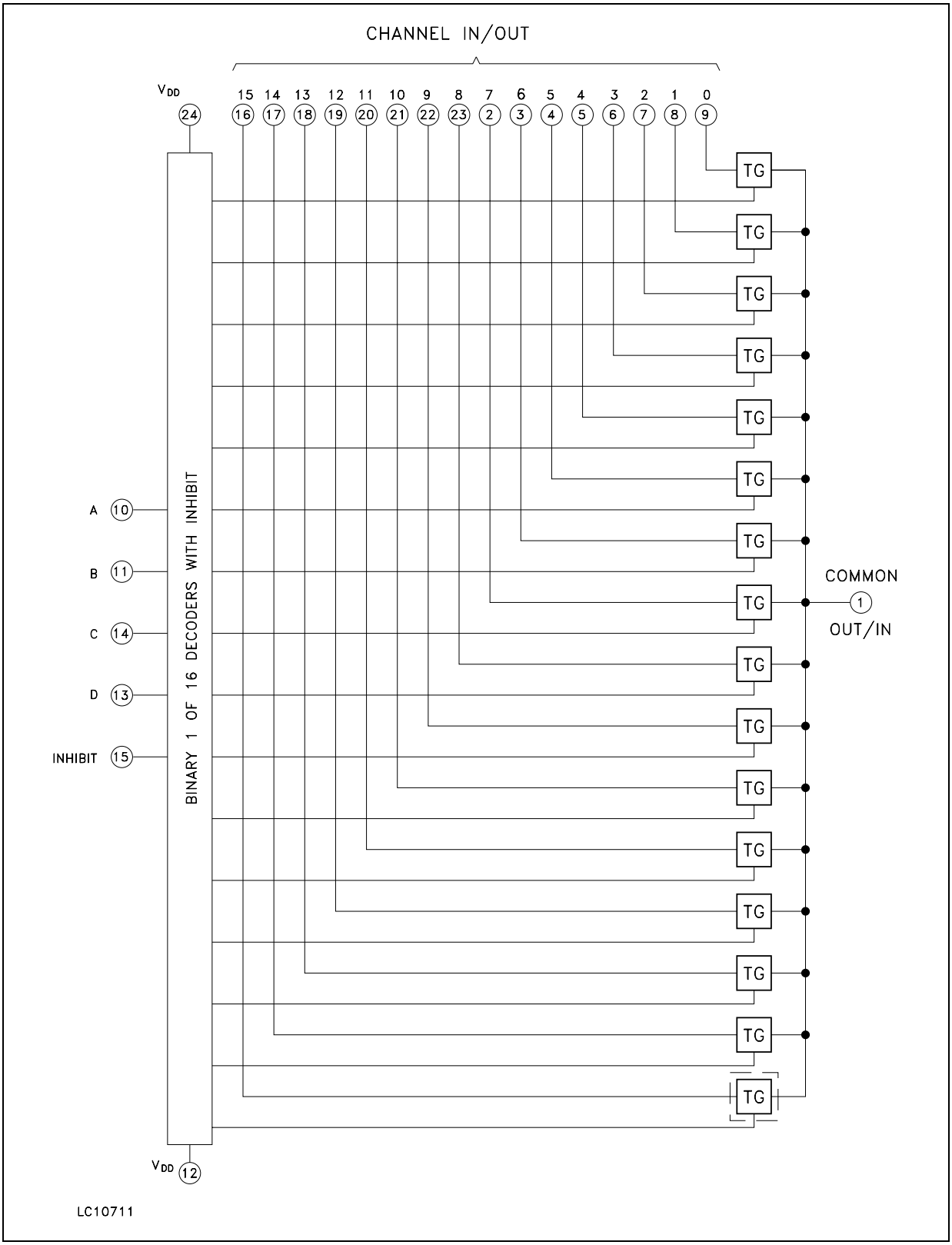
## FUNCTIONAL DIAGRAM




## TRUTH TABLE

| A | B | C | D | INH | SELECTED CHANNEL |
|---|---|---|---|---|---|
| X | X | X | X | H | NONE |
| L | L | L | L | L | 0 |
| H | L | L | L | L | 1 |
| L | H | L | L | L | 2 |
| H | H | L | L | L | 3 |
| L | L | H | L | L | 4 |
| H | L | H | L | L | 5 |
| L | H | H | L | L | 6 |
| H | H | H | L | L | 7 |
| L | L | L | H | L | 8 |
| H | L | L | H | L | 9 |
| L | H | L | H | L | 10 |
| H | H | L | H | L | 11 |
| L | L | H | H | L | 12 |
| H | L | H | H | L | 13 |
| L | H | H | H | L | 14 |
| H | H | H | H | L | 15 |

## LOGIC DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage | -0.5 to +22 | V |
| $V_I$ | DC Input Voltage | -0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current | ± 10 | mA |
| $P_D$ | Power Dissipation per Package | 200 | mW |
| | Power Dissipation per Output Transistor | 100 | mW |
| $T_{op}$ | Operating Temperature | -55 to +125 | °C |
| $T_{stg}$ | Storage Temperature | -65 to +150 | °C |

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.
All voltage values are referred to $V_{SS}$ pin voltage.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage | 3 to 20 | V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature | -55 to 125 | °C |

## STATIC ELECTRICAL CHARACTERISTICS

($T_{amb}$ = 25°C,Typical temperature coefficient for all $V_{DD}$ value is 0.3 %/°C)

| Symbol | Parameter | Test Condition | | | | Value | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_{IS}$ (V) | $V_{EE}$ (V) | $V_{SS}$ (V) | $V_{DD}$ (V) | $T_A$ = 25°C | | | -40 to 85°C | | -55 to 125°C | | |
| | | | | | | Min. | Typ. | Max. | Min. | Max. | Min. | Max. | |
| $I_L$ | Quiescent Supply Current | | | | 5 | | 0.04 | 5 | | 150 | | 150 | µA |
| | | | | | 10 | | 0.04 | 10 | | 300 | | 300 | |
| | | | | | 15 | | 0.04 | 20 | | 600 | | 600 | |
| | | | | | 20 | | 0.08 | 100 | | 3000 | | 3000 | |
| **SWITCH** | | | | | | | | | | | | | |
| $R_{ON}$ | On Resistance | $0 \le V_I \le V_{DD}$ | 0 | 0 | 5 | | 470 | 1050 | | 1200 | | 1200 | Ω |
| | | | | | 10 | | 180 | 400 | | 500 | | 520 | |
| | | | | | 15 | | 125 | 240 | | 300 | | 300 | |
| $\Delta_{ON}$ | Resistance $\Delta_{RON}$ (between any 2 of 4 switches) | | 0 | 0 | 5 | | 10 | | | | | | Ω |
| | | | | | 10 | | 10 | | | | | | |
| | | | | | 15 | | 5 | | | | | | |
| OFF (•) | Channel Leakage Current Any Channel Off | | 0 | 0 | 18 | | ±0.1 | 100 | | 1000 | | 1000 | µA |
| | Channel Leakage Current All Channel Off (Common Out/In) | | 0 | 0 | 18 | | ±0.1 | 100 | | 1000 | | 1000 | |
| C | Capacitance Input | | | -5 | 5 | | 5 | | | | | | pF |
| | Output capacitance | | | | | | 55 | | | | | | |
| | Feedthrough | | | | | | 0.2 | | | | | | |
| **CONTROL** | | | | | | | | | | | | | |
| $V_{IL}$ | Input Low Voltage | = VDD thru 1KΩ | $V_{EE}$ = $V_{SS}$ $R_L$ = 1KΩ to $V_{SS}$ $I_{IS}$ < 2µA (on all OFF channels) | | 5 | | | 1.5 | | 1.5 | | 1.5 | V |
| | | | | | 10 | | | 3 | | 3 | | 3 | |
| | | | | | 15 | | | 4 | | 4 | | 4 | |
| $V_{IH}$ | Input High Voltage | | | | 5 | 3.5 | | | 3.5 | | 3.5 | | V |
| | | | | | 10 | 7 | | | 7 | | 7 | | |
| | | | | | 15 | 11 | | | 11 | | 11 | | |
| $I_I$ | Input Leakage Current | $V_I$ = 0/18V | | | 18 | | $\pm 10^{-3}$ | ±0.1 | | ±1 | | ±1 | µA |
| $C_I$ | Input Capacitance | Any Address or Inhibit Input | | | | | 5 | 7.5 | | | | | pF |

The Noise Margin for both "1" and "0" level is: 1V min. with $V_{DD}$=5V, 2V min. with $V_{DD}$=10V, 2.5V min. with $V_{DD}$=15V

• Determined by minimum feasible leakage measurement for automating testing

**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200KΩ, $t_r = t_f$ = 20 ns)

| Symbol | Parameter | Test Condition | | | | | | | Value* | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_C$ (V) | $R_L$ (KΩ) | $f_I$ (KHz) | $V_I$ (V) | $V_{SS}$ (V) | $V_{DD}$ (V) | | Typ. | Max. | |
| **SWITCH** | | | | | | | | | | | |
| $t_{pd}$ | Propagation Delay Time (Signal Input to Output) | = $V_{DD}$ | 200 | | | 0 | 5 | | 30 | 60 | ns |
| | | | | | | | 10 | | 15 | 30 | |
| | | | | | | | 15 | | 11 | 20 | |
| | Frequency Response Channel "ON" (Sine Wave Input) at $20 \text{ Log } \frac{V_O}{V_I}$ = -3dB | = $V_{DD}$ | 1 | | 5 (•) | 0 | 10 | $V_O$ at Common Out/In | 14 | | ns |
| | | | | | | | | $V_O$ at Any Channel | 60 | | |
| | Feedthrough (All channels OFF) at $20 \text{ Log } \frac{V_O}{V_I}$ =-40dB | = $V_{SS}$ | 1 | | 5 (•) | 0 | 10 | $V_O$ at Common Out/In | 20 | | MHz |
| | | | | | | | | $V_O$ at Any Channel | 8 | | |
| | Frequency Signal Crosstalk at $20 \text{ Log } \frac{V_{O(A)}}{V_{I(B)}}$=-40dB | $V_{C(A)}$ =$V_{DD}$ $V_{C(B)}$ =$V_{SS}$ | 1 | | 5 (•) | 0 | 10 | Between Any two (A and B) Channels | 1 | | MHz |
| $t_W$ | Sine Wave Distortion ($f_{IS}$ = 1KHz sine wave) | 5 | 10 | 1 | 2 (•) | 0 | 5 | | 0.3 | | % |
| | | 10 | | | 3 (•) | | 10 | | 0.2 | | |
| | | 15 | | | 5 (•) | | 15 | | 0.12 | | |
| **CONTROL**(Address or Inhibit) | | | | | | | | | | | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay Time:Address or Inhibit to Signal OUT (Channel Turning ON) | | 1 | | | 0 | 5 | | 325 | 650 | ns |
| | | | | | | | 10 | | 135 | 270 | |
| | | | | | | | 15 | | 95 | 190 | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay Time:Address or Inhibit to Signal OUT (Channel Turning OFF) | | 0.3 | | | 0 | 5 | | 220 | 440 | ns |
| | | | | | | | 10 | | 90 | 180 | |
| | | | | | | | 15 | | 65 | 130 | |
| | Address or Inhibit to Signal Crosstalk | | 10** | | | 0 | 10 | | 75 | | mV peak |

(*) Typical temperature coefficient for all $V_{DD}$ value is 0.3 %/°C
(**) : Both Ends of Channel
(•) : Peak to Peak voltage symmetrical about ($V_{DD}$ - $V_{SS}$) / 2

## APPLICATION INFORMATION

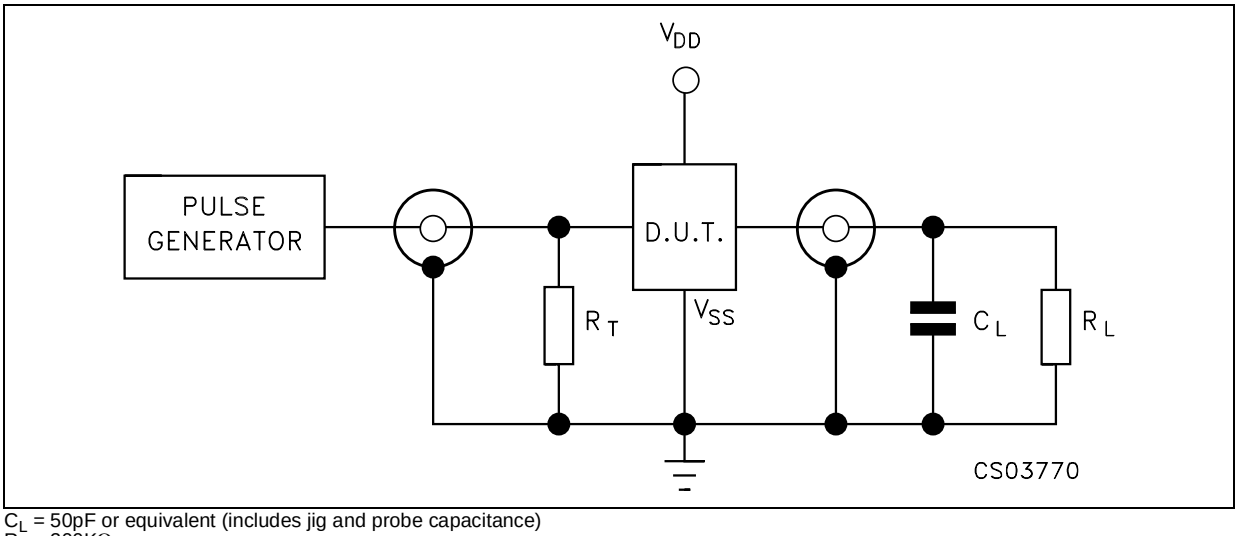
In applications where separate power sources are used to drive $V_{DD}$ and the signal inputs, the $V_{DD}$ current capability should exceed $V_{DD}/R_L$ ($R_L$ = effective external load). This provision avoids permanent current flow or clamp action on the $V_{DD}$ supply when power is applied or removed from the HCF4067B.

When switching from one address to another, some of the ON periods of the channels of the multiplexers will overlap momentarily, which may be objectionable in certain applications. Also, when a channel is turned ON or OFF by an address input, there is a momentary conductive path from the channel to $V_{SS}$, which will dump some charge from any capacitor connected to the input or output of the channel. The inhibit input turning on a channel will similarly dump some charge to $V_{SS}$.

The amount of charge dumped is mostly a function of the signal level above $V_{SS}$. Typically, at $V_{DD} - V_{SS} = 10V$, a 100 pF capacitor connected to the input or output of the channel will lose 3-4% of its voltage at the moment the channel turns ON or OFF. This loss of voltage is essentially independent of the address or inhibit signal transition time, if the transition time is less than 1-2 ms. When the inhibit signal turns a channel off, there is no change dumping of $V_{SS}$. Rather, there is a slight rise in the channel voltage level (65 mV typ.) due to the capacitance coupling from inhibit input to channel input or output. Address input also couple some voltage steps onto the channel signal levels.

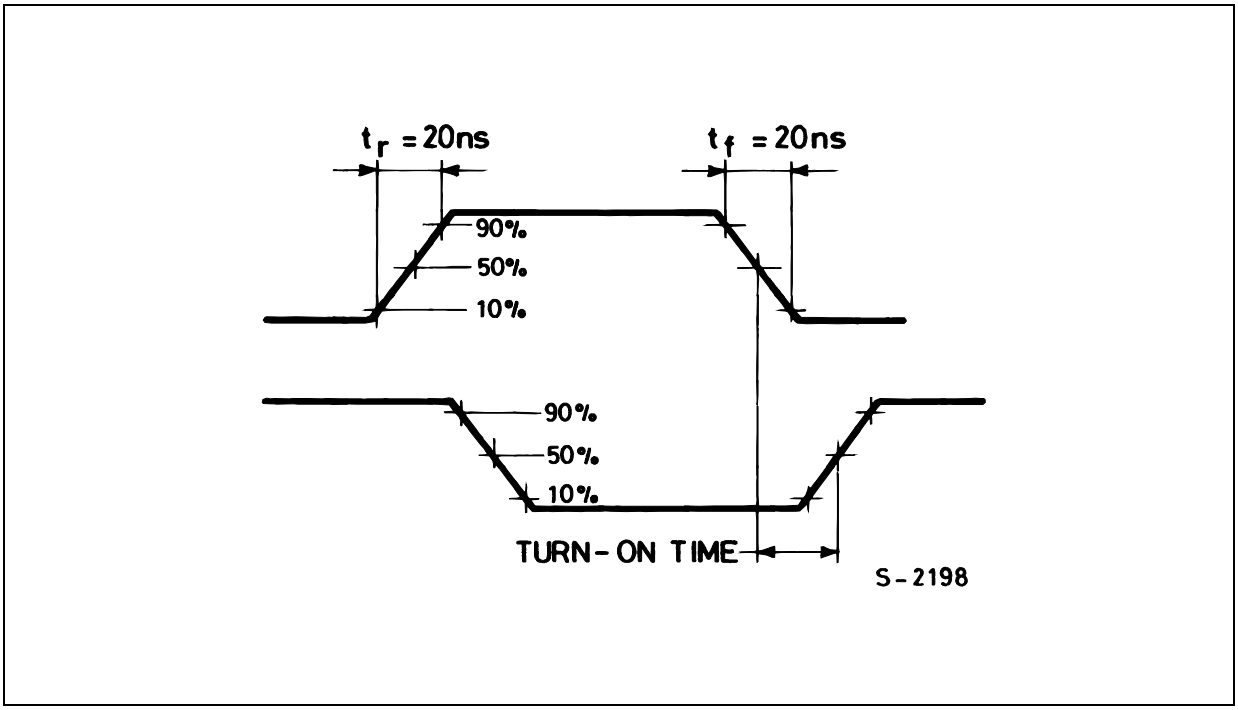
In certain applications, the external load-resistor current may include both $V_{DD}$ and signal line components. To avoid drawing $V_{DD}$ current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.8V (calculated from $R_{ON}$ values shown in ELECTRICAL CHARACTERISTICS CHART). No $V_{DD}$ current will flow through $R_L$ if the switch current flows into terminal 1 on the HCF4067B.

## TEST CIRCUIT

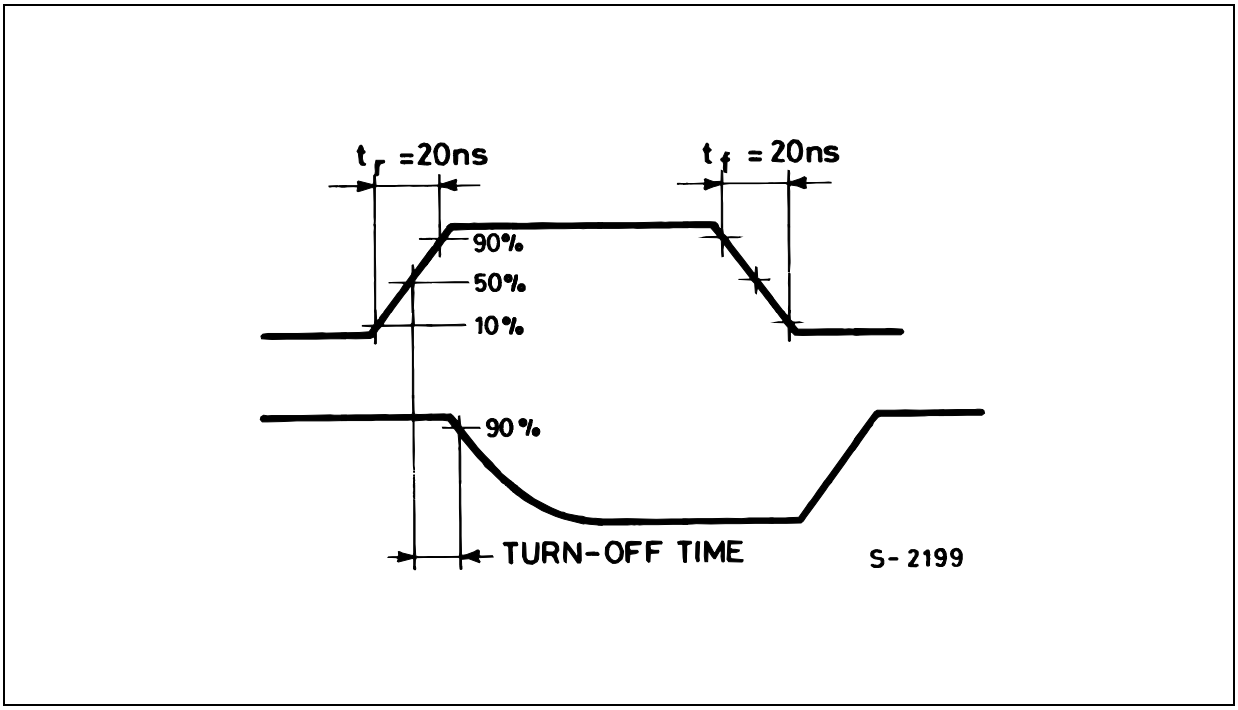



$C_L$ = 50pF or equivalent (includes jig and probe capacitance)
$R_L$ = 200KΩ
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

**WAVEFORM : PROPAGATION DELAY TIMES** (f=1MHz; 50% duty cycle)

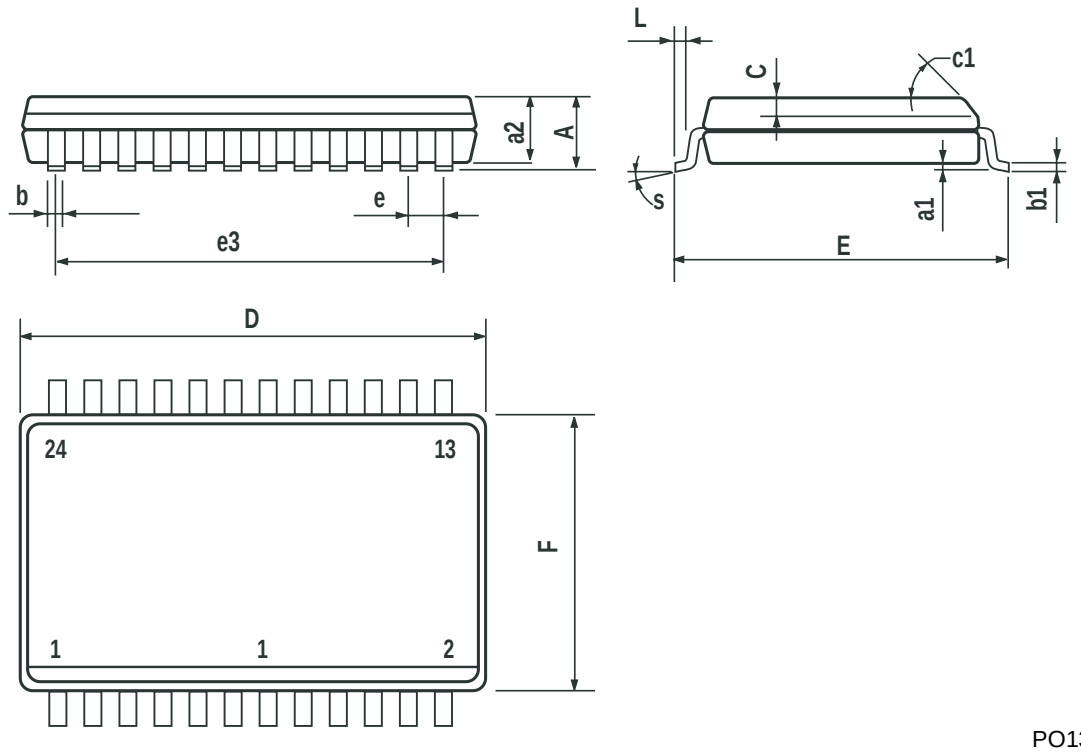



**WAVEFORM : PROPAGATION DELAY TIMES** (f=1MHz; 50% duty cycle)



## SO-24 MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | | | 2.65 | | | 0.104 |
| a1 | 0.1 | | 0.2 | 0.004 | | 0.008 |
| a2 | | | 2.45 | | | 0.096 |
| b | 0.35 | | 0.49 | 0.014 | | 0.019 |
| b1 | 0.23 | | 0.32 | 0.009 | | 0.012 |
| C | | 0.5 | | | 0.020 | |
| c1 | 45° (typ.) | | | | | |
| D | 15.20 | | 15.60 | 0.598 | | 0.614 |
| E | 10.00 | | 10.65 | 0.393 | | 0.419 |
| e | | 1.27 | | | 0.050 | |
| e3 | | 13.97 | | | 0.550 | |
| F | 7.40 | | 7.60 | 0.291 | | 0.300 |
| L | 0.50 | | 1.27 | 0.020 | | 0.050 |
| S | 8° (max.) | | | | | |




PO13T