Excellent Integrated System Limited

Stocking Distributor

Click to view price, real time Inventory, Delivery & Lifecycle Information:

STMicroelectronics
VNN1NV0413TR

For any questions, you can email us directly:
sales@integrated-circuit.com

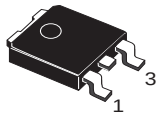
VND1NV04
VNN1NV04 - VNS1NV04

OMNIFET II
fully autoprotected Power MOSFET

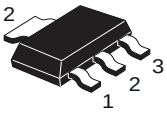
Features

Parameter	Symbol	Value
Max on-state resistance (per ch.)	R_{ON}	250 mΩ
Current limitation (typ)	I_{LIMH}	1.7 A
Drain-source clamp voltage	V_{CLAMP}	40 V

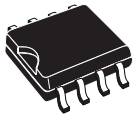
- Linear current limitation
- Thermal shutdown
- Short circuit protection
- Integrated clamp
- Low current drawn from input pin
- Diagnostic feedback through input pin
- ESD protection
- Direct access to the gate of the Power MOSFET (analog driving)
- Compatible with standard Power MOSFET



TO-252 (DPAK)



SOT-223



SO-8

Description

The VND1NV04, VNN1NV04, VNS1NV04 are monolithic devices designed in STMicroelectronics® VIPower® M0-3 Technology, intended for replacement of standard Power MOSFETs from DC up to 50 KHz applications. Built in thermal shutdown, linear current limitation and overvoltage clamp protect the chip in harsh environments.

Fault feedback can be detected by monitoring the voltage at the input pin.

Table 1. Device summary

Package	Order codes			
	Tube	Tube (lead free)	Tape and reel	Tape and reel (lead free)
TO-252 (DPAK)	VND1NV04	VND1NV04-E	VND1NV0413TR	VND1NV04TR-E
SOT-223	VNN1NV04	-	VNN1NV0413TR	-
SO-8	VNS1NV04	-	VNS1NV0413TR	-

Contents

List of tables

List of figures

1 Block diagram and pin description

Figure 1. Block diagram

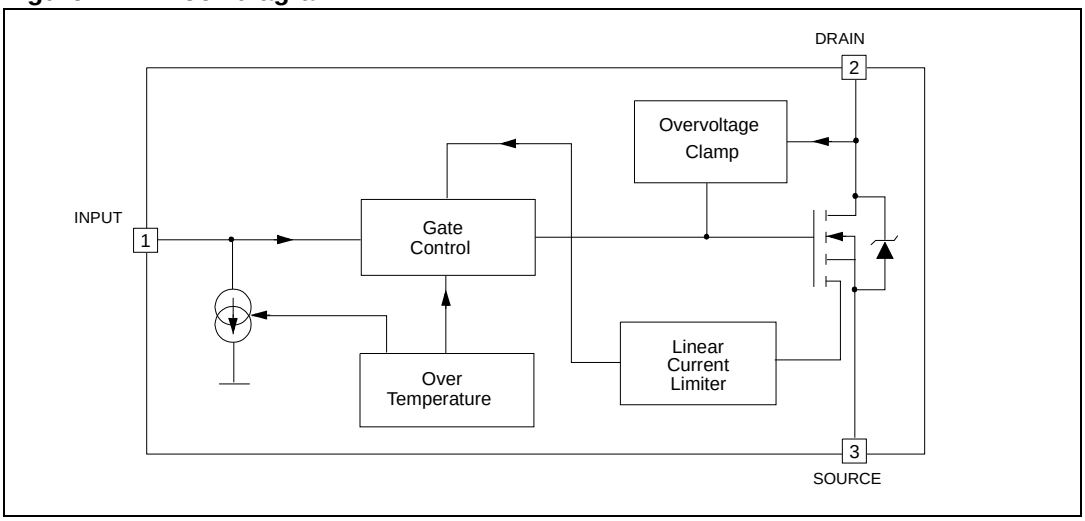
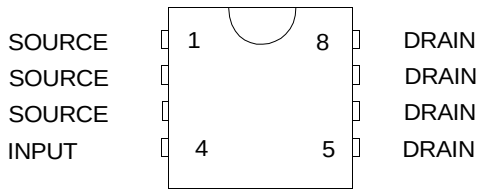


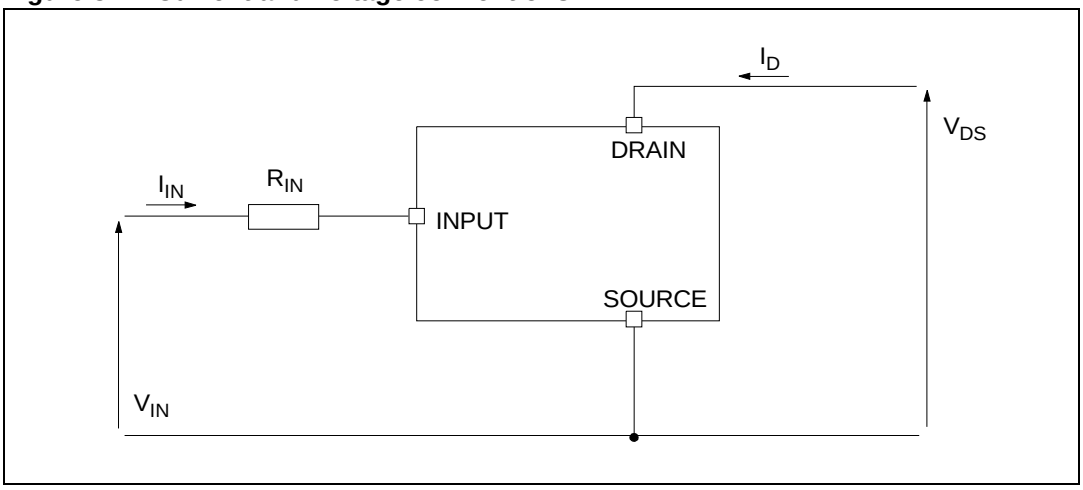
Figure 2. Configuration diagram (top view)



1. For the pins configuration related to SOT-223 and DPAK see outline at page 1.

2 Electrical specifications

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

The rating listed in *Table 2: Absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to Absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute maximum ratings

Symbol	Parameter	Value			Unit
		SOT-223	SO-8	DPAK	
V_{DSn}	Drain-source voltage (V_{INn}=0 V)	Internally clamped			V
V_{INn}	Input voltage	Internally clamped			V
I_{INn}	Input current	+/-20			mA
$R_{IN\ MINn}$	Minimum input series impedance	330			Ω
I_{Dn}	Drain current	Internally limited			A
I_{Rn}	Reverse DC output current	-3			A
V_{ESD1}	Electrostatic discharge (R=1.5 KΩ, C=100 pF)	4000			V
V_{ESD2}	Electrostatic discharge on output pins only (R=330 Ω, C=150 pF)	16500			V
P_{tot}	Total dissipation at T_c=25 °C	7	8.3	35	W
T_j	Operating junction temperature	Internally limited			°C
T_c	Case operating temperature	Internally limited			°C
T_{stg}	Storage temperature	-55 to 150			°C

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Maximum value			Unit
		SOT-223	SO-8	DPAK	
$R_{thj\text{-}case}$	Thermal resistance junction-case	18		3.5	°C/W
$R_{thj\text{-}lead}$	Thermal resistance junction-lead		15		°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	70(1)	65(1)	54(1)	°C/W

1. When mounted on a standard single-sided FR4 board with 50 mm^2 of Cu (at least 35 µm thick) connected to all DRAIN pins

2.3 Electrical characteristics

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Off (-40 °C<Tj<150 °C, unless otherwise specified)						
V_{CLAMP}	Drain-source clamp voltage	V_{IN}=0 V; I_D=0.5 A	40	45	55	V
V_{CLTH}	Drain-source clamp threshold voltage	V_{IN}=0 V; I_D=2 mA	36			V
V_{INTH}	Input threshold voltage	V_{DS}=V_{IN}; I_D=1 mA	0.5		2.5	V
I_{ISS}	Supply current from input pin	V_{DS}=0 V; V_{IN}=5 V		100	150	µA
V_{INCL}	Input-source clamp voltage	I_{IN}=1 mA	6	6.8	8	V
		I_{IN}=-1 mA	-1.0		-0.3	
I_{DSS}	Zero input voltage drain current (V_{IN}=0 V)	V_{DS}=13 V; V_{IN}=0 V; T_j=25 °C			30	µA
		V_{DS}=25 V; V_{IN}=0 V			75	
On (-40 °C<Tj<150 °C, unless otherwise specified)						
$R_{DS(on)}$	Static drain-source on resistance	V_{IN}=5 V; I_D=0.5 A; T_j=25 °C			250	mΩ
		V_{IN}=5 V; I_D=0.5 A			500	
Dynamic (T_j=25 °C, unless otherwise specified)						
g_{fs} (1)	Forward transconductance	V_{DD}=13 V; I_D=0.5 A		2		S
C_{OSS}	Output capacitance	V_{DS}=13 V; f=1 MHz; V_{IN}=0 V		90		pF

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Switching (T_j=25 °C, unless otherwise specified)						
$t_{d(on)}$	Turn-on delay time	V_{DD}=15 V; I_D=0.5 A V_{gen}=5 V; R_{gen}=$R_{IN\ MIN}$=330 Ω (see *Figure 4*)		70	200	ns
t_r	Rise time			170	500	ns
$t_{d(off)}$	Turn-off delay time			350	1000	ns
t_f	Fall time			200	600	ns
$t_{d(on)}$	Turn-on delay time	V_{DD}=15 V; I_D=0.5 A V_{gen}=5 V; R_{gen}=2.2 KΩ (see *Figure 4*)		0.25	1.0	µs
t_r	Rise time			1.3	4.0	µs
$t_{d(off)}$	Turn-off delay time			1.8	5.5	µs
t_f	Fall time			1.2	4.0	µs
$(dI/dt)_{on}$	Turn-on current slope	V_{DD}=15 V; I_D=1.5 A V_{gen}=5 V; R_{gen}=$R_{IN\ MIN}$=330 Ω		5		A/µs
Q_i	Total input charge	V_{DD}=12 V; I_D=0.5 A; V_{IN}=5 V I_{gen}=2.13 mA (see *Figure 7*)		5		nC
Source drain diode (T_j=25 °C, unless otherwise specified)						
V_{SD}(1)	Forward on voltage	I_{SD}=0.5 A; V_{IN}=0 V		0.8		V
t_{rr}	Reverse recovery time	I_{SD}=0.5 A; dI/dt=6 A/µs V_{DD}=30 V; L=200 µH (see *Figure 5*)		205		ns
Q_{rr}	Reverse recovery charge			100		nC
I_{RRM}	Reverse recovery current			0.7		A
Protections (-40 °C<T_j<150 °C, unless otherwise specified)						
I_{lim}	Drain current limit	V_{IN}=5 V; V_{DS}=13 V	1.7		3.5	A
t_{dlim}	Step response current limit	V_{IN}=5 V; V_{DS}=13 V		2.0		µs
T_{jsh}	Overtemperature shutdown		150	175	200	°C
T_{jrs}	Overtemperature reset		135			°C
I_{gf}	Fault sink current	V_{IN}=5 V; V_{DS}=13 V; T_j=T_{jsh}	10	15	20	mA
E_{as}	Single pulse avalanche energy	Starting T_j=25 °C; V_{DD}=24 V V_{IN}=5 V R_{gen}=$R_{IN\ MIN}$=330 Ω; L=50 mH (see *Figure 6* and *Figure 8*)	55			mJ

1. Pulsed: pulse duration = 300 µs, duty cycle 1.5 %

Figure 4. Switching time test circuit for resistive load

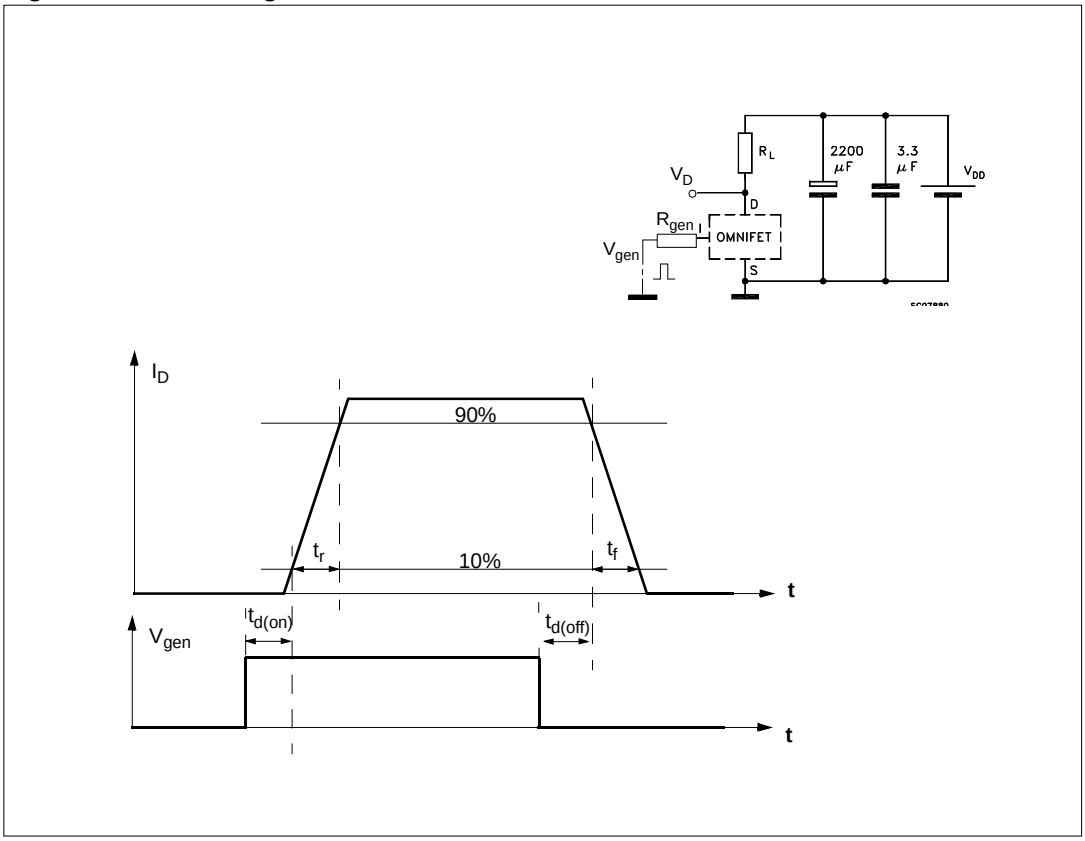


Figure 5. Test circuit for diode recovery times

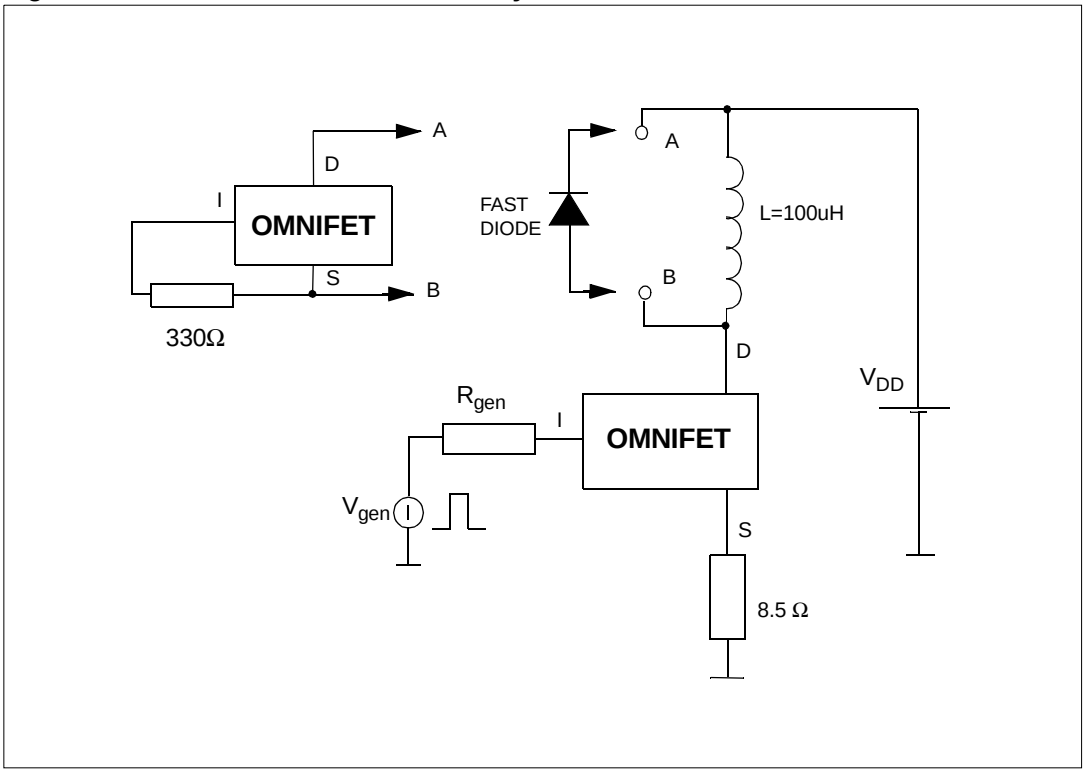


Figure 6. Unclamped inductive load test circuits

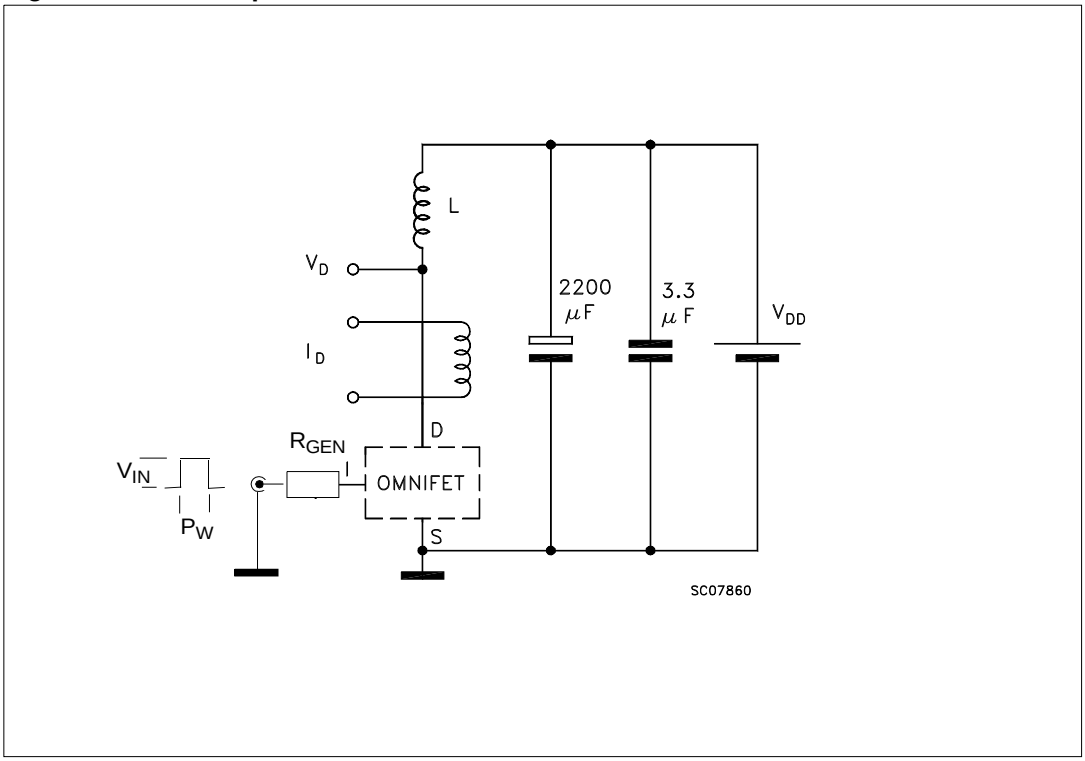


Figure 7. Input charge test circuit

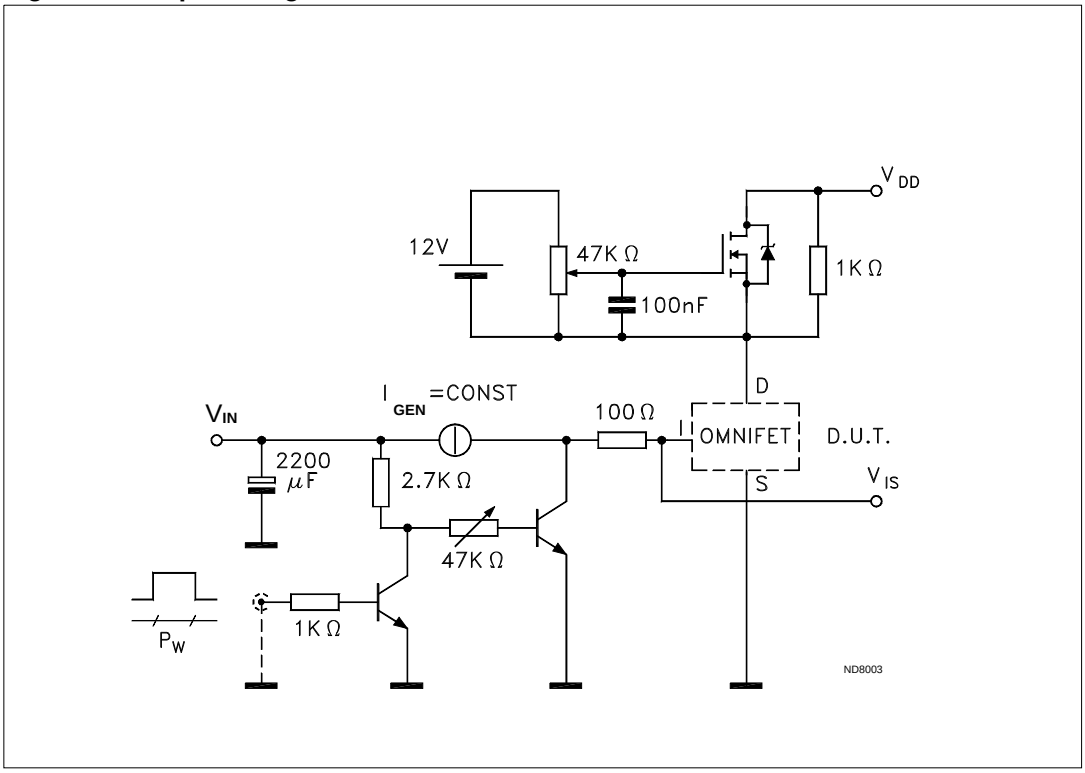
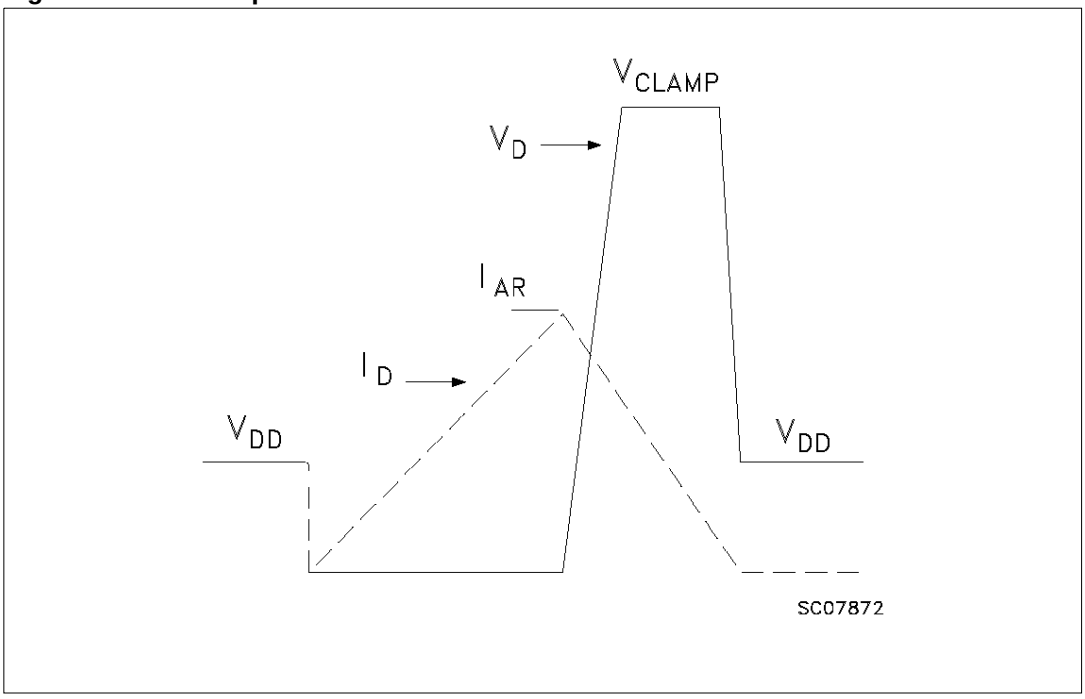


Figure 8. Unclamped inductive waveforms



2.4 Electrical characteristics curves

Figure 9. Source-drain diode forward characteristics

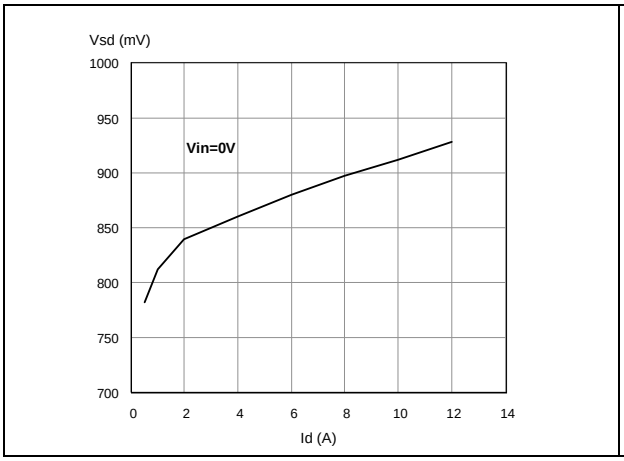


Figure 10. Static drain-source on resistance

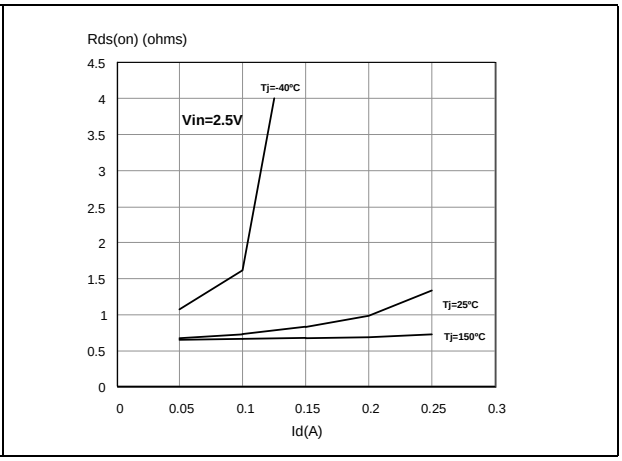


Figure 11. Derating curve

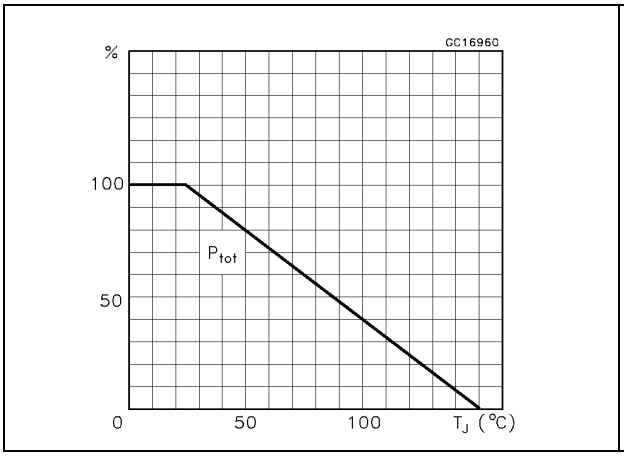


Figure 12. Static drain-source on resistance vs. input voltage (part 1/2)

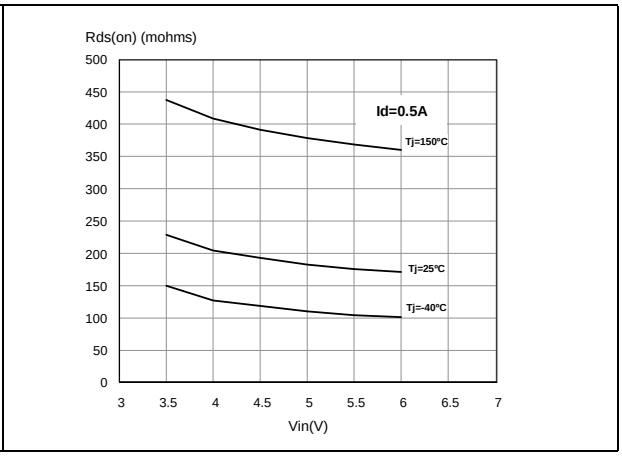


Figure 13. Static drain-source on resistance vs. input voltage (part 2/2)

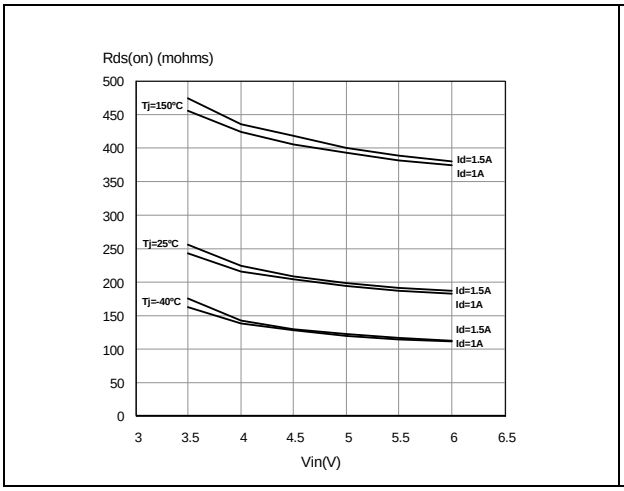


Figure 14. Transconductance

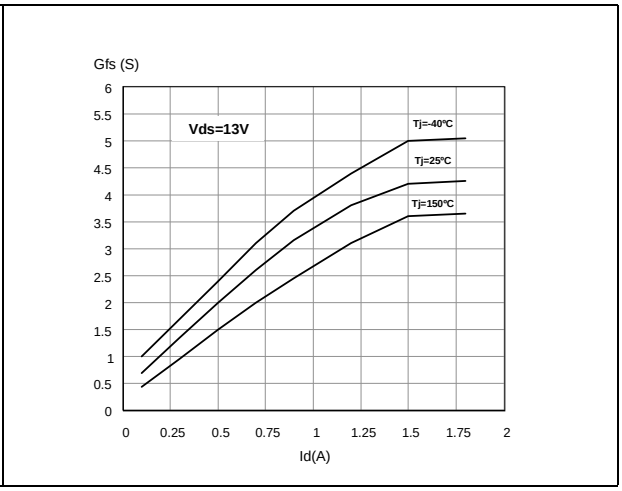


Figure 15. Static drain-source on resistance vs. Id

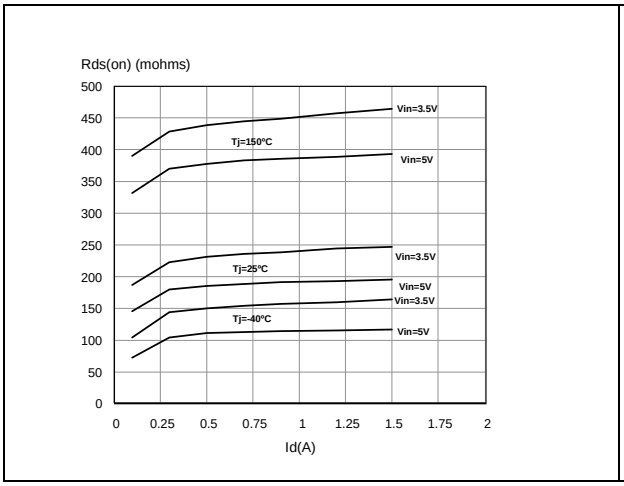


Figure 16. Transfer characteristics

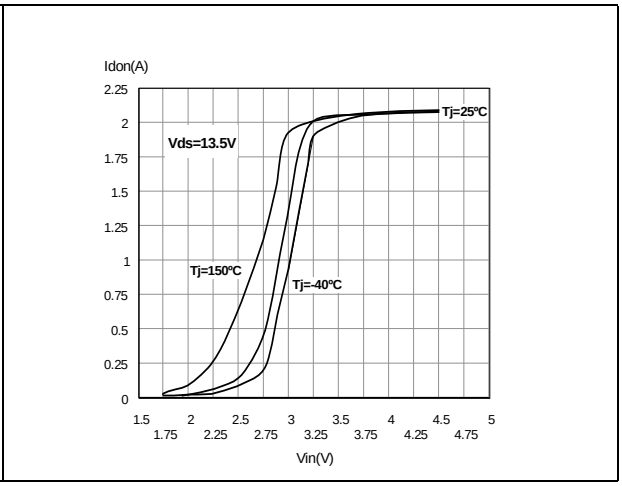


Figure 17. Turn-on current slope (part 1/2)

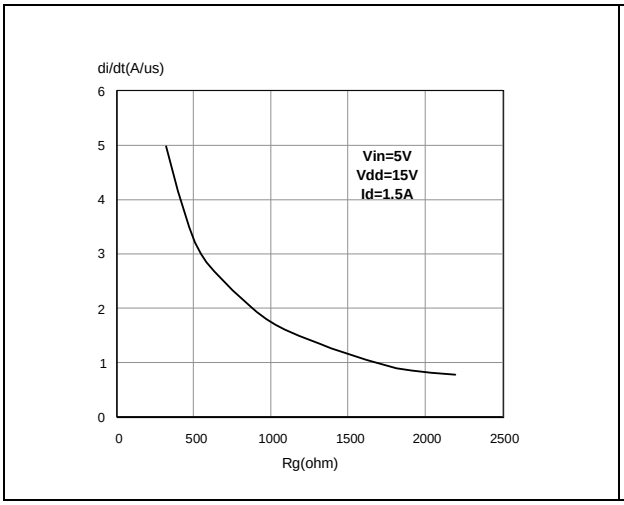


Figure 18. Turn-on current slope (part 2/2)

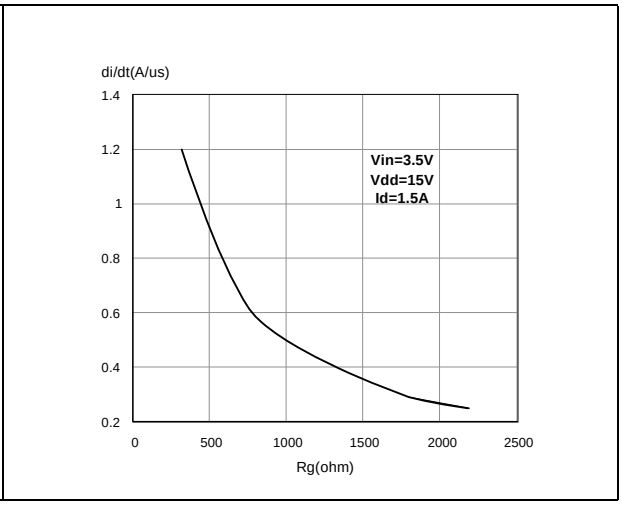


Figure 19. Input voltage vs. input charge

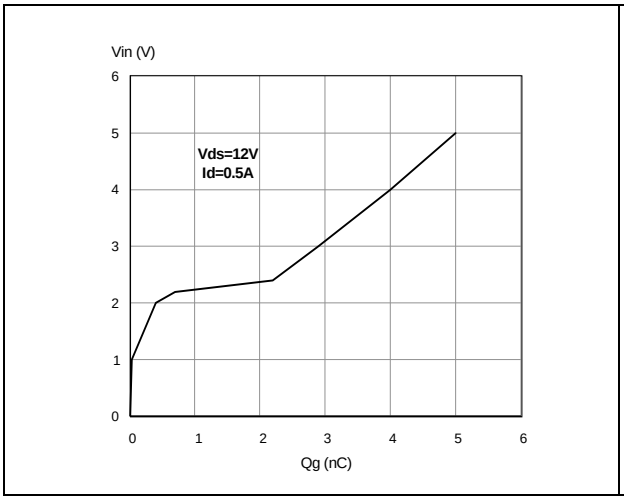


Figure 20. Turn-off drain source voltage slope (part 1/2)

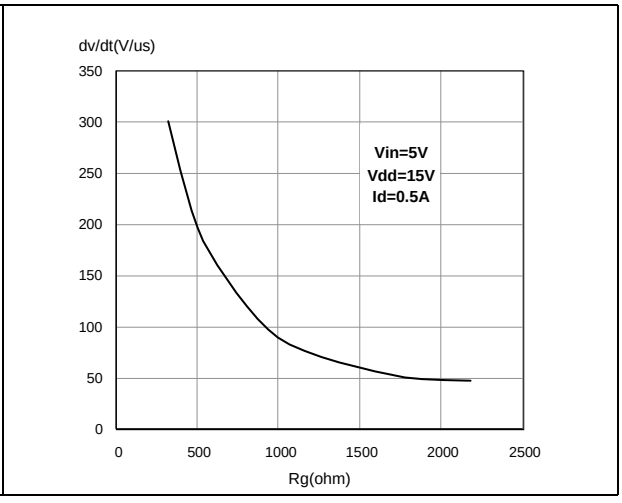


Figure 21. Turn-off drain-source voltage slope (part 2/2)

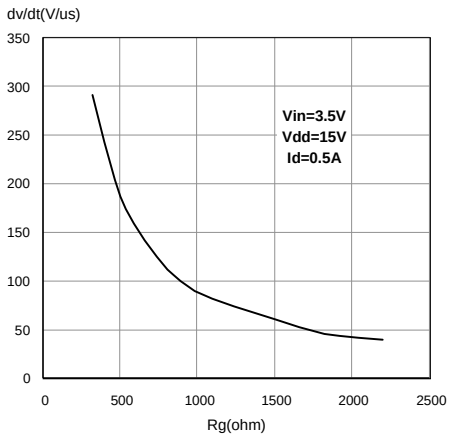


Figure 22. Capacitance variations

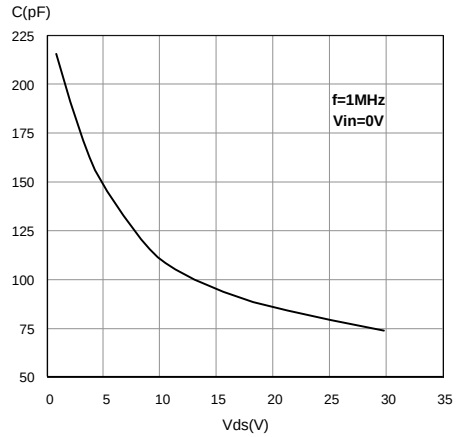


Figure 23. Switching time resistive load (part 1/2)

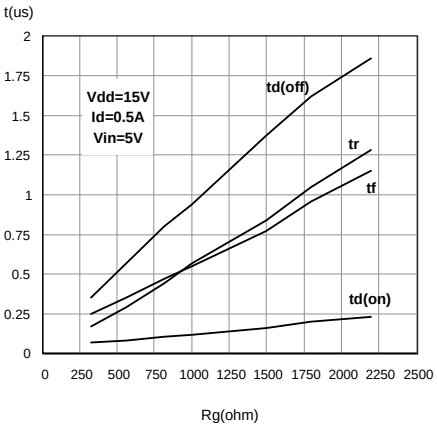


Figure 24. Switching time resistive load (part 2/2)

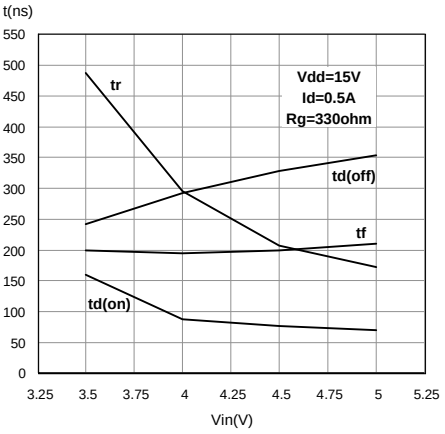


Figure 25. Output characteristics

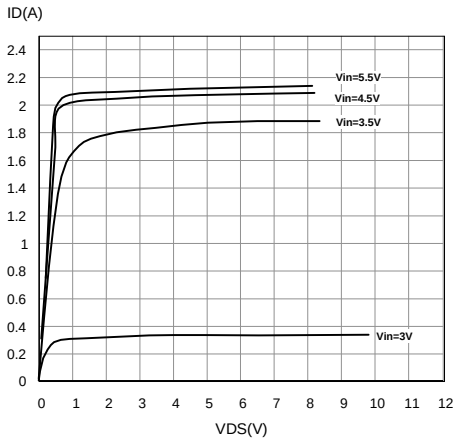


Figure 26. Normalized on resistance vs. temperature

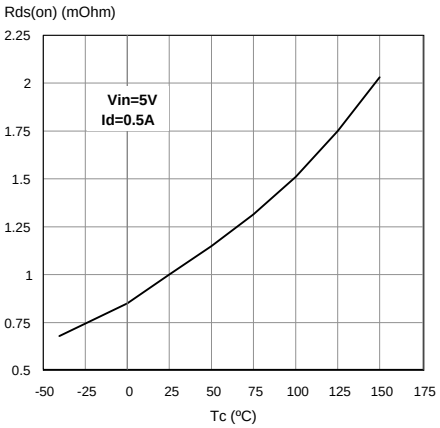


Figure 27. Normalized input threshold voltage vs. temperature

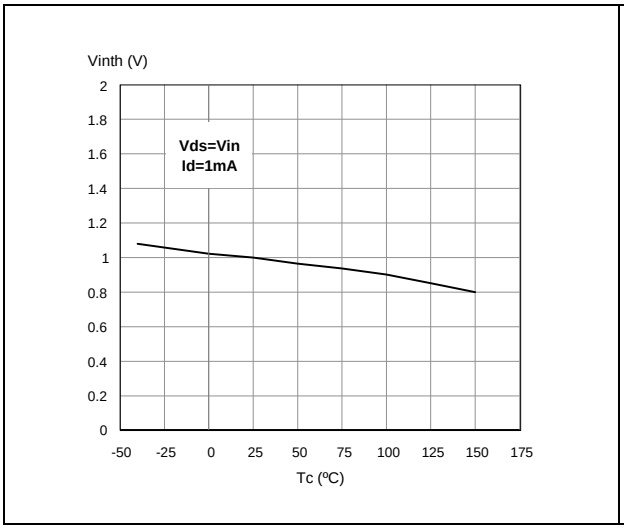


Figure 28. Normalized current limit vs. junction temperature

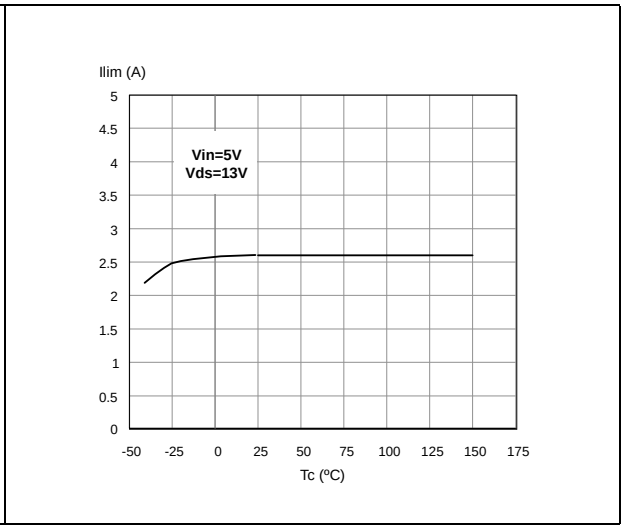
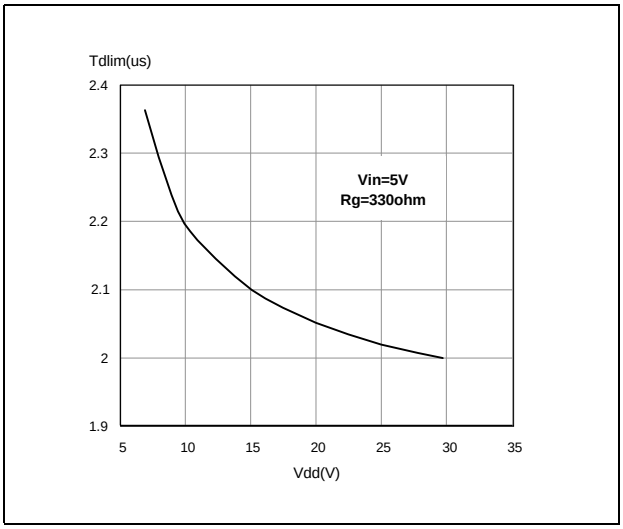


Figure 29. Step response current limit



3 Protection features

During normal operation, the input pin is electrically connected to the gate of the internal Power MOSFET through a low impedance path.

The device behaves like a standard Power MOSFET and it can be used as a switch from DC up to 50 KHz. The only difference from the user's point of view is that a small DC current I_{ISS} (typ. 100 µA) flows into the input pin in order to supply the internal circuitry.

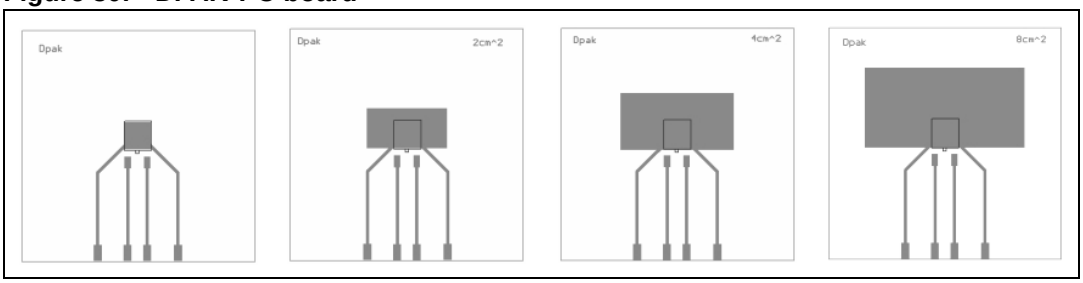
The device integrates:

- Overvoltage clamp protection gives
  - Internally set at 45 V, along with the rugged avalanche characteristics of the Power MOSFET stage give this device unrivalled ruggedness and energy handling capability. This feature is mainly important when driving inductive loads.
- Linear current limiter circuit
  - Limits the drain current I_D to I_{lim} whatever the input pin voltages. When the current limiter is active, the device operates in the linear region, so power dissipation may exceed the capability of the heatsink. Both case and junction temperatures increase, and if this phase lasts long enough, junction temperature may reach the overtemperature threshold T_{jsh}.
- Overtemperature and short circuit protection
  - These are based on sensing the chip temperature and are not dependent on the input voltage. The location of the sensing element on the chip in the power stage area ensures fast, accurate detection of the junction temperature. Overtemperature cutout ranges is from 150 to 190 °C, a typical value is 170 °C. The device is automatically restarted when the chip temperature falls of about 15 °C below shutdown temperature.
- Status feedback
  - In the case of an overtemperature fault condition ($T_j > T_{jsh}$), the device tries to sink a diagnostic current I_{gf} through the input pin in order to indicate fault condition. If driven from a low impedance source, this current may be used in order to warn the control circuit of a device shutdown. If the drive impedance is high enough so that the input pin driver is not able to supply the current I_{gf}, the input pin falls to 0 V. This does not however affect the device operation: no requirement is put on the current capability of the input pin driver except to be able to supply the normal operation drive current I_{ISS}. Additional features of this device are ESD protection according to the Human Body model and the ability to be driven from a TTL logic circuit.

4 Package and PCB thermal data

4.1 DPAK thermal data

Figure 30. DPAK PC board



1. Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 58 mm x 58 mm,PCB thickness = 2 mm, Cu thickness=35 µm , Copper areas: from minimum pad layout to 16 cm^2).

Figure 31. DPAK $R_{thj\text{-}amb}$ vs. PCB copper area in open box free air condition

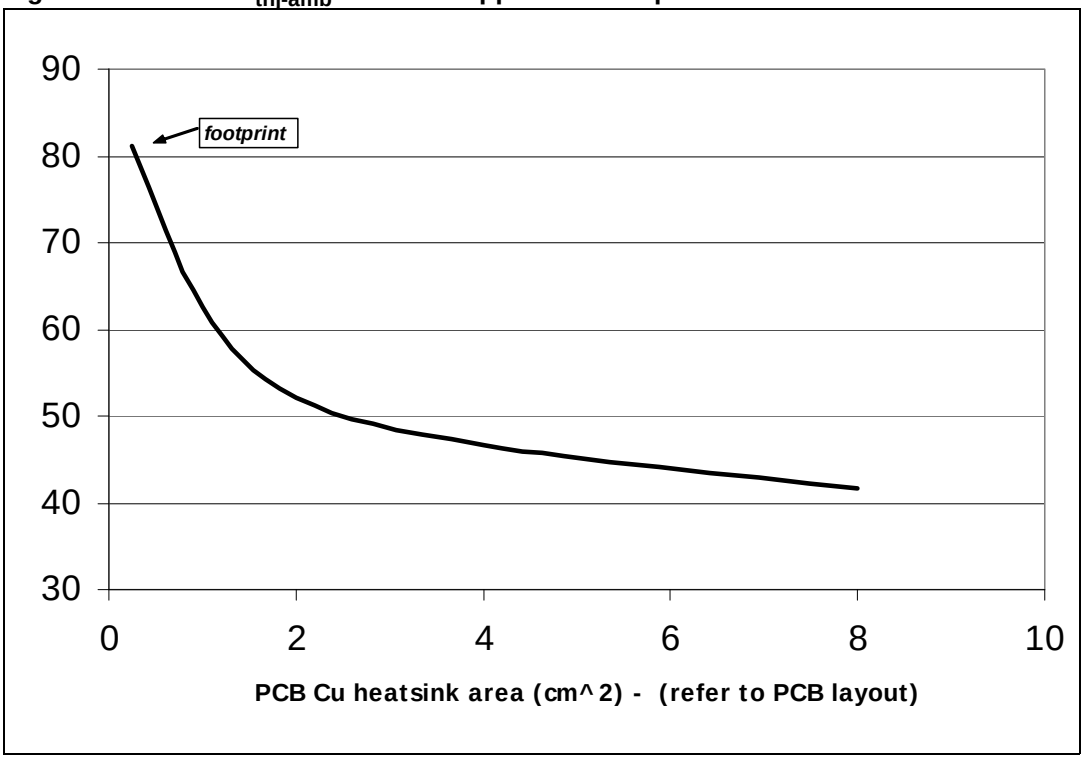
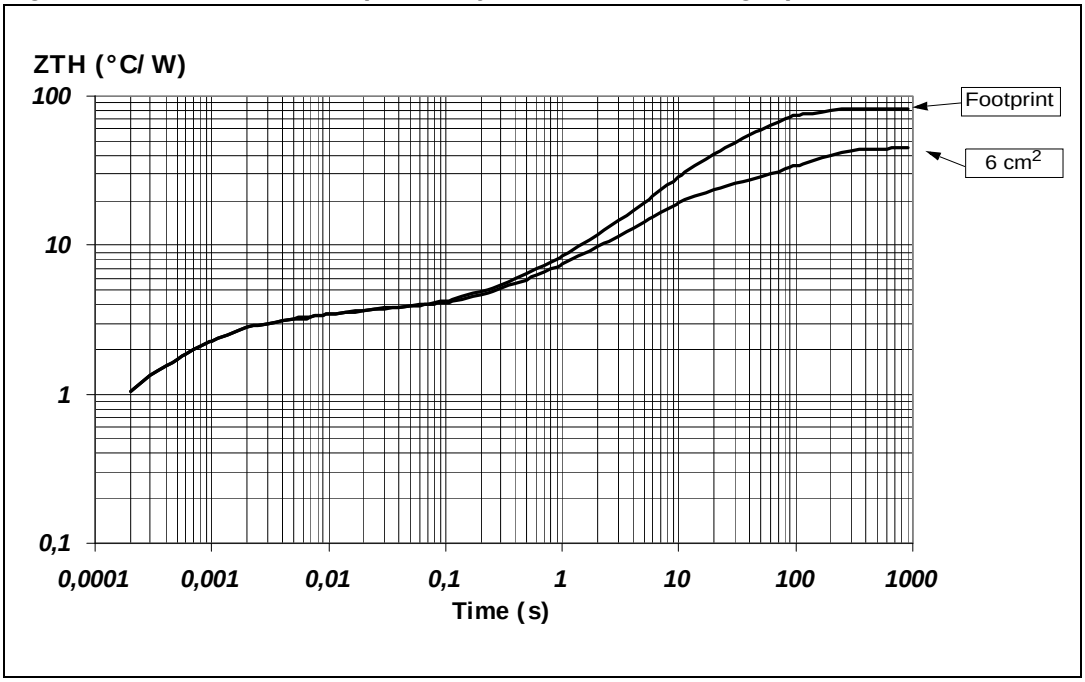


Figure 32. DPAK thermal impedance junction ambient single pulse



Equation 1: Pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1-\delta)$$

where $\delta = t_P/T$

Figure 33. DPAK thermal fitting model of a single channel

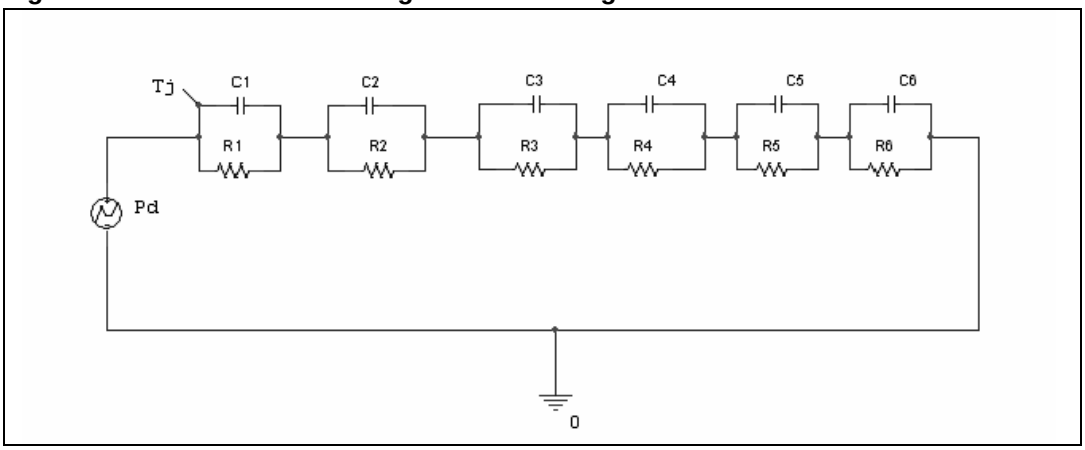


Table 5. DPAK thermal parameter

Area/island (cm^2)	0.25	6
R1 (°C/W)	0.8	
R2 (°C/W)	1.6	
R3 (°C/W)	0.8	
R4 (°C/W)	2	
R5 (°C/W)	15	
R6 (°C/W)	61	24
C1 (W·s/°C)	0.00006	
C2 (W·s/°C)	0.0005	
C3 (W·s/°C)	0.01	
C4 (W·s/°C)	0.3	
C5 (W·s/°C)	0.45	
C6 (W·s/°C)	0.8	5

4.2 SOT-223 thermal data

Figure 34. SOT-223 PC board

1. Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 58 mm x 58 mm,PCB thickness = 2 mm, Cu thickness=35 µm , Copper areas: from minimum pad layout to 0.8 cm^2).

Figure 35. SOT-223 $R_{thj-amb}$ vs. PCB copper area in open box free air condition

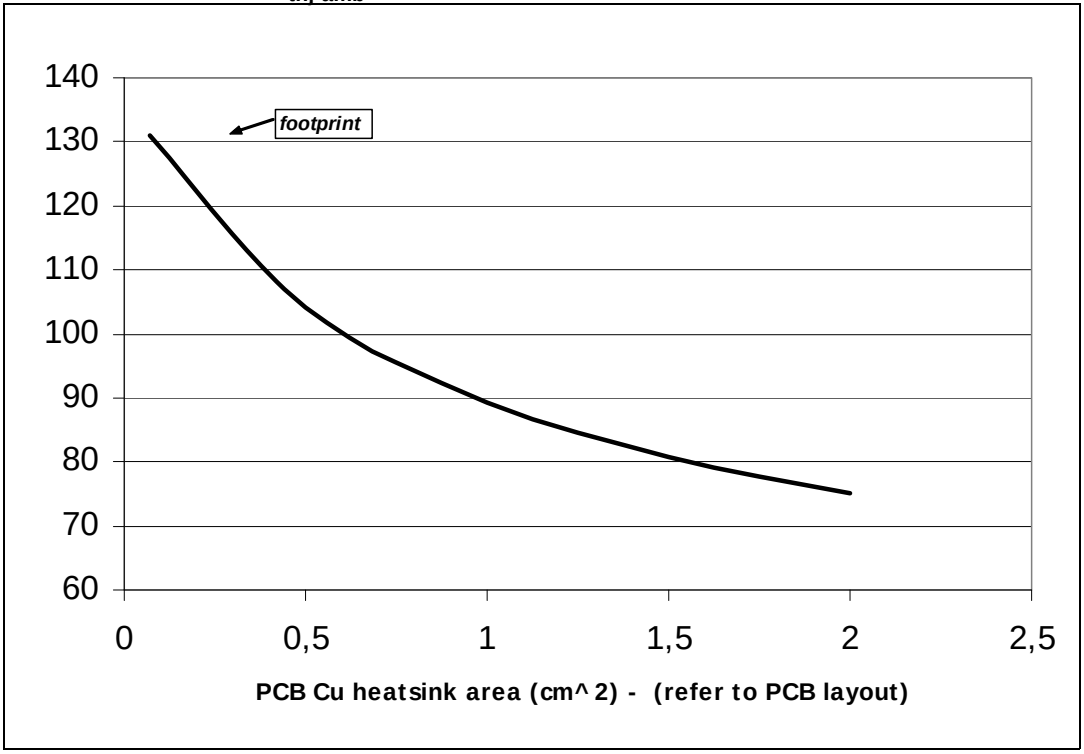
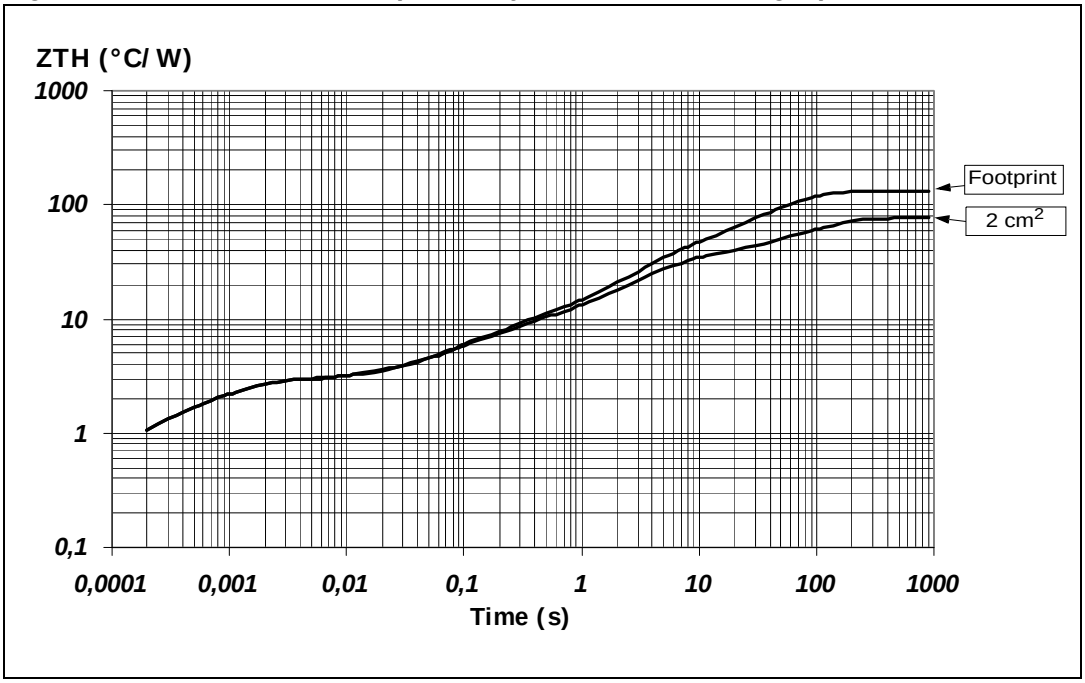


Figure 36. SOT-223 thermal impedance junction ambient single pulse



Equation 2: Pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_P/T$

Figure 37. SOT-223 thermal fitting model of a single channel

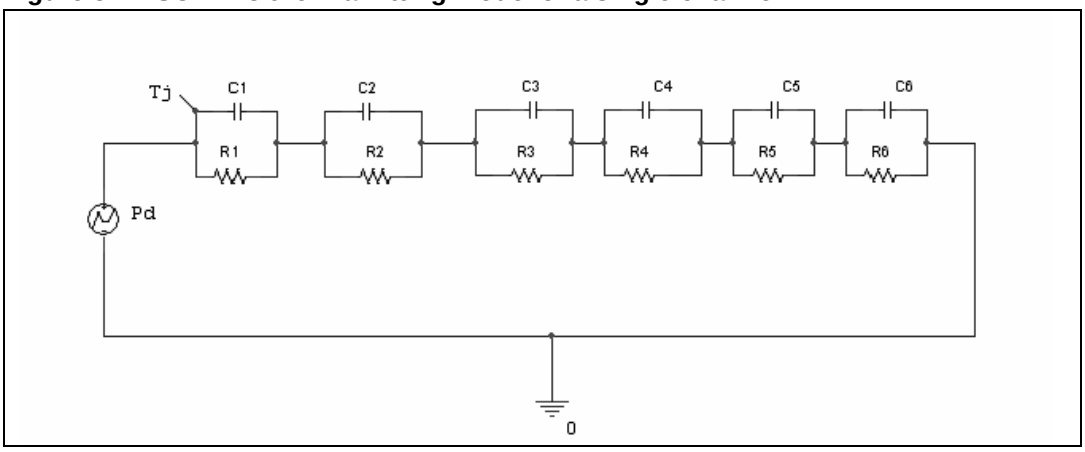
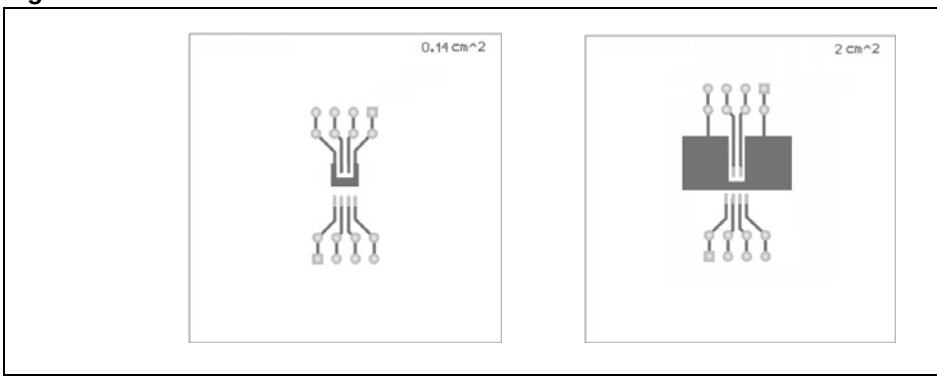


Table 6. SOT-223 thermal parameter

Area/island (cm^2)	FP	2
R1 (°C/W)	0.8	
R2 (°C/W)	1.6	
R3 (°C/W)	4.5	
R4 (°C/W)	24	
R5 (°C/W)	0.1	
R6 (°C/W)	100	45
C1 (W·s/°C)	0.00006	
C2 (W·s/°C)	0.0005	
C3 (W·s/°C)	0.03	
C4 (W·s/°C)	0.16	
C5 (W·s/°C)	1000	
C6 (W·s/°C)	0.5	2

4.3 SO-8 thermal data

Figure 38. SO-8 PC board



1. Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 58 mm x 58 mm,PCB thickness = 2 mm, Cu thickness=35 µm , Copper areas: from minimum pad layout to 2 cm^2).

Figure 39. SO-8 $R_{thj\text{-}amb}$ vs. PCB copper area in open box free air condition

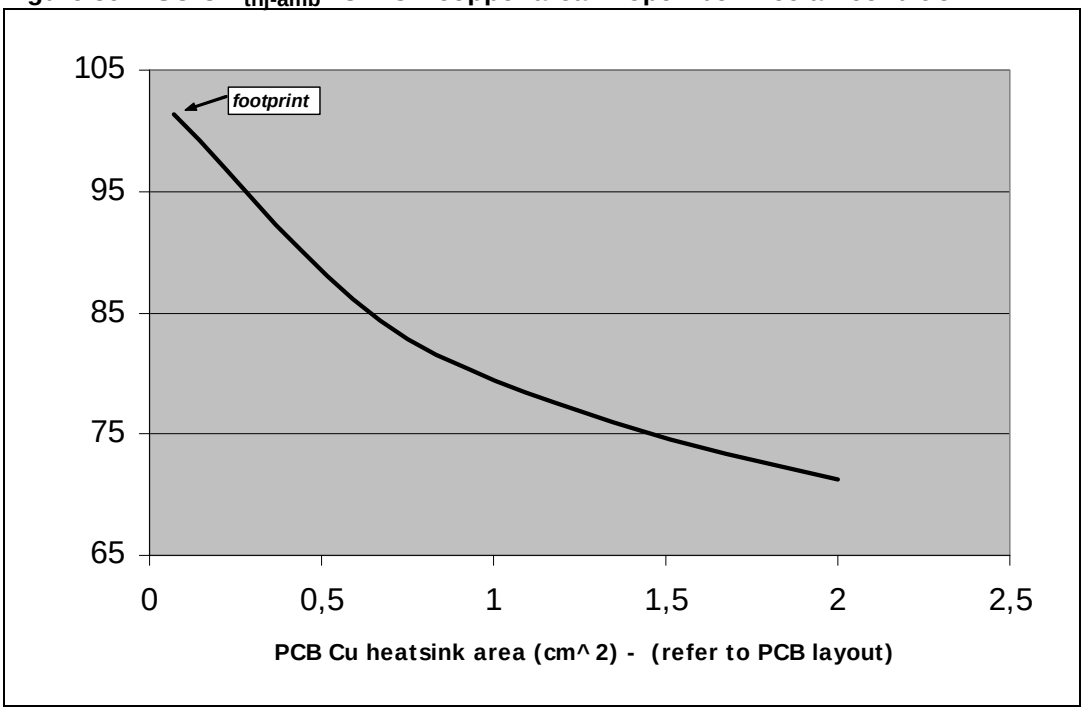
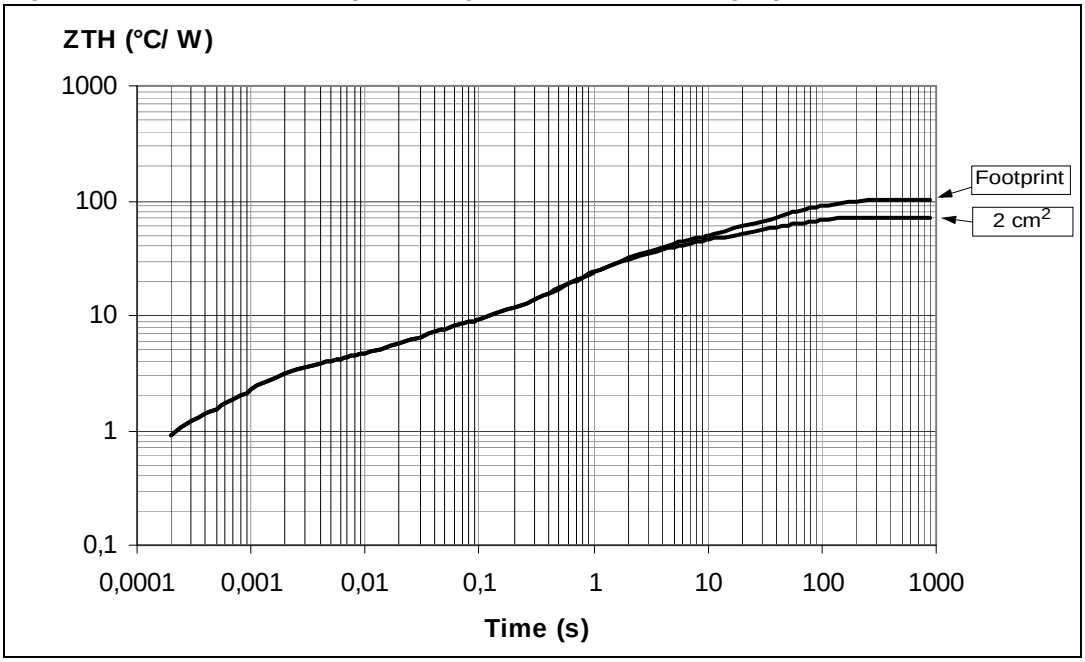


Figure 40. SO-8 thermal impedance junction ambient single pulse



Equation 3: Pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_P/T$

Figure 41. SO-8 thermal fitting model of a single channel

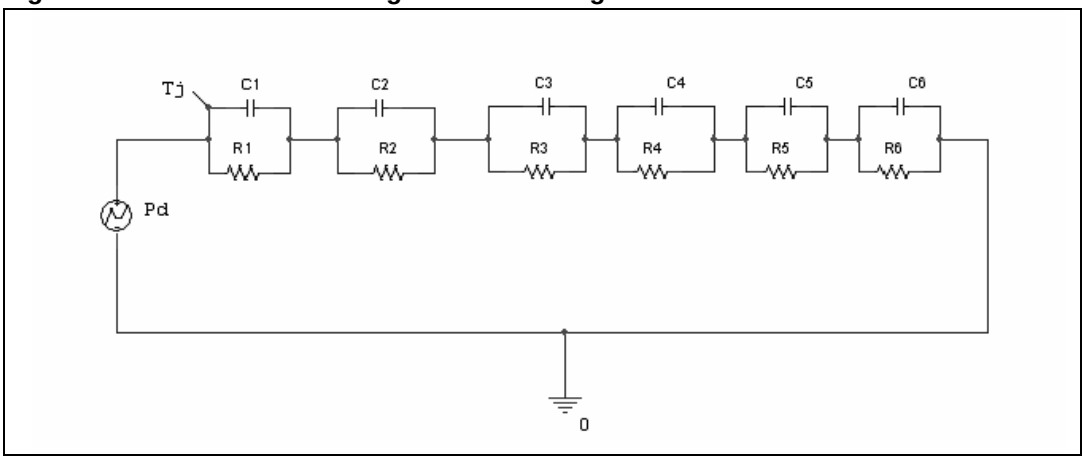


Table 7. SO-8 thermal parameter

Area/island (cm^2)	FP	2
R1 (°C/W)	0.8	
R2 (°C/W)	2.6	
R3 (°C/W)	3.5	
R4 (°C/W)	21	
R5 (°C/W)	16	
R6 (°C/W)	58	28
C1 (W·s/°C)	0.00006	
C2 (W·s/°C)	0.0005	
C3 (W·s/°C)	0.0075	
C4 (W·s/°C)	0.045	
C5 (W·s/°C)	0.35	
C6 (W·s/°C)	1.05	2

5 Package and packing information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

5.1 DPAK mechanical data

Figure 42. DPAK package dimensions

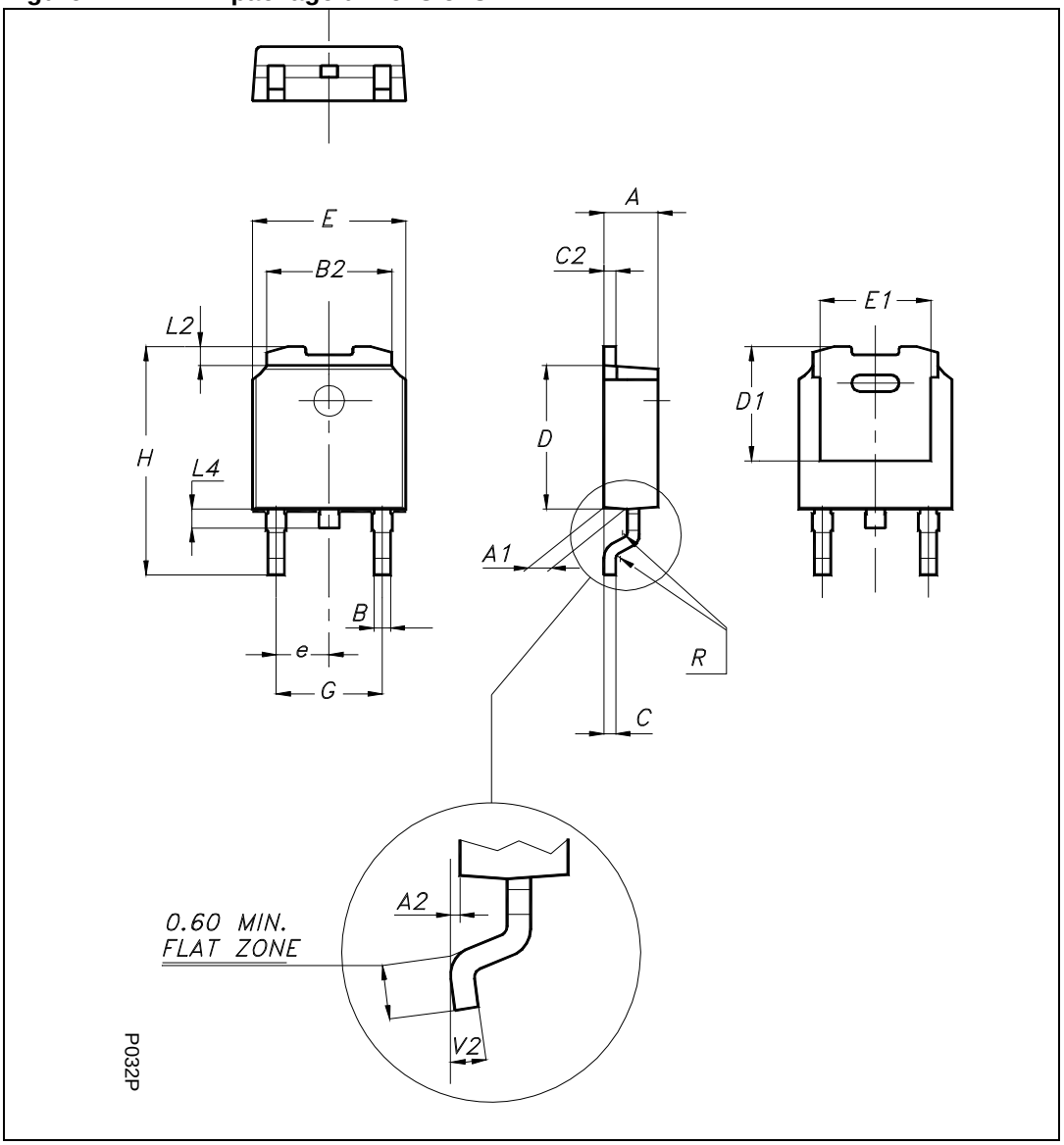
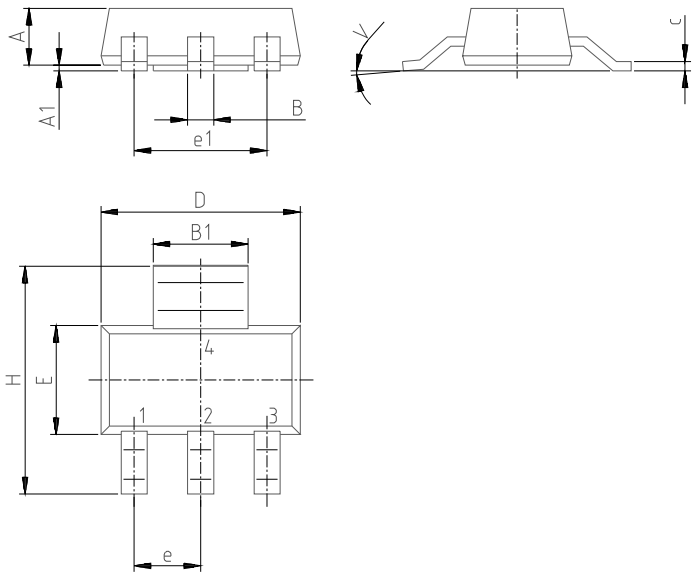


Table 8. DPAK mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
B	0.64		0.90
B2	5.20		5.40
C	0.45		0.60
C2	0.48		0.60
D	6.00		6.20
D1		5.1	
E	6.40		6.60
E1		4.7	
e		2.28	
G	4.40		4.60
H	9.35		10.10
L2		0.8	
L4	0.60		1.00
R		0.2	
V2	0°	8°	
Package weight	Gr. 0.29		

5.2 SOT-223 mechanical data

Figure 43. SOT-223 mechanical data & package outline



Dim.	mm.			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.8			0.071
B	0.6	0.7	0.85	0.024	0.027	0.033
B1	2.9	3	3.15	0.114	0.118	0.124
c	0.24	0.26	0.35	0.009	0.01	0.014
D	6.3	6.5	6.7	0.248	0.256	0.264
e		2.3			0.09	
e1		4.6			0.181	
E	3.3	3.5	3.7	0.13	0.138	0.146
H	6.7	7	7.3	0.264	0.276	0.287
V	10° (max)					
A1	0.02		0.1	0.0008		0.004

5.3 SO8 mechanical data

Table 9. SO-8 mechanical data

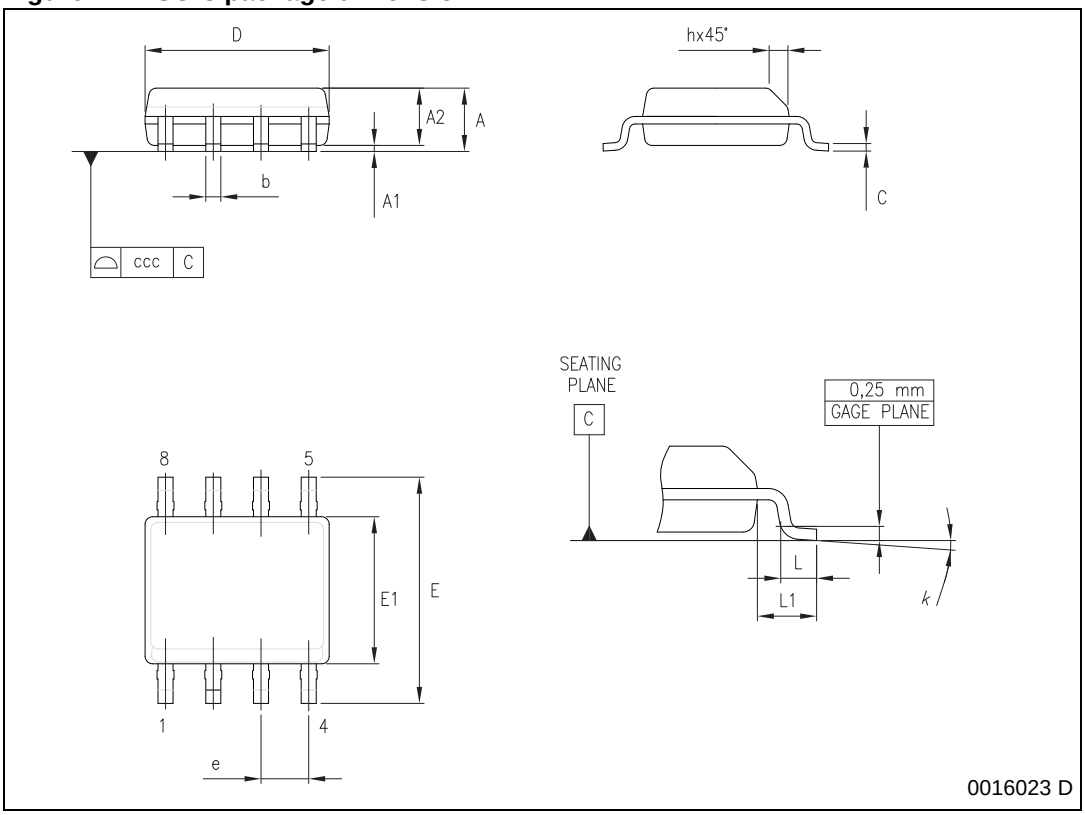
Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		

Table 9. SO-8 mechanical data (continued)

Dim.	mm		
	Min.	Typ.	Max.
b	0.28		0.48
c	0.17		0.23
D(1)	4.80	4.90	5.00
E	5.80	6.00	6.20
E1(2)	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
k	0°		8°
ccc			0.10

1. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm in total (both side).
2. Dimension “E1” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm per side.

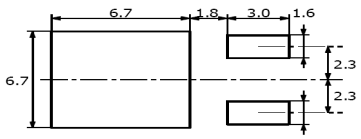
Figure 44. SO-8 package dimension



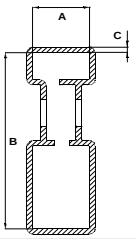
5.4 DPAK packing information

The devices can be packed in tube or tape and reel shipments (see the *Table 1: Device summary*).

DPAK FOOTPRINT



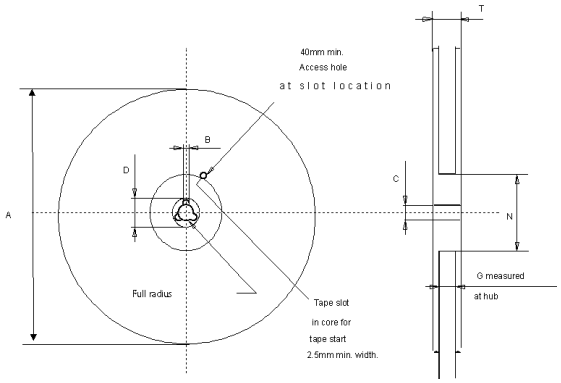
TUBE SHIPMENT (no suffix)



Base Q.ty	75
Bulk Q.ty	3000
Tube length (± 0.5)	532
A	6
B	21.3
C (± 0.1)	0.6

All dimensions are in mm.

TAPE AND REEL SHIPMENT (suffix “13TR”)



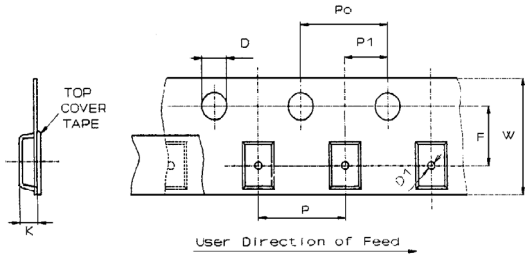
REEL DIMENSIONS

Base Q.ty	2500
Bulk Q.ty	2500
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	16.4
N (min)	60
T (max)	22.4

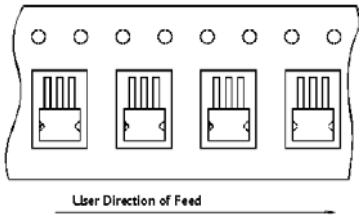
TAPE DIMENSIONS

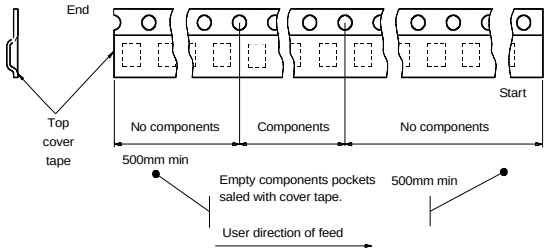
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

Tape width	**W**	16
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	8
Hole Diameter	**D (± 0.1/-0)**	1.5
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.05)**	7.5
Compartment Depth	**K (max)**	6.5
Hole Spacing	**P1 (± 0.1)**	2



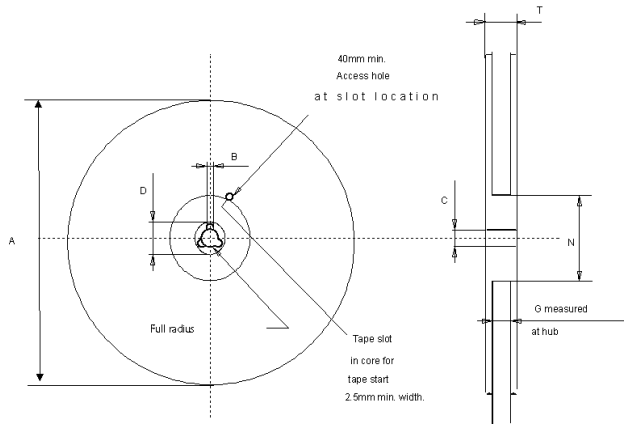
All dimensions are in mm.





5.5 SOT-223 packing information

Figure 45. SOT-223 tape and reel shipment (suffix “TR”)



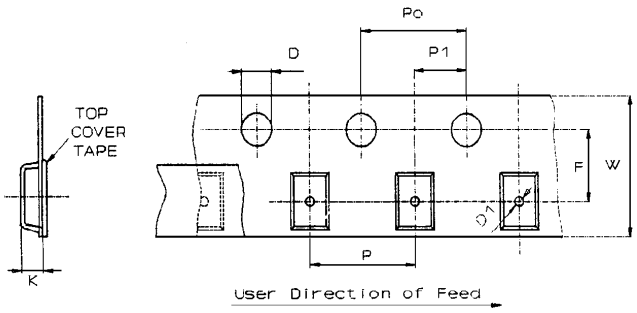
Reel dimensions

Base Q.ty	1000
Bulk Q.ty	1000
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	12.4
N (min)	60
T (max)	18.4

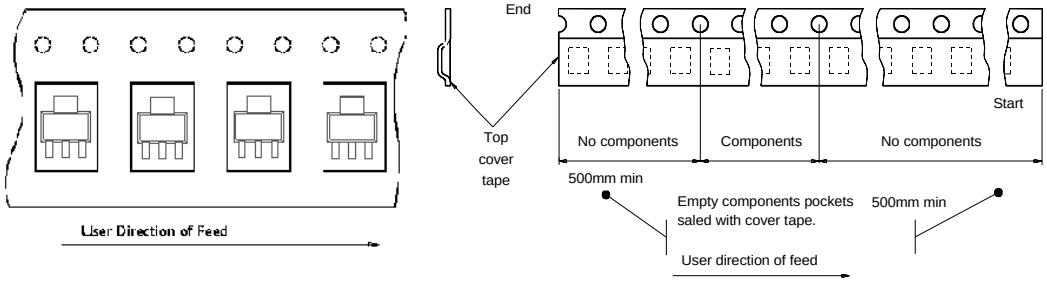
Tape dimensions

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	**W**	12
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	8
Hole Diameter	**D (+ 0.1/-0)**	1.5
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.05)**	5.5
Compartment Depth	**K (max)**	4.5
Hole Spacing	**P1 (± 0.1)**	2

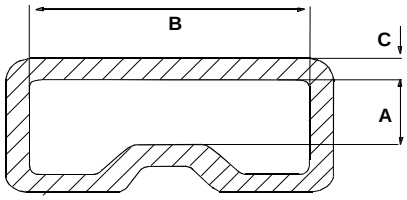


All dimensions are in mm.



5.6 SO8 packing information

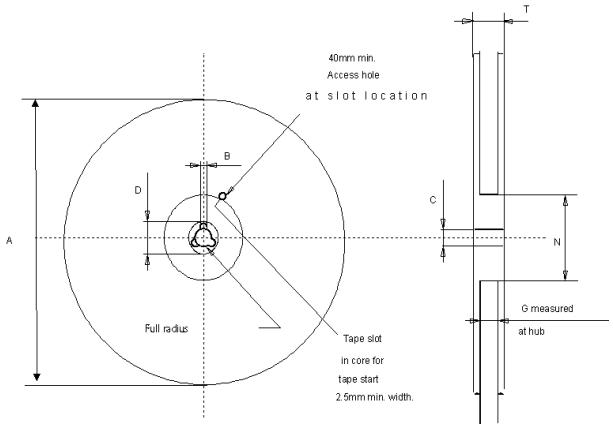
Figure 46. SO-8 tube shipment (no suffix)



Base Q.ty	100
Bulk Q.ty	2000
Tube length (± 0.5)	532
A	3.2
B	6
C (± 0.1)	0.6

All dimensions are in mm.

Figure 47. SO-8 tape and reel shipment (suffix "TR")



REEL DIMENSIONS

Base Q.ty	2500
Bulk Q.ty	2500
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	12.4
N (min)	60
T (max)	18.4

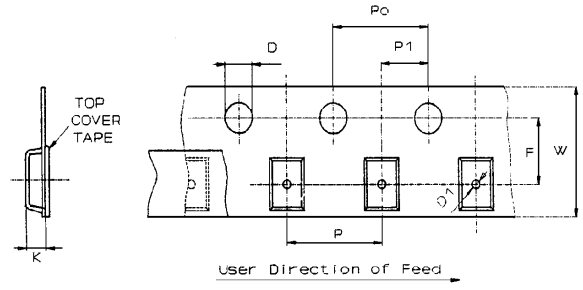
All dimensions are in mm.

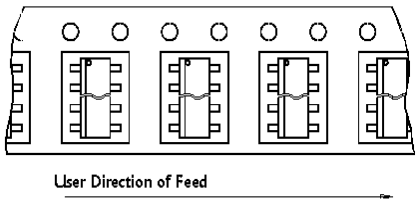
TAPE DIMENSIONS

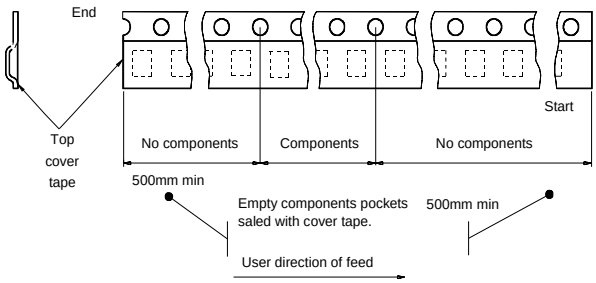
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	**W**	12
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	8
Hole Diameter	**D (+ 0.1/-0)**	1.5
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.05)**	5.5
Compartment Depth	**K (max)**	4.5
Hole Spacing	**P1 (± 0.1)**	2

All dimensions are in mm.







6 Revision history

Table 10. Document revision history

Date	Revision	Changes
Feb-2003	1	Initial release.
16-Apr-2009	2	Added *Table 1: Device summary* and *Section 4: Package and PCB thermal data* Updated *Section 5: Package and packing information on page 25*
01-Dic-2011	3	Upadate *Table 1: Device summary*. Update the entire document using the new coorporate template.
20-Sep-2013	4	Updated Disclaimer.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

ST PRODUCTS ARE NOT DESIGNED OR AUTHORIZED FOR USE IN: (A) SAFETY CRITICAL APPLICATIONS SUCH AS LIFE SUPPORTING, ACTIVE IMPLANTED DEVICES OR SYSTEMS WITH PRODUCT FUNCTIONAL SAFETY REQUIREMENTS; (B) AERONAUTIC APPLICATIONS; (C) AUTOMOTIVE APPLICATIONS OR ENVIRONMENTS, AND/OR (D) AEROSPACE APPLICATIONS OR ENVIRONMENTS. WHERE ST PRODUCTS ARE NOT DESIGNED FOR SUCH USE, THE PURCHASER SHALL USE PRODUCTS AT PURCHASER’S SOLE RISK, EVEN IF ST HAS BEEN INFORMED IN WRITING OF SUCH USAGE, UNLESS A PRODUCT IS EXPRESSLY DESIGNATED BY ST AS BEING INTENDED FOR “AUTOMOTIVE, AUTOMOTIVE SAFETY OR MEDICAL” INDUSTRY DOMAINS ACCORDING TO ST PRODUCT DESIGN SPECIFICATIONS. PRODUCTS FORMALLY ESCC, QML OR JAN QUALIFIED ARE DEEMED SUITABLE FOR USE IN AEROSPACE BY THE CORRESPONDING GOVERNMENTAL AGENCY.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.
Information in this document supersedes and replaces all information previously supplied.
The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com