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ON Semiconductor MC74HC74ADTR2

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MC74HC74A

Dual D Flip-Flop with Set and Reset

High-Performance Silicon-Gate CMOS

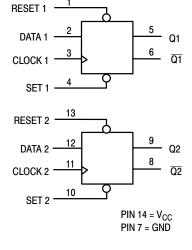
The MC74HC74A is identical in pinout to the LS74. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of two D flip–flops with individual Set, Reset, and Clock inputs. Information at a D–input is transferred to the corresponding Q output on the next positive going edge of the clock input. Both Q and \overline{Q} outputs are available from each flip–flop. The Set and Reset inputs are asynchronous.

Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the JEDEC Standard No. 7.0 A Requirements
- Chip Complexity: 128 FETs or 32 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

LOGIC DIAGRAM





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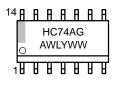


SOIC-14 NB D SUFFIX CASE 751A TSSOP-14 DT SUFFIX CASE 948G

PIN ASSIGNMENT

RESET 1	[1 ●	14	l v _{cc}
DATA 1	2	13	RESET 2
CLOCK 1	3	12	DATA 2
SET 1	4	11	CLOCK 2
Q1	5	10	SET 2
Q1	6	9] Q2
GND	7	8] <u>Q2</u>

MARKING DIAGRAMS



SOIC-14 NB



TSSOP-14

 $\begin{array}{lll} A & = Assembly \ Location \\ L, \ WL & = Wafer \ Lot \\ Y, \ YY & = Year \\ W, \ WW & = Work \ Week \end{array}$

G or ■ = Pb–Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

Datasheet of MC74HC74ADTR2 - IC D-TYPE POS TRG DUAL 14TSSOP

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FUNCTION TABLE

	Inputs				puts
Set	Set Reset Clock Data				Q
L	Н	Х	Χ	Н	L
Н	L	X	Χ	L	Н
L	L	Χ	X	H*	H*
Н	Н		Н	Н	L
Н	Н	\mathcal{L}	L	L	Н
Н	Н	L	X	No Cl	nange
Н	Н	Н	Χ		nange
Н	Н	~	Χ	No Cl	nange

^{*}Both outputs will remain high as long as Set and Reset are low, but the output states are unpredictable if Set and Reset go high simultaneously.

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to + 7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
V _{out}	DC Output Voltage (Referenced to GND)	-0.5 to V_{CC} + 0.5	V
l _{in}	DC Input Current, per Pin	±20	mA
l _{out}	DC Output Current, per Pin	±25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±50	mA
P _D	Power Dissipation in Still Air, SOIC Package† TSSOP Package†	500 450	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds		°C
	(SOIC or TSSOP Package)	260	
		300	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND \leq (V_{in} or V_{out}) \leq V_{CC} .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

†Derating: SOIC Package: –7 mW/°C from 65° to 125°C TSSOP Package: –6.1 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V _{CC}	V
T _A	Operating Temperature, All Package Types		- 55	+125	°C
t _r , t _f	Input Rise and Fall Time	V _{CC} = 2.0 V	0	1000	ns
	(Figures 1, 2, 3)	$V_{CC} = 3.0 \text{ V}$	0	600	
		$V_{CC} = 4.5 \text{ V}$	0	500	
		$V_{CC} = 6.0 \text{ V}$	0	400	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

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DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

				Gu	aranteed Li	mit	
Symbol	Parameter	Test Conditions	V _{CC} V	–55 to 25°C	≤ 85°C	≤ 125°C	Unit
V _{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \le 20 \mu\text{A}$	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V _{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $ I_{out} \le 20 \mu A$	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
V _{OH}	Minimum High-Level Output Voltage	$\begin{split} &V_{in} = V_{IH} \text{ or } V_{IL} \\ & I_{out} \leq 20 \ \mu\text{A} \end{split}$ $&V_{in} = V_{IH} \text{ or } V_{IL} I_{out} \leq 2.4 \ \text{mA} \\ & I_{out} \leq 4.0 \ \text{mA} \\ & I_{out} \leq 5.2 \ \text{mA} \end{split}$	2.0 4.5 6.0 3.0 4.5 6.0	1.9 4.4 5.9 2.48 3.98 5.48	1.9 4.4 5.9 2.34 3.84 5.34	1.9 4.4 5.9 2.2 3.7 5.2	V
V _{OL}	Maximum Low–Level Output Voltage	$\begin{split} &V_{in} = V_{IH} \text{ or } V_{IL} \\ & I_{out} \leq 20 \ \mu\text{A} \end{split}$ $&V_{in} = V_{IH} \text{ or } V_{IL} \begin{aligned} & I_{out} \leq 2.4 \text{ mA} \\ & I_{out} \leq 4.0 \text{ mA} \\ & I_{out} \leq 5.2 \text{ mA} \end{aligned}$	2.0 4.5 6.0 3.0 4.5 6.0	0.1 0.1 0.1 0.26 0.26 0.26	0.1 0.1 0.1 0.33 0.33 0.33	0.1 0.1 0.1 0.4 0.4 0.4	V
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	6.0	±0.1	±1.0	±1.0	μА
I _{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu A$	6.0	2.0	20	80	μΑ

AC ELECTRICAL CHARACTERISTICS ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6.0 \text{ ns}$)

			Guaranteed Limit			
Symbol	Parameter	v _{cc}	– 55 to 25°C	≤ 85°C	≤ 125°C	Unit
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0 3.0 4.5 6.0	6.0 15 30 35	4.8 10 24 28	4.0 8.0 20 24	MHz
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock to Q or Q (Figures 1 and 4)	2.0 3.0 4.5 6.0	100 75 20 17	125 90 25 21	150 120 30 26	ns
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Set or Reset to Q or Q (Figures 2 and 4)	2.0 3.0 4.5 6.0	105 80 21 18	130 95 26 22	160 130 32 27	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0 3.0 4.5 6.0	75 30 15 13	95 40 19 16	110 55 22 19	ns
C _{in}	Maximum Input Capacitance	_	10	10	10	pF

		Typical @ 25°C, V _{CC} = 5.0 V	
C_PD	Power Dissipation Capacitance (Per Flip-Flop)*	32	pF

^{*} Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

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TIMING REQUIREMENTS (Input $t_r = t_f = 6.0 \text{ ns}$)

			Gu	aranteed Li	mit	İ
Symbol	Parameter	V _{CC} V	–55 to 25°C	≤ 85°C	≤ 125°C	Unit
t _{su}	Minimum Setup Time, Data to Clock (Figure 3)	2.0 3.0 4.5 6.0	80 35 16 14	100 45 20 17	120 55 24 20	ns
t _h	Minimum Hold Time, Clock to Data (Figure 3)	2.0 3.0 4.5 6.0	3.0 3.0 3.0 3.0	3.0 3.0 3.0 3.0	3.0 3.0 3.0 3.0	ns
t _{rec}	Minimum Recovery Time, Set or Reset Inactive to Clock (Figure 2)	2.0 3.0 4.5 6.0	8.0 8.0 8.0 8.0	8.0 8.0 8.0 8.0	8.0 8.0 8.0 8.0	ns
t _w	Minimum Pulse Width, Clock (Figure 1)	2.0 3.0 4.5 6.0	60 25 12 10	75 30 15 13	90 40 18 15	ns
t _w	Minimum Pulse Width, Set or Reset (Figure 2)	2.0 3.0 4.5 6.0	60 25 12 10	75 30 15 13	90 40 18 15	ns
t _r , t _f	Maximum Input Rise and Fall Times (Figures 1, 2, 3)	2.0 3.0 4.5 6.0	1000 800 500 400	1000 800 500 400	1000 800 500 400	ns

ORDERING INFORMATION

Device	Package	Shipping [†]
MC74HC74ADG	SOIC-14 NB (Pb-Free)	55 Units / Rail
NLV74HC74ADG*	SOIC-14 NB (Pb-Free)	55 Units / Rail
MC74HC74ADR2G	SOIC-14 NB (Pb-Free)	2500 / Tape & Reel
NLV74HC74ADR2G*	SOIC-14 NB (Pb-Free)	2500 / Tape & Reel
MC74HC74ADTR2G	TSSOP-14 (Pb-Free)	2500 / Tape & Reel
NLV74HC74ADTR2G*	TSSOP-14 (Pb-Free)	2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP

Capable.

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SWITCHING WAVEFORMS

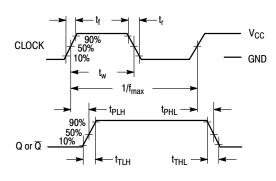


Figure 1.

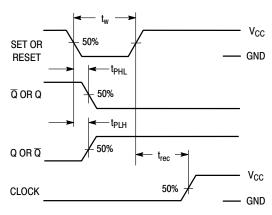


Figure 2.

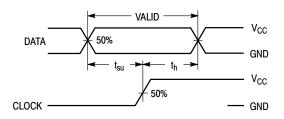
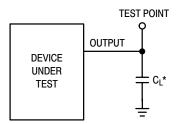


Figure 3.



*Includes all probe and jig capacitance

Figure 4.

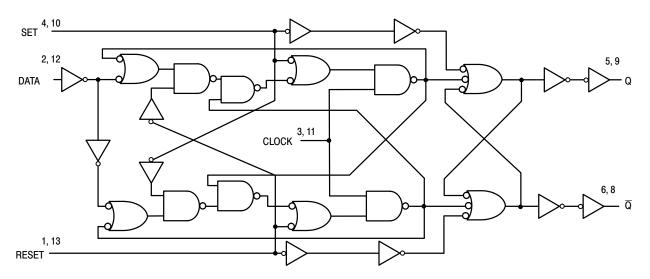


Figure 5. EXPANDED LOGIC DIAGRAM

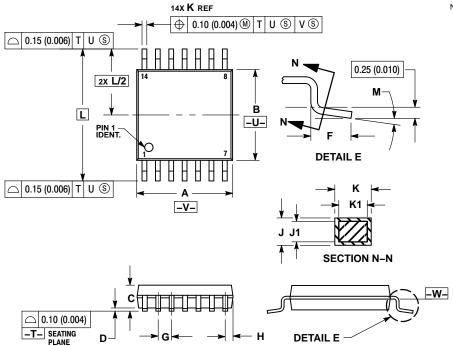
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PACKAGE DIMENSIONS

TSSOP-14 CASE 948G **ISSUE B**



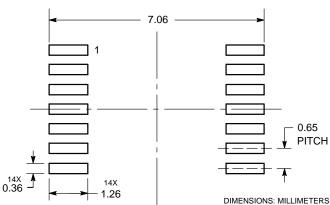
- NOTES:

 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.06) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION ALLOWABLE

 - DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K (U.U.O.) TO THE IN EACESS OF THE K
 DIMENSION AT MAXIMUM MATERIAL
 CONDITION.
 6. TERMINAL NUMBERS ARE SHOWN FOR
 REFERENCE ONLY.
 7. DIMENSION A AND B ARE TO BE
 DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INC	HES
DIM	MIN	MAX	MIN	MAX
Α	4.90	5.10	0.193	0.200
В	4.30	4.50	0.169	0.177
С		1.20		0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65	BSC	0.026	BSC
Н	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40	BSC	0.252 BSC	
M	0 °	8°	0 °	8 °

SOLDERING FOOTPRINT





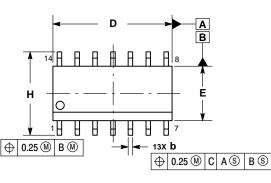
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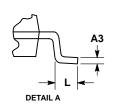
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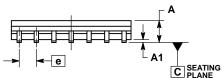
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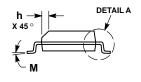
PACKAGE DIMENSIONS











NOTES:

- IOTES:

 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.

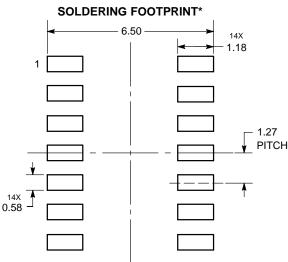
 2. CONTROLLING DIMENSION: MILLIMETERS.

 3. DIMENSION 5 DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.

 4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.

 5. MAXIMILIM MOLD PROTRUSION.0.15 PER
- 5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIN	IETERS	S INCHES	
DIM	MIN	MAX	MIN	MAX
Α	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
q	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
Е	3.80	4.00	0.150	0.157
ø	1.27 BSC		0.050	BSC
Η	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
٦	0.40	1.25	0.016	0.049
М	0 °	7°	0 °	7°



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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