128-Position I²C®-Compatible Digital Potentiometer

AD5247

FEATURES

128 positions
End-to-end resistance: 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ
Ultracompact, SC70-6 (2 mm × 2.1 mm) package
I²C-compatible interface
Full read/write of wiper register
Power-on preset to midscale
Single-supply 2.7 V to 5.5 V
Low temperature coefficient: 45 ppm/°C
Low power, I_{DD} = 3 µA typical
Wide operating temperature range: –40°C to +125°C
Available in Pb–free package
Evaluation board available

APPLICATIONS

Mechanical potentiometer replacement in new designs
Transducer adjustment of pressure, temperature, position, chemical, and optical sensors
RF amplifier-biasing
LCD brightness and contrast adjustment
Automotive electronics adjustment
Gain control and offset adjustment

FUNCTIONAL BLOCK DIAGRAM

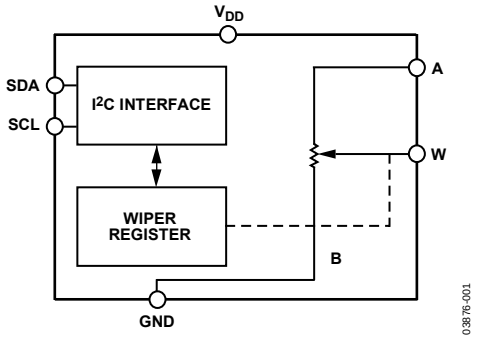

Figure 1.

GENERAL DESCRIPTION

The AD5247 provides a compact, 2 mm × 2.1 mm, packaged solution for 128-position adjustment applications. This device performs the same electronic adjustment function as a mechanical potentiometer or a variable resistor. Available in four different end-to-end resistance values (5 kΩ, 10 kΩ, 50 kΩ, and 100 kΩ), these low temperature coefficient devices are ideal for high accuracy and stability variable resistance adjustments.

The wiper settings are controllable through the I²C-compatible digital interface, which can also be used to read back the present wiper register control word. The 10 kΩ and 100 kΩ options each have three hard-coded slave address options available to allow users access to three of these devices on one I²C bus (see Table 8 for a full list of slave address locations).

The resistance between the wiper and either end point of the fixed resistor varies linearly with respect to the digital code transferred into the RDAC latch. Note the terms digital potentiometer, VR (variable resistor), and RDAC are used interchangeably in this document.

Operating from a 2.7 V to 5.5 V power supply and consuming 3 µA allows the AD5247 to be used in portable battery-operated applications.

Rev. B

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TABLE OF CONTENTS

REVISION HISTORY

3/07—Rev. A to Rev. B

Changes to General Description Section ... 1
Added Table 8 ... 13
Changes to I²C-Compatible 2-Wire Serial Bus Section ... 15
Changes to Ordering Guide ... 18

7/06—Rev. 0 to Rev. A

Updated Format ... Universal
Changes to Absolute Maximum Ratings section ... 6
Changes to Ordering Guide ... 18

9/03—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 kΩ VERSION

V_{DD} = 5 V ± 10% or 3 V ± 10%, $V_A = V_{DD}$, −40°C < T_A < +125°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE						
Resistor Differential Nonlinearity[2]	R-DNL	R_{WB}, V_A = no connect	−1.5	±0.1	+1.5	LSB
Resistor Integral Nonlinearity[2]	R-INL	R_{WB}, V_A = no connect	−4	±0.75	+4	LSB
Nominal Resistor Tolerance[3]	ΔR_{AB}		−30		+30	%
Resistance Temperature Coefficient[3]	$\Delta R_{AB}/\Delta T$			45		ppm/°C
Output Resistance	R_{WB}	Code = 0x00		75	300	Ω
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE						
Differential Nonlinearity[4]	DNL		−1	±0.1	+1	LSB
Integral Nonlinearity[4]	INL		−1	±0.2	+1	LSB
Voltage Divider Temperature Coefficient	$\Delta V_W/\Delta T$	Code = 0x40		15		ppm/°C
Full-Scale Error	V_{WFSE}	Code = 0x7F	−3	−2	0	LSB
Zero-Scale Error	V_{WZSE}	Code = 0x00	0	1	2	LSB
RESISTOR TERMINALS						
Voltage Range[5]	V_A, V_W		GND		V_{DD}	V
Capacitance A[6]	C_A	f = 1 MHz, measured to GND, code = 0x40		45		pF
Capacitance W[6]	C_W	f = 1 MHz, measured to GND, code = 0x40		60		pF
Common-Mode Leakage	I_{CM}	$V_A = V_{DD}/2$		1		nA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	V_{IH}	V_{DD} = 5 V	2.4			V
Input Logic Low	V_{IL}	V_{DD} = 5 V			0.8	V
Input Logic High	V_{IH}	V_{DD} = 3 V	2.1			V
Input Logic Low	V_{IL}	V_{DD} = 3 V			0.6	V
Input Current	I_{IL}	V_{IN} = 0 V or 5 V			±1	μA
Input Capacitance[6]	C_{IL}			5		pF
POWER SUPPLIES						
Power Supply Range	$V_{DD\ RANGE}$		2.7		5.5	V
Supply Current	I_{DD}	V_{IH} = 5 V or V_{IL} = 0 V		3	8	μA
Power Dissipation[7]	P_{DISS}	V_{IH} = 5 V or V_{IL} = 0 V, V_{DD} = 5 V			40	μW
Power Supply Sensitivity	PSSR	V_{DD} = 5 V ± 10%, code = midscale		±0.003	±0.05	%/%
DYNAMIC CHARACTERISTICS[6, 8]						
Bandwidth –3 dB	BW_5 K	R_{AB} = 5 kΩ, code = 0x40		1.2		MHz
Total Harmonic Distortion	THD_W	V_A = 1 V rms, V_B = 0 V, f = 1 kHz		0.05		%
V_W Settling Time	t_S	V_A = 5 V, ±1 LSB error band		1		μs
Resistor Noise Voltage Density	e_{N_WB}	R_{WB} = 2.5 kΩ, R_S = 0 Ω		6		nV/√Hz

[1] Typical specifications represent average readings at 25°C and V_{DD} = 5 V.
[2] Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic.
[3] $V_A = V_{DD}$, wiper (V_W) = no connect.
[4] INL and DNL are measured at V_W, with the RDAC configured as a potentiometer divider similar to a voltage output DAC. $V_A = V_{DD}$ and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic under operating conditions.
[5] Resistor Terminal A and Resistor Terminal W have no limitations on polarity with respect to each other.
[6] Guaranteed by design and not subject to production test.
[7] P_{DISS} is calculated from ($I_{DD} \times V_{DD}$). CMOS logic level inputs result in minimum power dissipation.
[8] All dynamic characteristics use V_{DD} = 5 V.

ELECTRICAL CHARACTERISTICS—10 kΩ, 50 kΩ, AND 100 kΩ VERSIONS

V_{DD} = 5 V ± 10% or 3 V ± 10%, $V_A = V_{DD}$, −40°C < T_A < +125°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE						
Resistor Differential Nonlinearity[2]	R-DNL	R_{WB}, V_A = no connect	−1	±0.1	+1	LSB
Resistor Integral Nonlinearity[2]	R-INL	R_{WB}, V_A = no connect	−2	±0.25	+2	LSB
Nominal Resistor Tolerance[3]	ΔR_{AB}		−20		+20	%
Resistance Temperature Coefficient[3]	$\Delta R_{AB}/\Delta T$			45		ppm/°C
Output Resistance	R_{WB}	Code = 0x00		75	300	Ω
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE						
Differential Nonlinearity[4]	DNL		−1	±0.1	+1	LSB
Integral Nonlinearity[4]	INL		−1	±0.2	+1	LSB
Voltage Divider Temperature Coefficient	$\Delta V_W/\Delta T$	Code = 0x40		15		ppm/°C
Full-Scale Error (50 kΩ, 100 kΩ)	V_{WFSE}	Code = 0x7F	−1	−1	0	LSB
Zero-Scale Error (50 kΩ, 100 kΩ)	V_{WZSE}	Code = 0x00	0	0.4	1	LSB
Full-Scale Error (10 kΩ)	V_{WFSE}	Code = 0x7F	−2	−0.5	0	LSB
Zero-Scale Error (10 kΩ)	V_{WZSE}	Code = 0x00	0	0.5	1	LSB
RESISTOR TERMINALS						
Voltage Range[5]	V_A, V_W		GND		V_{DD}	V
Capacitance A[6]	C_A	f = 1 MHz, measured to GND, code = 0x40		45		pF
Capacitance W[6]	C_W	f = 1 MHz, measured to GND, code = 0x40		60		pF
Common-Mode Leakage	I_{CM}	$V_A = V_{DD}/2$		1		nA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	V_{IH}	V_{DD} = 5 V	2.4			V
Input Logic Low	V_{IL}	V_{DD} = 5 V			0.8	V
Input Logic High	V_{IH}	V_{DD} = 3 V	2.1			V
Input Logic Low	V_{IL}	V_{DD} = 3 V			0.6	V
Input Current	I_{IL}	V_{IN} = 0 V or 5 V			±1	µA
Input Capacitance[6]	C_{IL}			5		pF
POWER SUPPLIES						
Power Supply Range	$V_{DD\ RANGE}$		2.7		5.5	V
Supply Current	I_{DD}	V_{IH} = 5 V or V_{IL} = 0 V		3	8	µA
Power Dissipation[7]	P_{DISS}	V_{IH} = 5 V or V_{IL} = 0 V, V_{DD} = 5 V			40	µW
Power Supply Sensitivity	PSSR	V_{DD} = 5 V ± 10%, code = midscale		±0.01	±0.02	%/%
DYNAMIC CHARACTERISTICS[6, 8]						
Bandwidth –3 dB	BW	R_{AB} = 10 kΩ/50 kΩ/100 kΩ, code = 0x40		600/100/40		kHz
Total Harmonic Distortion	THD_W	V_A =1 V rms, f = 1 kHz, R_{AB} = 10 kΩ		0.05		%
V_W Settling Time (10 kΩ/50 kΩ/100 kΩ)	t_S	V_A = 5 V ±1 LSB error band		2		µs
Resistor Noise Voltage Density	e_{N_WB}	R_{WB} = 5 kΩ, R_S = 0		9		nV/√Hz

[1] Typical specifications represent average readings at 25°C and V_{DD} = 5 V.
[2] Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic.
[3] $V_A = V_{DD}$, wiper (V_W) = no connect.
[4] INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output DAC. $V_A = V_{DD}$ and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.
[5] Resistor Terminal A and Resistor Terminal W have no limitations on polarity with respect to each other.
[6] Guaranteed by design, not subject to production test.
[7] P_{DISS} is calculated from ($I_{DD} \times V_{DD}$). CMOS logic level inputs result in minimum power dissipation.
[8] All dynamic characteristics use V_{DD} = 5 V.

TIMING CHARACTERISTICS—5 kΩ, 10 kΩ, 50 kΩ, AND 100 kΩ VERSIONS

V_{DD} = 5 V ± 10% or 3 V ± 10%, $V_A = V_{DD}$, −40°C < T_A < +125°C, unless otherwise noted.

Table 3.

Parameter[1, 2, 3]	Symbol	Min	Typ[4]	Max	Unit
SCL Clock Frequency	f_{SCL}			400	kHz
Bus Free Time Between Stop and Start, t_{BUF}	t_1	1.3			µs
Hold Time (Repeated Start), $t_{HD;STA}$[5]	t_2	0.6			µs
Low Period of SCL Clock, t_{LOW}	t_3	1.3			µs
High Period of SCL Clock, t_{HIGH}	t_4	0.6		50	µs
Setup Time for Repeated Start Condition, $t_{SU;STA}$	t_5	0.6			µs
Data Hold Time, $t_{HD;DAT}$	t_6			0.9	µs
Data Setup Time, $t_{SU;DAT}$	t_7	100			ns
Fall Time of Both SDA and SCL Signals, t_F	t_8			300	ns
Rise Time of Both SDA and SCL Signals, t_R	t_9			300	ns
Setup Time for Stop Condition, $t_{SU;STO}$	t_{10}	0.6			µs

[1] Specifications apply to all parts.
[2] Guaranteed by design, not subject to production test.
[3] See timing diagrams (Figure 2, Figure 33, and Figure 34) for locations of measured values.
[4] Typical specifications represent average readings at 25°C and V_{DD} = 5 V.
[5] After this period, the first clock pulse is generated.

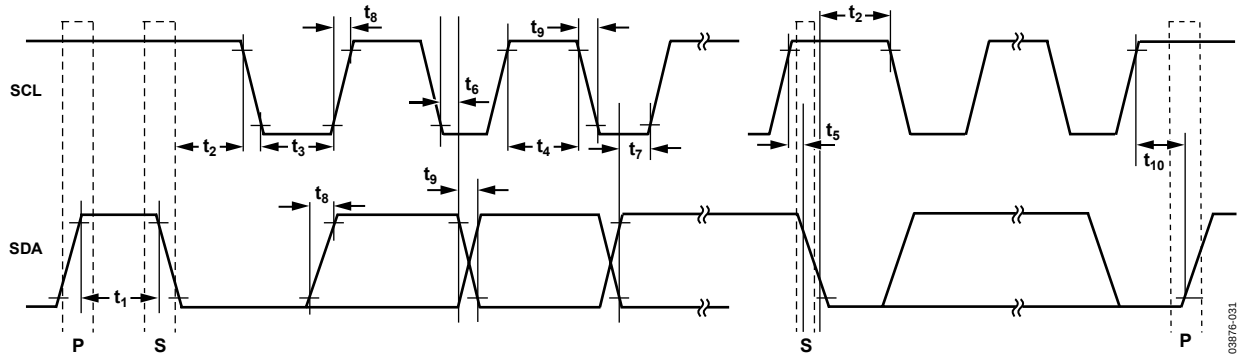

Figure 2. I²C Interface, Detailed Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
V_A, V_W to GND	V_{DD}
Terminal Current, Ax to Bx, Ax to Wx, Bx to Wx	
Pulsed[1]	±20 mA
Continuous	±5 mA
Digital Inputs and Output Voltage to GND	0 V to V_{DD} + 0.3 V
Operating Temperature Range	−40°C to +125°C
Maximum Junction Temperature (T_{JMAX})	150°C
Storage Temperature Range	−65°C to +150°C
Thermal Resistance θ_{JA}[2]: (SC70-6)	340°C/W
Reflow Soldering Peak Temperature	
SnPb	240°C
Pb-Free	260°C

[1] Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.

[2] Package power dissipation = (T_{JMAX} − T_A)/θ_{JA}.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

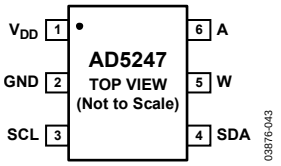

Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD}	Positive Power Supply.
2	GND	Digital Ground and B Termination Voltage.
3	SCL	Serial Clock Input; Positive Edge Triggered.
4	SDA	Serial Data Input/Output.
5	W	Terminal W.
6	A	Terminal A.

TYPICAL PERFORMANCE CHARACTERISTICS

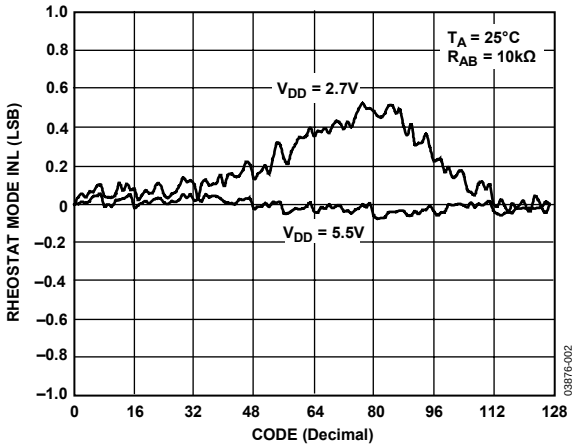

Figure 4. R-INL vs. Code vs. Supply Voltages

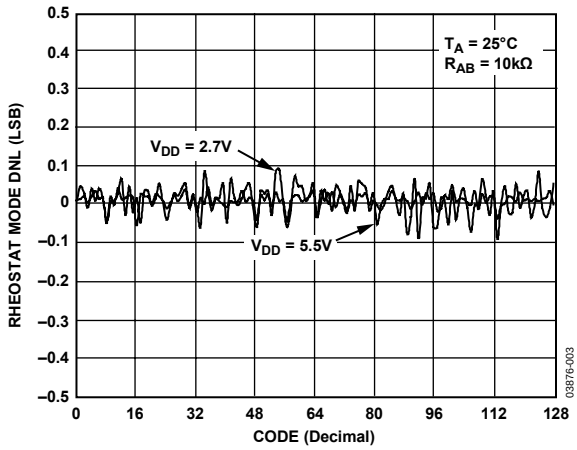

Figure 5. R-DNL vs. Code vs. Supply Voltages

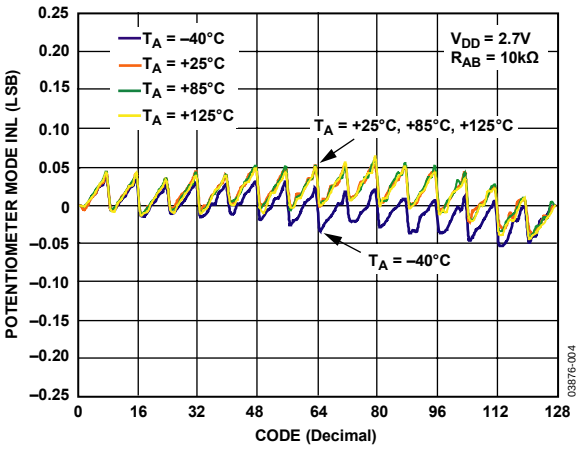

Figure 6. INL vs. Code vs. Temperature

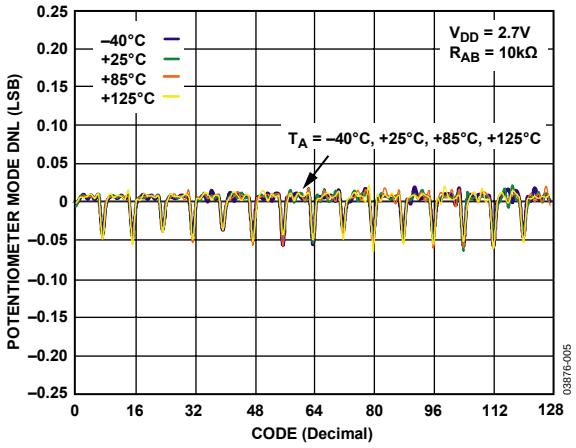

Figure 7. DNL vs. Code vs. Temperature

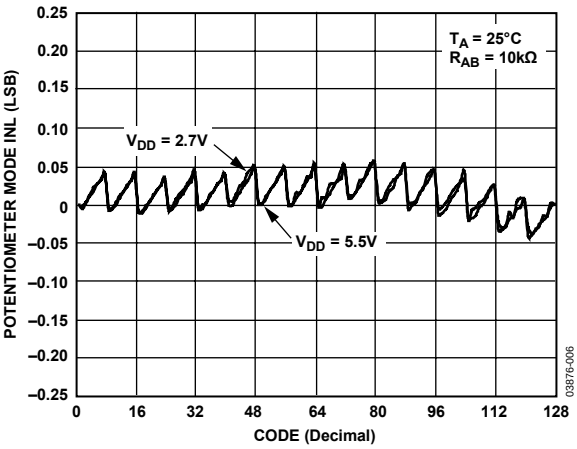

Figure 8. INL vs. Code vs. Supply Voltages

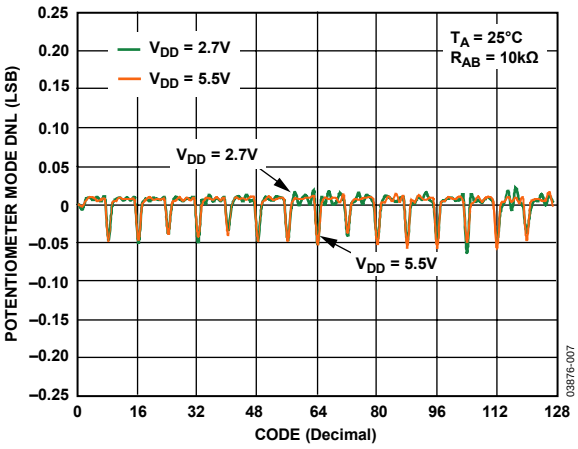

Figure 9. DNL vs. Code vs. Supply Voltages