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DAC8800FP

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ANALOG DEVICES

Octal 8-Bit CMOS D/A Converter

DAC8800

FEATURES

- ±1/2 LSB Total Unadjusted Error
- 2μs Settling Time
- Serial Data Input
- ±Full-Scale Output Set by $V_{REF}H$ and $V_{REF}L$
- Unipolar and Bipolar Operation
- TTL Input Compatible
- 20-Pin DIP or SOL Package
- Low Cost

APPLICATIONS

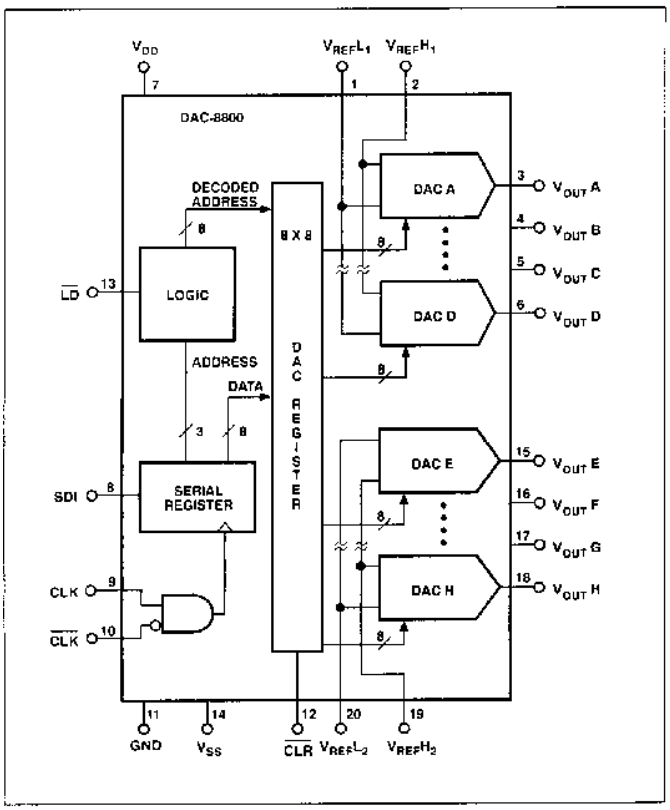
- Voltage Set Point Control
- Digital Offset & Gain Adjustment
- Microprocessor Controlled Calibration
- General Purpose Trimming Adjustments

GENERAL DESCRIPTION

The DAC-8800 TrimDAC™ is designed to be a general purpose digitally controlled voltage adjustment device. The output voltage range can be independently set for each set of four D/A converters. In addition, both unipolar and bipolar output voltage ranges are easy to establish by external reference input high and low terminals. The digitally-programmed output voltages are ideal for op amp trimming, voltage-controlled amplifier gain setting and any general purpose trimming tasks.

A three-wire serial digital interface loads the contents of eight internal DAC registers which establish the output voltage levels. An asynchronous Clear ($\overline{CLR}$) input places all DACs in a zero code output condition, very handy for system power-up. An internal regulator provides TTL input compatibility over a wide range of V_{DD} supply voltages. Single supply operation is available by connecting V_{SS} to GND.

FUNCTIONAL DIAGRAM



ORDERING INFORMATION †

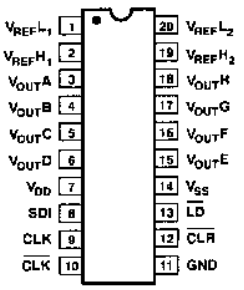
PACKAGE			OPERATING TEMPERATURE RANGE
CERDIP 20-PIN	PLASTIC 20-PIN	SO 20-PIN	
DAC8800BR*	–	–	–55°C to +125°C
DAC8800FR	DAC8800FP	DAC8800FS††	–40°C to +85°C

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP and plastic DIP packages.

†† For availability and burn-in information on SO package, contact your local sales office.

PIN CONNECTIONS



20-PIN CERDIP (R-Suffix)

20-PIN SOL (S-Suffix)

20-PIN EPOXY DIP (P-Suffix)

REV. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 Fax: 617/326-8703 Twx: 710/394-6577
Telex: 924491 Cable: ANALOG NORWOODMASS

ELECTRICAL CHARACTERISTICS: (Note 1) Unless otherwise noted, SINGLE SUPPLY: V_{DD} = +12V, V_{SS} = 0V, $V_{REF}H$ = +5V, $V_{REF}L$ = 0V; or DUAL SUPPLY: V_{DD} = +12V, V_{SS} = –5V, $V_{REF}H$ = +2.5V, $V_{REF}L$ = –2.5V; F GRADE: –40°C ≤ T_A ≤ +85°C; B GRADE: –55°C ≤ T_A ≤ +125°C.

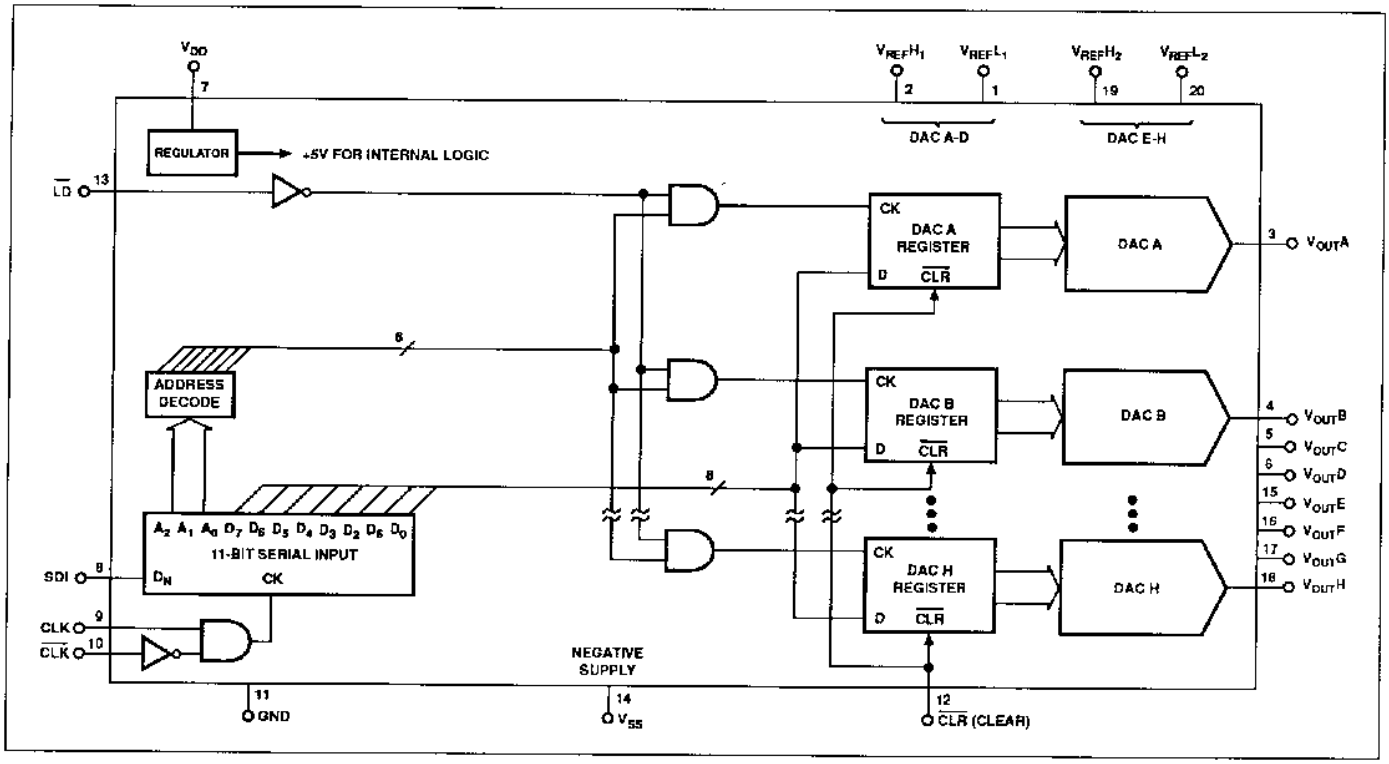
PARAMETER	SYMBOL	CONDITIONS	DAC-8800 MIN	TYP	MAX	UNITS
STATIC ACCURACY	All specifications apply for DACs A, B, C, D, E, F, G, H					
Resolution	N		8	–	–	Bits
Total Unadjusted Error (Note 2)	TUE		–	–	±1/2	LSB
Differential Nonlinearity (Note 3)	DNL		–	–	±1	LSB
Full Scale Error	G_{FSE}		–	–	±1/2	LSB
Zero Code Error	V_{ZSE}		–	–	±1/2	LSB
DAC Output Resistance	R_{OUT}		8	12	16	kΩ
DAC Output Resistance Match	$\Delta R_{OUT}/R_{OUT}$		–	0.5	–	%
REFERENCE INPUT						
Voltage Range (Note 5)	$V_{REF}H$	Pins 2 & 19	$V_{REF}L$	–	$(V_{DD} - 4)$	V
	$V_{REF}L$	Pins 1 & 20	V_{SS}	–	$V_{REF}H$	
Input Resistance	$V_{REF}H$	Digital Inputs = 55_H	2	3	–	kΩ
Input Resistance Match	$\Delta R_{REF}H/R_{REF}H$	Digital Inputs = 55_H	–	0.5	–	%
Reference Input Capacitance (Note 4)	C_{REF}	Digital Inputs All Zeros Digital Inputs All Ones	– –	50 75	75 100	pF
DIGITAL INPUTS						
Logic High	V_{INH}		2.4	–	–	V
Logic Low	V_{INL}		–	–	0.8	V
Input Current	I_{IN}	V_{IN} = 0V or +5V	–	–	±1	µA
Input Capacitance (Note 4)	C_{IN}		–	4	8	pF
Input Coding				BINARY		
POWER SUPPLIES (Note 6)						
Positive Supply Current	I_{DD}	Dual Supply TTL Dual Supply CMOS	– –	1 0.2	2 0.4	mA
Negative Supply Current	I_{SS}	Dual Supply	–	0.01	0.2	mA
Power Dissipation	P_{DISS}	Single Supply Operation Dual Supply Operation	– –	12 12	24 25	mW
DC Power Supply Rejection Ratio	PSRR	ΔV_{DD} =±5%	–	0.001	0.01	%/%
DYNAMIC PERFORMANCE (Note 4)						
V_{OUT} Settling Time	t_S	±1/2 LSB Error Band	–	0.8	2	µs
Channel-to-Channel Crosstalk (Note 7)	CT	Measured Between Adjacent DAC Outputs	–	80	–	nVs

ELECTRICAL CHARACTERISTICS: (Note 1) Unless otherwise noted, SINGLE SUPPLY: V_{DD} = +12V, V_{SS} = 0V, $V_{REF}H$ = +5V, $V_{REF}L$ = 0V; or DUAL SUPPLY: V_{DD} = +12V, V_{SS} = –5V, $V_{REF}H$ = +2.5V, $V_{REF}L$ = –2.5V; F GRADE: –40°C ≤ T_A ≤ +85°C; B GRADE: –55°C ≤ T_A ≤ +125°C. *Continued*

PARAMETER	SYMBOL	CONDITIONS	DAC-8800 MIN	TYP	MAX	UNITS
SWITCHING CHARACTERISTICS (Notes 4, 8)						
Input Clock Pulse Width	t_{CH}, t_{CL}	Clock Level High or Low	60	–	–	ns
Data Setup Time	t_{DS}		30	–	–	ns
Data Hold Time	t_{DH}		30	–	–	ns
DAC Register Load Pulse Width	t_{LD}		50	–	–	ns
Clear Pulse Width	t_{CLR}		50	–	–	ns
Clock Edge to Load Time	t_{CKLD}		50	–	–	ns
Load Edge to Next Clock Edge Time	t_{LDCK}		50	–	–	ns

NOTES:
1. Testing performed in SINGLE SUPPLY mode, except I_{DD}, I_{SS}, and PSRR which are tested in DUAL SUPPLY mode.
2. Includes Full Scale Error, Relative Accuracy, and Zero Code Error.
3. All devices guaranteed monotonic over the full operating temperature range.
4. Guaranteed by design and not subject to production test.
5. V_{DD} – 4 volts is the maximum reference voltage for the above specifications. Also $V_{REF}H \geq V_{REF}L$.
6. Digital Input voltages $V_{IN} = V_{INL}$ or V_{INH} for TTL condition; V_{IN} = 0V or +5V for CMOS condition. DAC outputs unloaded. P_{DISS} is calculated from $(I_{DD} \times V_{DD}) + (I_{SS} \times V_{SS})$.
7. Measured at V_{OUT} pin where an adjacent V_{OUT} pin is making a full-scale voltage change.
8. See timing diagram for location of measured values.

DETAILED DAC-8800 BLOCK DIAGRAM



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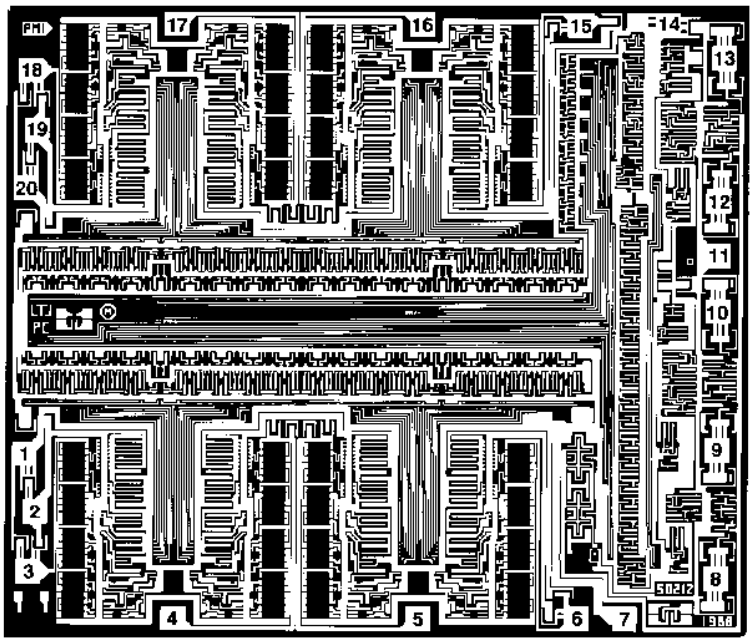
DICE CHARACTERISTICS



DIE SIZE 0.151 × 0.130 Inch, 19,630 sq. mils
(3.8354 × 3.3033 mm, 12.664 sq. mm)

1. $V_{REF}L_1$
2. $V_{REF}H_1$
3. $V_{OUT}A$
4. $V_{OUT}B$
5. $V_{OUT}C$
6. $V_{OUT}D$
7. V_{DD}
8. SDI
9. CLK
10. $\overline{CLK}$
11. GND
12. $\overline{CLR}$
13. $\overline{LD}$
14. V_{SS}
15. $V_{OUT}E$
16. $V_{OUT}F$
17. $V_{OUT}G$
18. $V_{OUT}H$
19. $V_{REF}H_2$
20. $V_{REF}L_2$

WAFER TEST LIMITS at V_{DD} = +12V, V_{SS} = 0V, $V_{REF}H$ = +5V, $V_{REF}L$ = 0V; T_A = +25°C unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS		DAC-8800G LIMIT	UNITS
Total Unadjusted Error	TUE			±1/2	LSB MAX
Differential Nonlinearity	DNL			±1	LSB MAX
Full Scale Error	G_{FSE}			±1/2	LSB MAX
Zero Code Error	V_{ZSE}			±1/2	LSB MAX
DAC Output Resistance	R_{OUT}			8 16	kΩ MIN kΩ MAX
Reference Input Resistance	$R_{REF}H$	Digital Inputs = 55H		2	kΩ MIN
Digital Inputs High	V_{INH}			2.4	V MIN
Digital Inputs Low	V_{INL}			0.8	V MAX
Digital Input Current	I_{IN}	V_{IN} = 0V or +5V		±1	µA MAX
Positive Supply Current	I_{DD}	V_{SS} = −5V	TTL CMOS	2 0.4	mA MAX
Negative Supply Current	I_{SS}	V_{SS} = −5V		0.2	mA MAX
DC Power Supply Rejection Ratio	PSRR	ΔV_{DD} = ±5%		0.01	%/% MAX

NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted)

V_{DD} to V_{SS} ..... 0V, +20V
V_{DD} to GND ..... 0V, +20V
V_{SS} to GND ..... –20V, 0V
Digital Input Voltage to GND ..... GND – 0.3V, V_{DD} + 0.3V
$V_{REF}H$ to GND ..... $V_{REF}L$, V_{DD}
$V_{REF}L$ to GND ..... V_{SS}, $V_{REF}H$
V_{OUT} to GND ..... $V_{REF}L$, $V_{REF}H$
Operating Temperature Range
Military, DAC-8800BR ..... –55°C to +125°C
Extended Industrial, DAC-8800FR,FP,FS ...–40°C to +85°C
Maximum Junction Temperature (T_j Max) ..... +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Package Power Dissipation ..... $(T_j \text{ Max} - T_A)/\Theta_{jA}$

PACKAGE TYPE	Θ_{jA} (Note 1)	Θ_{jC}	UNITS
20-Pin Hermetic DIP (R)	76	11	°C/W
20-Pin Plastic DIP (P)	69	27	°C/W
20-Pin SO (S)	88	25	°C/W

NOTE:
1. Θ_{jA} is specified for worst case mounting conditions, i.e., Θ_{jA} is specified for device in socket for CerDIP, and P-DIP packages; Θ_{jA} is specified for device soldered to printed circuit board for SO package.

CAUTION:
1. Do not apply voltages higher than V_{DD} or less than V_{SS} potential on any terminal.
2. The digital control inputs are zener-protected; however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
3. Do not insert this device into powered sockets; remove power before insertion or removal.
4. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to device.

TABLE 1: PIN Function Description

PIN	MNEMONIC	DESCRIPTION
1	$V_{REF}L_1$	External DAC voltage reference input shared by DAC A, B, C, D. $V_{REF}L_1$ determines the lowest negative DAC output voltage. $V_{REF}L_1$ must be equal to or more positive than V_{SS}.
2	$V_{REF}H_1$	External DAC voltage reference input shared by DAC A, B, C, D. $V_{REF}H_1$ determines the highest positive DAC output voltage.
3	$V_{OUT}A$	DAC A Output } Output voltage determined by external $V_{REF}H_1$ and $V_{REF}L_1$.
4	$V_{OUT}B$	DAC B Output
5	$V_{OUT}C$	DAC C Output
6	$V_{OUT}D$	DAC D Output
7	V_{DD}	Positive supply, allowable input voltage range +4.5V to +16V.
8	SDI	Serial Data Input } TTL Input Compatible
9	CLK	Serial Clock Input, positive edge triggered
10	$\overline{CLK}$	Clock Enable or Serial Clock Input, negative edge triggered
11	GND	Ground
12	$\overline{CLR}$	Clear Input (Active Low). Asynchronous TTL compatible input that resets all DAC registers to zero code.
13	$\overline{LD}$	Load DAC Register Strobe, TTL compatible input that transfers data bits from serial input register into the decoded DAC register. See Table 2.
14	V_{SS}	Negative Supply, allowable input voltage range 0V to –12V.
15	$V_{OUT}E$	DAC E Output } Output voltage determined by external $V_{REF}H_2$ and $V_{REF}L_2$.
16	$V_{OUT}F$	DAC F Output
17	$V_{OUT}G$	DAC G Output
18	$V_{OUT}H$	DAC H Output
19	$V_{REF}H_2$	External DAC voltage reference input shared by DAC E, F, G, H. $V_{REF}H_2$ determines the highest positive DAC output voltage.
20	$V_{REF}L_2$	External DAC voltage reference input shared by DAC E, F, G, H. $V_{REF}L_2$ determines the lowest negative DAC output voltage. $V_{REF}L_2$ must be equal to or more positive than V_{SS}.

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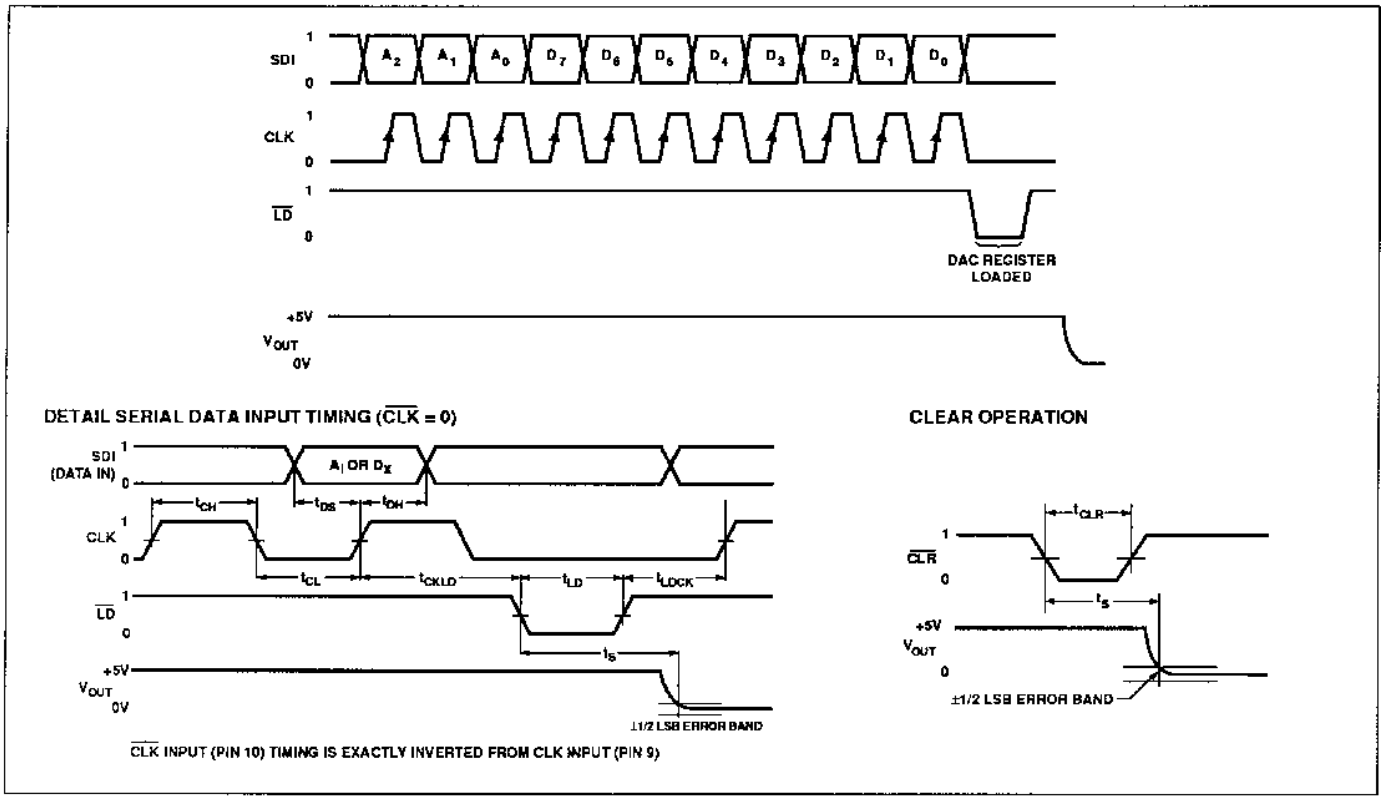


FIGURE 1: *Timing Diagrams*

TABLE 2: Serial Input Decode Table

LAST → FIRST

LSB D0	D1	D2	D3	D4	D5	D6	MSB D7	LSB A0	A1	MSB A2

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0	DAC OUTPUT VOLTAGE (K = $V_{REF}H - V_{REF}L$)
0	0	0	0	0	0	0	0	$V_{REF}L$
0	0	0	0	0	0	0	1	(1/256) x K + $V_{REF}L$
				⋮				
0	1	1	1	1	1	1	1	(127/256) x K + $V_{REF}L$
1	0	0	0	0	0	0	0	(128/256) x K + $V_{REF}L$
1	0	0	0	0	0	0	1	(129/256) x K + $V_{REF}L$
				⋮				
1	1	1	1	1	1	1	1	(255/256) x K + $V_{REF}L$

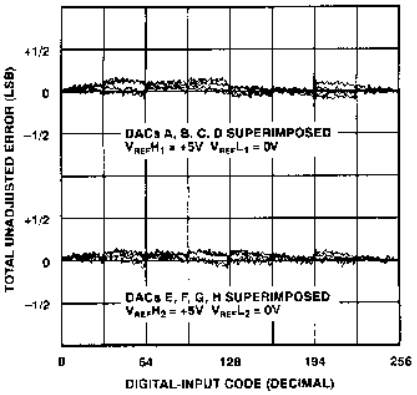
MSB A2	A1	LSB A0	DAC UPDATED
0	0	0	DAC A
0	0	1	DAC B
0	1	0	DAC C
0	1	1	DAC D
1	0	0	DAC E
1	0	1	DAC F
1	1	0	DAC G
1	1	1	DAC H

TABLE 3: Logic Control Input Truth Table

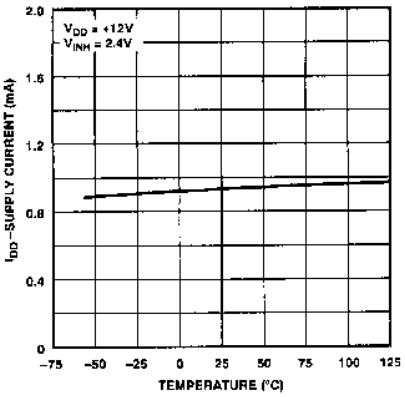
CLK	$\overline{CLK}$	INPUT SHIFT REGISTER OPERATON
↑	L	Shift Data
H	↓	Shift Data
L	X	No Operation
X	H	No Operation

TYPICAL PERFORMANCE CHARACTERISTICS

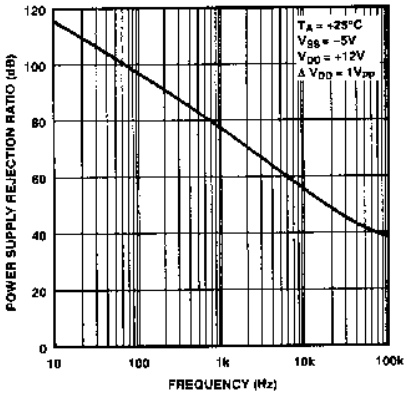
TOTAL UNADJUSTED ERROR vs DIGITAL INPUT CODE



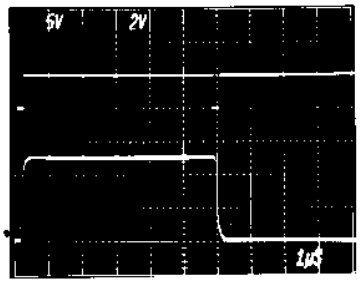
SUPPLY CURRENT vs TEMPERATURE



POWER SUPPLY REJECTION RATIO vs FREQUENCY

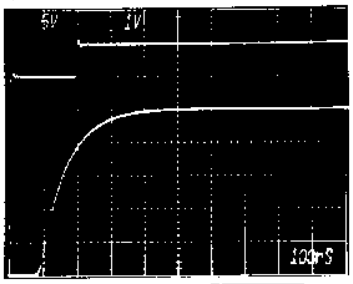


DAC OUTPUT SETTLING TIME POSITIVE & NEGATIVE TRANSITIONS



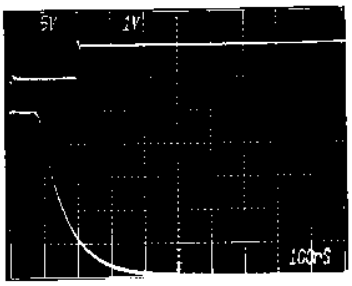
UPPER TRACE: t_{LD} INPUT (5V/DIV)
LOWER TRACE: V_{OUT}A (2V/DIV)
CONDITIONS: V_{DD} = +12V, $V_{REF}H_1$ = +5V, $V_{REF}L_1$ = 0V, V_{SS} = 0V, R_L = 1MΩ, C_L = 3.4pF

EXPANDED DAC OUTPUT SETTLING TIME POSITIVE TRANSITION



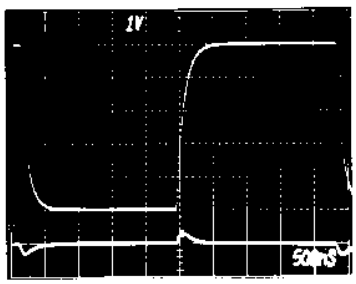
UPPER TRACE: t_{LD} INPUT (5V/DIV)
LOWER TRACE: V_{OUT}A (1V/DIV)
CONDITIONS: V_{DD} = +12V, $V_{REF}H_1$ = +5V, $V_{REF}L_1$ = 0V, V_{SS} = 0V, R_L = 1MΩ, C_L = 3.4pF

EXPANDED DAC OUTPUT SETTLING TIME NEGATIVE TRANSITION



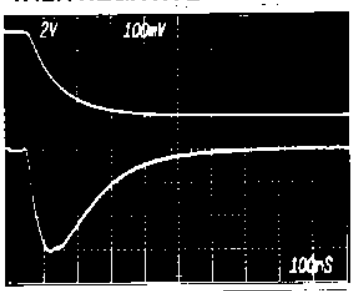
UPPER TRACE: t_{LD} INPUT (5V/DIV)
LOWER TRACE: V_{OUT}A (1V/DIV)
CONDITIONS: V_{DD} = +12V, $V_{REF}H_1$ = +5V, $V_{REF}L_1$ = 0V, V_{SS} = 0V, R_L = 1MΩ, C_L = 3.4pF

DAC OUTPUT CHANNEL-TO-CHANNEL CROSSTALK BOTH TRANSITIONS



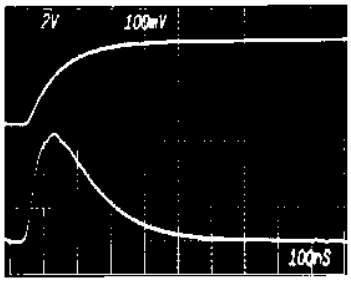
UPPER TRACE: V_{OUT}A 0 TO +5V CHANGE
LOWER TRACE: V_{OUT}B (1V/DIV)
CONDITIONS: V_{DD} = +12V, $V_{REF}H_1$ = +5V, $V_{REF}L_1$ = 0V, V_{SS} = 0V, R_L = 1MΩ, C_L = 3.4pF

EXPANDED DAC OUTPUT CHANNEL-TO-CHANNEL CROSS-TALK NEGATIVE TRANSITION



UPPER TRACE: V_{OUT}A +5V TO 0V CHANGE
LOWER TRACE: V_{OUT}B (100mV/DIV)
CONDITIONS: V_{DD} = +12V, $V_{REF}H_1$ = +5V, $V_{REF}L_1$ = 0V, V_{SS} = 0V, R_L = 1MΩ, C_L = 3.4pF

EXPANDED DAC OUTPUT CHANNEL-TO-CHANNEL CROSS-TALK POSITIVE TRANSITION



UPPER TRACE: V_{OUT}A 0 TO +5V CHANGE
LOWER TRACE: V_{OUT}B (100mV/DIV)
CONDITIONS: V_{DD} = +12V, $V_{REF}H_1$ = +5V, $V_{REF}L_1$ = 0V, V_{SS} = 0V, R_L = 1MΩ, C_L = 3.4pF

DAC8800

CIRCUIT OPERATION

The DAC-8800 provides a programmable voltage output adjustment capability. Changing the programmed output voltage of each DAC is accomplished by clocking in an 11-bit serial data word into pin SDI (Serial Data Input). The format of this data word is three address bits, MSB first, followed by 8 data bits, MSB first. Table 2 provides the serial input decode table for data loading. DAC outputs can be changed one at a time in random sequence. The fast serial-data clocking of 6.6MHz makes it possible to load all 8 DACs in as little time as 14 microseconds. The exact timing requirements are provided in Figure 1.

A clear ($\overline{CLR}$) input pin allows the circuit to be powered-up in the all zero state or a system reset pulse connected to $\overline{CLR}$ can asynchronously clear all data registers.

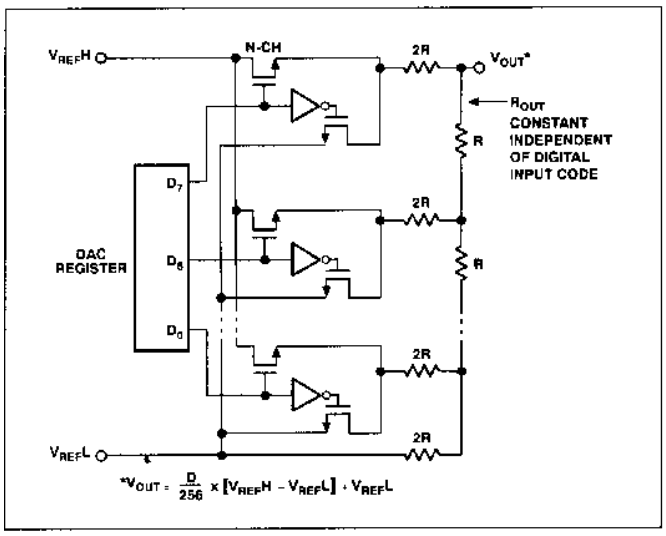


FIGURE 2: *DAC-8800 TrimDAC™ Equivalent DAC Circuit*

The output voltage range is determined by the external input voltages applied to $V_{REF}H$ and $V_{REF}L$. See Figure 2 for a simplified equivalent DAC circuit. If a negative supply is used on V_{SS} then $V_{REF}L$ may be set negative resulting in a programmable bipolar output voltage swing.

The actual output voltage, V_{OUT}, depends on $V_{REF}H$ and $V_{REF}L$ as follows:

$$V_{OUT}(D) = D \times (V_{REF}H - V_{REF}L)/256 + V_{REF}L$$

where D is a whole number binary digital input word loaded into the DAC register. For example, when $V_{REF}H$ = +5V and $V_{REF}L$ = 0V unipolar output operation results with the following binary digital inputs:

D	$V_{OUT}(D)$	$V_{REF}H$ = +5.00V; $V_{REF}L$ = 0V
255	4.98V	Full-Scale
128	2.50V	Half-Scale
1	0.02V	1 LSB
0	0.00V	Zero-Scale also generated When $\overline{CLR}$ Input Activated

Bipolar output operation is achieved when $V_{REF}H$ = +2.5V and $V_{REF}L$ = –2.5V, also note V_{SS} must be equal to or more negative than $V_{REF}L$. V_{SS} = –5V is a good choice for this example. The following example lists the actual bipolar output voltages produced by the binary digital input which would now be considered offset-binary coded:

D	$V_{OUT}(D)$	$V_{REF}H$ = +2.50V; $V_{REF}L$ = –2.50V
255	2.48V	Positive Full-Scale
129	0.02V	Positive 1 LSB
128	0.00V	Bipolar Zero-Scale
127	–0.02V	Negative 1 LSB
0	–2.50V	Negative Full-Scale

REFERENCE INPUTS ($V_{REF}H_1$, $V_{REF}L_1$, $V_{REF}H_2$, $V_{REF}L_2$)

The external voltages connected to the V_{REF} input pins determine the programmable output voltage ranges of the two sets of four DACs in the DAC-8800. Specifically, $V_{REF}H_1$ and $V_{REF}L_1$ are connected to DACs, A, B, C, D, and $V_{REF}H_2$ and $V_{REF}L_2$ are connected to DACs E, F, G, H.

Inspection of the DAC-8800 equivalent DAC circuit (Figure 2) shows the external $V_{REF}H$ and $V_{REF}L$ inputs connected to the internal DAC switches. During updating, the DAC switches produce transient current flowing from $V_{REF}H$ to $V_{REF}L$. It is recommended to place 0.01µF bypass capacitors across the $V_{REF}H$ and $V_{REF}L$ inputs to minimize the voltage transients.

A wide range of external voltage references can be used subject to the reference input voltage range boundary conditions. First $V_{REF}H$ should always be more positive than $V_{REF}L$. DC voltages are recommended. $V_{REF}L$ can be equal to the negative power supply V_{SS}. This feature results in single supply operation when V_{SS} is at ground. $V_{REF}H$ should not be closer than four volts to V_{DD}. This is due to the DAC-8800 NMOS only DAC switches which will no longer operate properly if $V_{REF}H$ is closer to V_{DD} than four volts. Total unadjusted error degrades when ($V_{DD} - V_{REF}H$) is less than four volts as shown in Figure 3.

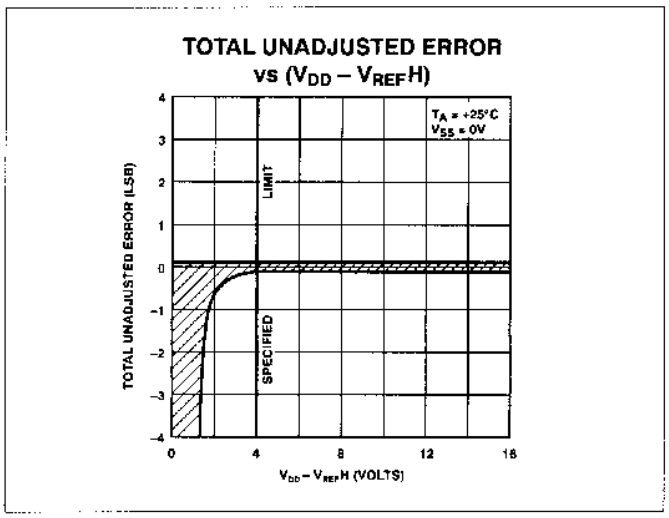


FIGURE 3: *Effect on TUE Operating Beyond ($V_{DD} - V_{REF}H$) > 4V Limit*

RECOMMENDED OPERATING POWER SUPPLY VOLTAGE RANGES

Although the DAC-8800 is thoroughly specified for operation with V_{DD} = +12V and V_{SS} = 0V or–5V, it will still function with the following recommended boundary conditions:

- $(V_{DD} - V_{SS}) < 18V$
- $4.5V < V_{DD} < 16V$
- $0V > V_{SS} > -12V$

In all cases the reference voltage boundary conditions still apply. The boundary conditions described here make it possible to use DAC-8800 with a wide variety of readily available supply voltages. Some choices include, but are not limited to:

V_{DD}/V_{SS} = +15V/0V; +12V/0V; +12V/–5V; +5V/–5V; +5V/–12V

DAC OUTPUTS (V_{OUT} A, B, C, D, E, F, G, H)

The eight D/A converter voltage outputs have a constant output resistance independent of digital input code. The distribution of R_{OUT} from DAC to DAC within the DAC-8800 typically matches by 0.5%. Device to device R_{OUT} matching is process-lot to process-lot dependent having a ±20% variation. The change in R_{OUT} with temperature is very small as a result of PMI's low temperature coefficient SiCr thin-film resistor process.

The nominal DAC output capacitance measures three picofarads and has little variation with temperature.

One aspect of the nominal 12.5kΩ DAC output resistance is channel-to-channel crosstalk. Under a worst case condition of adjacent DAC outputs when DAC A makes a five volt output voltage change DAC B exhibits a 300mV voltage transient. See photograph in typical characteristics section of data sheet.

The channel-to-channel crosstalk is due to the 0.15pF inter-pin package capacitance. A FET probe with 3.4pF input capacitance was used to measure the DAC output channel-to-channel crosstalk characteristics shown. In voltage transient sensitive applications, minimization of crosstalk can be accomplished by placing ground traces between adjacent DAC output pins. DAC output bypass capacitors will also minimize voltage transients.

Output settling time has a dominant pole response as the photograph in the typical characteristics section shows. The output settling time characteristic consists of an 80 nanosecond propagation delay followed by a single RC decay waveform determined by the nominal R_{OUT} of 12.5kΩ times C_{OUT} plus C_{LOAD} which includes the oscilloscope probe.

The digital feedthrough from the serial data inputs (CLK, and SDI) to the DAC outputs measures less than 20mV.

DIGITAL INTERFACING

The DAC-8800 contains a standard three-wire serial input control interface. The three inputs are clock (CLK), load ($\overline{LD}$), and serial data input (SDI). A $\overline{CLK}$ input pin is available for negative edge triggered data loading. The edge sensitive clock input pin requires clean transitions to avoid clocking incorrect data into the serial input register. Standard logic families work well. If mechanical switches are used for product evaluation they should be debounced by a flip-flop or other suitable means.

The logic control input truth table (Table 3) defines operation of the serial data input register.

The CLK input is used to place data in the serial data input register. The unused clock input (CLK or $\overline{CLK}$) should be tied to the active state (CLK = 1 or $\overline{CLK}$ = 0 for active). The load strobe ($\overline{LD}$) which must follow the eleventh active CLK edge transfers the

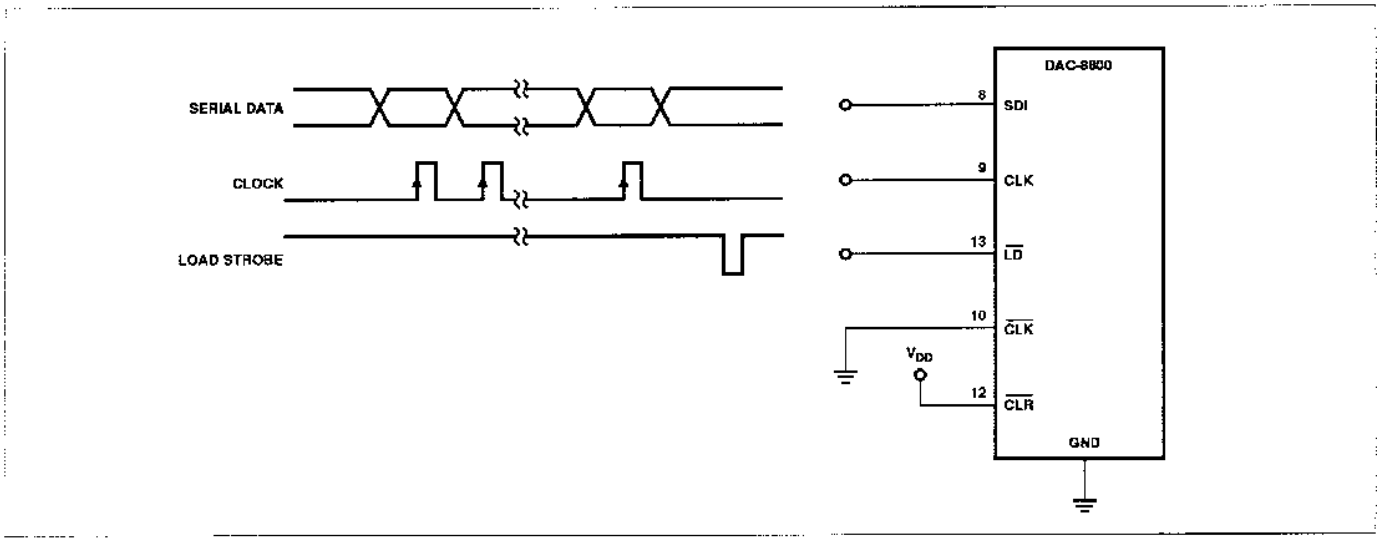


FIGURE 4: *Three-Wire Serial Interface Connections*

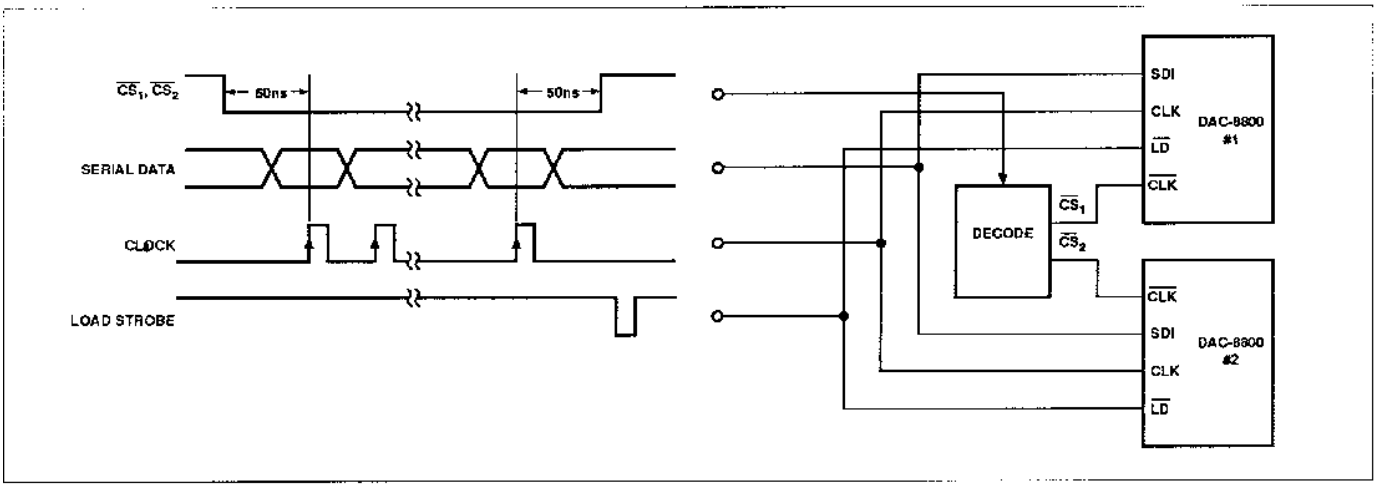


FIGURE 5a: *Decoding Multiple DAC-8800s*

data from the serial data input register to the DAC register decoded from the first three address bits clocked into the input register. Any extra CLK edges after the eleventh edge looses the first bits shifted in. See Table 2 for a complete description. See Figure 4 for an example using the CLK input pin to clock data into the SDI.

The unused clock input of Figure 4 can be used to provide a chip select ($\overline{CS}$) feature for applications using more than one DAC-8800. Figure 5a shows the proper connection and timing of the CLK inputs which assures that the $\overline{CLK}$ acting as a chip select ($\overline{CS}$) is taken to the active low state selecting the desired DAC-8800.

Another method of decoding multiple DAC-8800s is shown in Figure 5b. Here all the DAC serial input registers receive the same input data; however, only one of DAC's $\overline{LD}$ input is activated to transfer its serial input register contents into the destination DAC register. In this circuit the $\overline{LD}$ timing generated by the address decoder should follow the DAC-8800 standard timing requirements. Note the address decoder should not be activated by its $\overline{WR}$ input while the coded address inputs are changing.

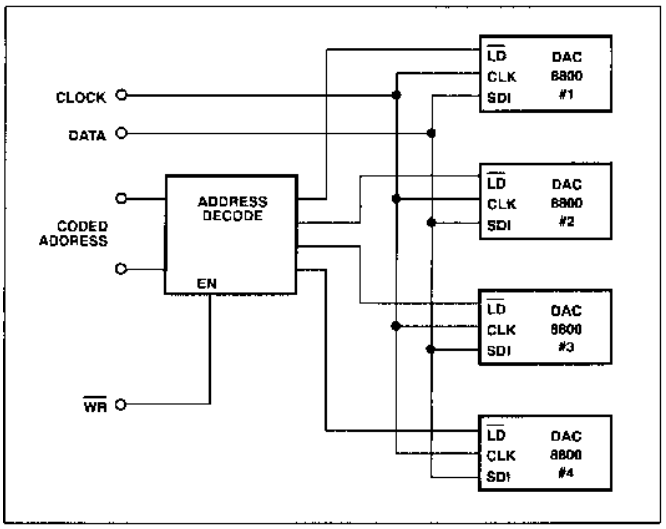


FIGURE 5b: *Decoding Multiple DAC-8800s Using the $\overline{LD}$ Input Pin*

APPLICATIONS

DIGITALLY PROGRAMMABLE AUDIO AMPLIFIER

The DAC-8800 is well suited to digitally control the gain or attenuation settings of eight voltage controlled amplifiers (VCAs). In professional audio mixing consoles, music synthesizers and other audio processor's VCAs, such as the SSM-2014, adjust audio channel gain and attenuation from front panel potentiometers. The VCA provides a clean gain transition control of audio level when the slew rate of the analog input control voltage (V_C) is properly chosen. Taking advantage of the 12.5kΩ nominal output resistance of the DAC-8800 it is very easy to control the slew rate of V_{OUT} by appropriate selection of C_{OUT}. Figure 6 shows one channel of a digitally programmable audio amplifier.

The reference high ($V_{REF}H$) and reference low ($V_{REF}L$) input voltages of the DAC-8800 provide a digitally programmable output voltage of −1.2V to +1.2V which is connected to the control voltage (V_C) input terminal of the SSM-2014 VCA. The gain of the SSM-2014 is guaranteed to change from −15dB to + 15dB for 1.2 to −1.2V input V_C voltage. A C_{OUT} of 0.1μF provides a control voltage transition time of 1.2ms which generates a click free change in audio channel gain.

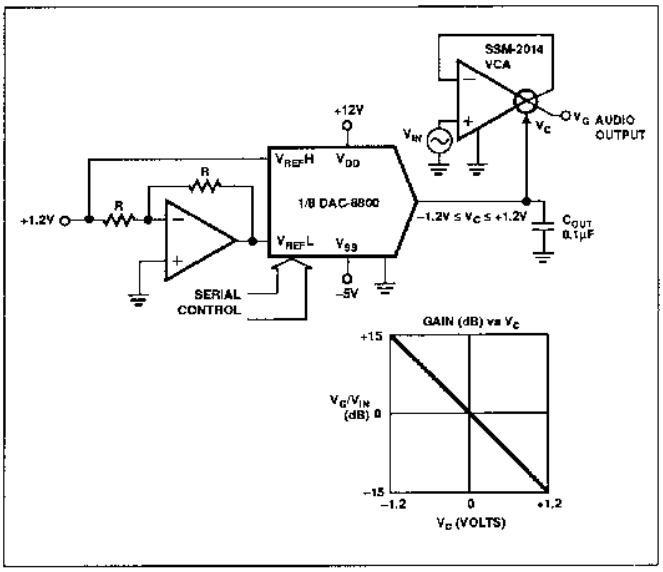


FIGURE 6: *Digitally Programmable Amplifier*

BUFFERING THE DAC-8800 OUTPUT

External op amps can be used to buffer the output of the DAC-8800's nominal 12.5kΩ output resistance. In Figure 7 a variety of possibilities are shown. The quad low power OP-420 is used as a simple buffer to reduce the output resistance of DAC A. The OP-420 was chosen for its wide operating supply range, both single and dual, low power consumption, and low cost.

The next two DACs, B and C, are configured in a summing arrangement where DAC C provides the course output voltage setting and DAC B can be used for fine adjustment. The insertion of R_1 in series with DAC B attenuates its contribution to the voltage sum node at the DAC C output.

DAC D in Figure 7 is in a noninverting gain of two configuration increasing the available output swing to 10V. Appropriate choice of external op amp gain can achieve output voltage swings beyond the range of the DAC-8800 if the external op amp power supply voltages are sufficiently high. In addition, the op amp feedback network termination could be a bias voltage which would provide an offset to the output signal swing.

SETTING COMPARATOR TRIP POINTS

The DAC-8800 is ideal to provide setpoints for voltage input comparators. In Figure 8 the very low power CMP-404 detects whether input voltage (V_{IN}) is higher or lower than the programmed limit values providing TTL compatible output signals. The compactness of the DAC-8800 makes it ideal for high density testing applications found in pin head electronics.

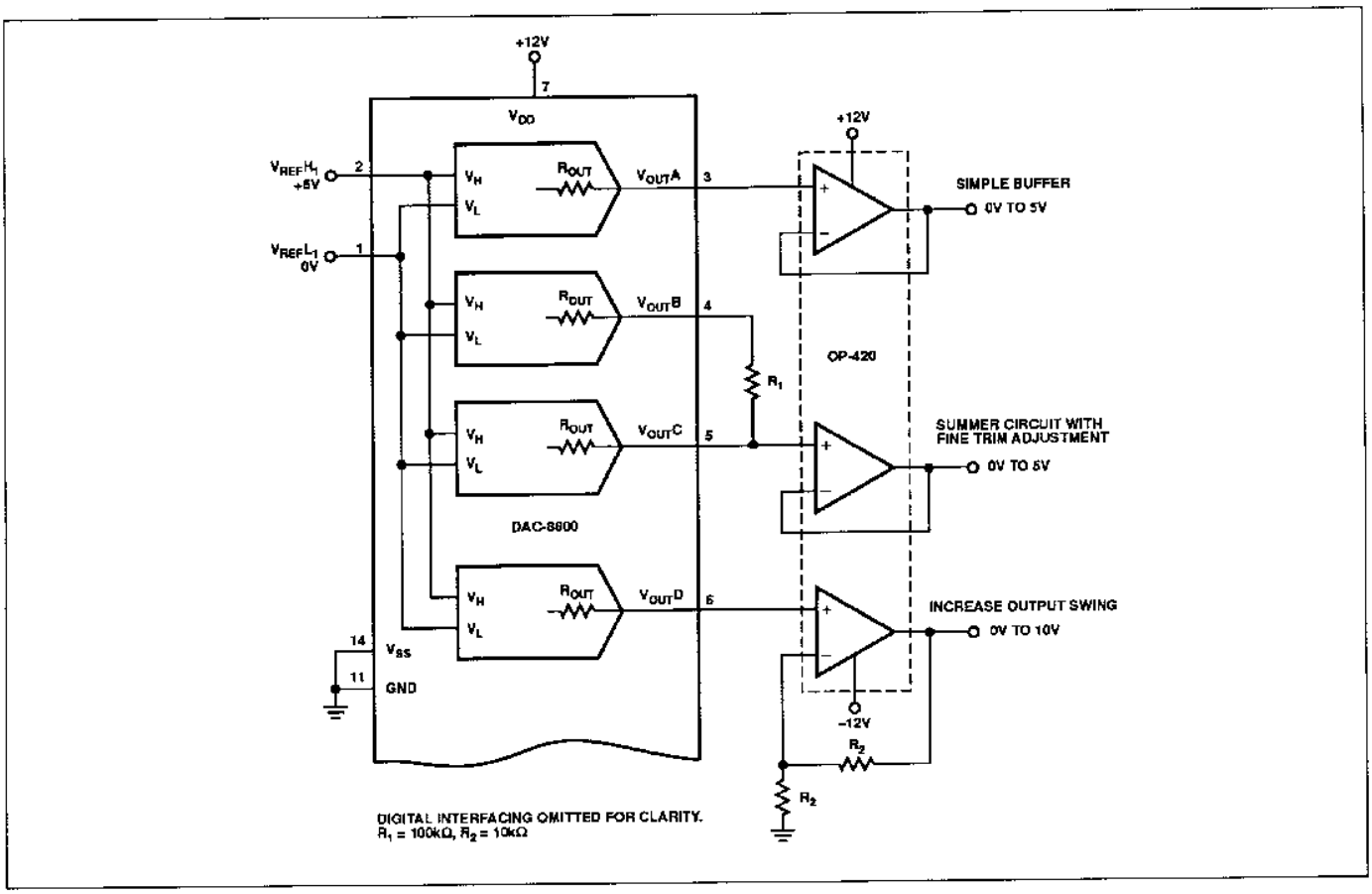


FIGURE 7: *Buffering the DAC-8800 Output*

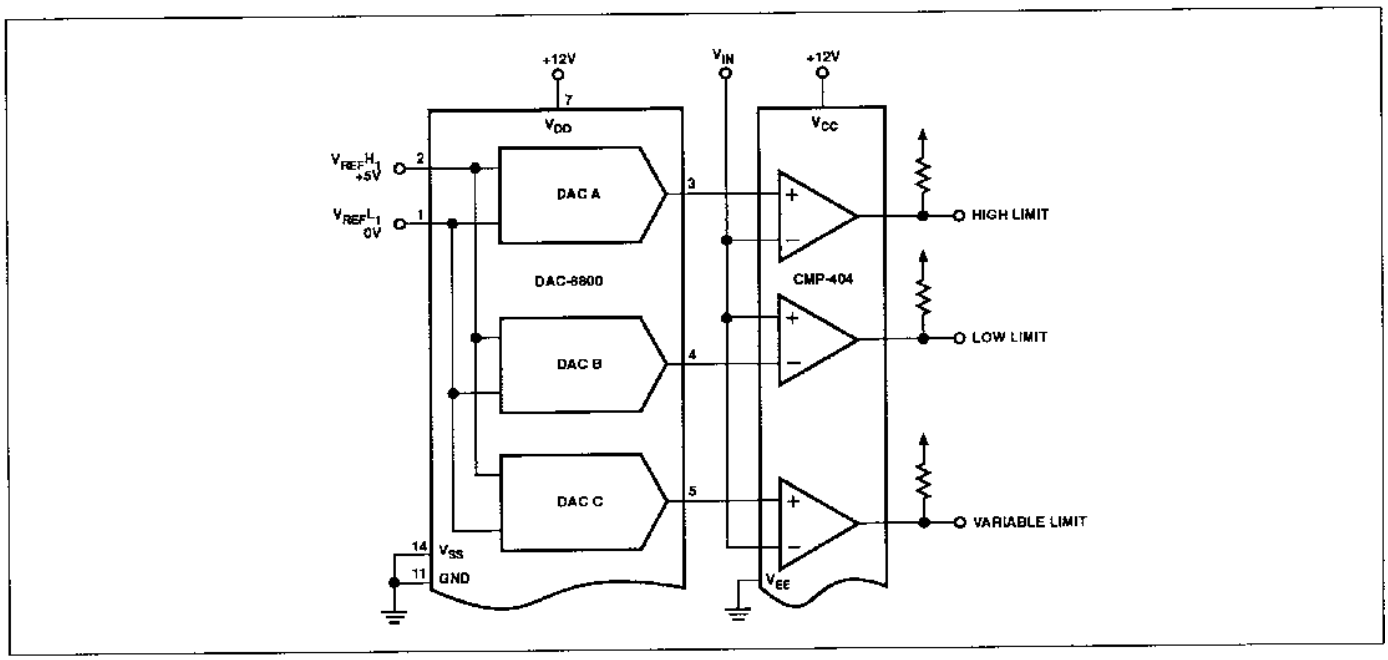


FIGURE 8: *Setting the Comparator Trip Points*

CURRENT SUMMING OUTPUT OPERATIONS

Since the DAC-8800 has a constant output resistance regardless of digital input code, it can be used in a current summing application. Figure 9 depicts the DAC output connected to the inverting input of an OP-20 low power consumption op amp. An external feedback resistor sets the output signal swing according to the formula given. The gain accuracy of this circuit has a wide variation due to the 30% output tolerance of the DAC-8800 R_{OUT} specification. A second DAC in the DAC-8800 could be used with an external resistor summed into the OP-20 current summing node to digitally adjust the full-scale swing.

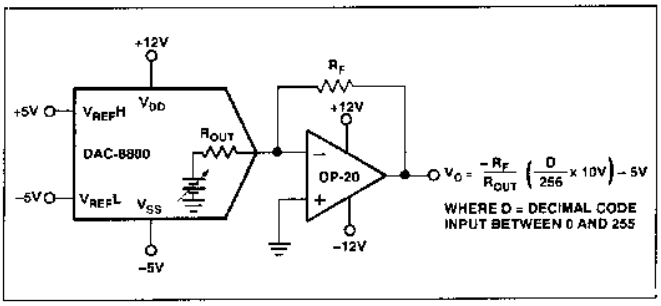


FIGURE 9: *Current Summing Output Operation*

OPTICALLY ISOLATED TWO-WIRE INTERFACE

Two-wire signal interfacing is often found in process control applications where electrical isolation of hazardous environments and minimization of wiring is necessary. Isolation transformers or optocouplers provide the high voltage isolation. Normally the DAC-8800 requires a three-wire interface to update the DAC contents. One technique which translates a two-wire interface into the three-wire signal control required by the DAC-8800 is shown in Figure 10. A single package CMOS-logic dual-retriggerable one-shot MC14538 provides the solution. At rest the optocouplers are both OFF allowing the pull-up resistors to sit at logic high. No undefined transients should occur on the control input line V_C to avoid inadvertently clocking incorrect data into the DAC-8800 serial input register. When it is time to update one of the DAC-8800 DACs, the CONTROL line will go

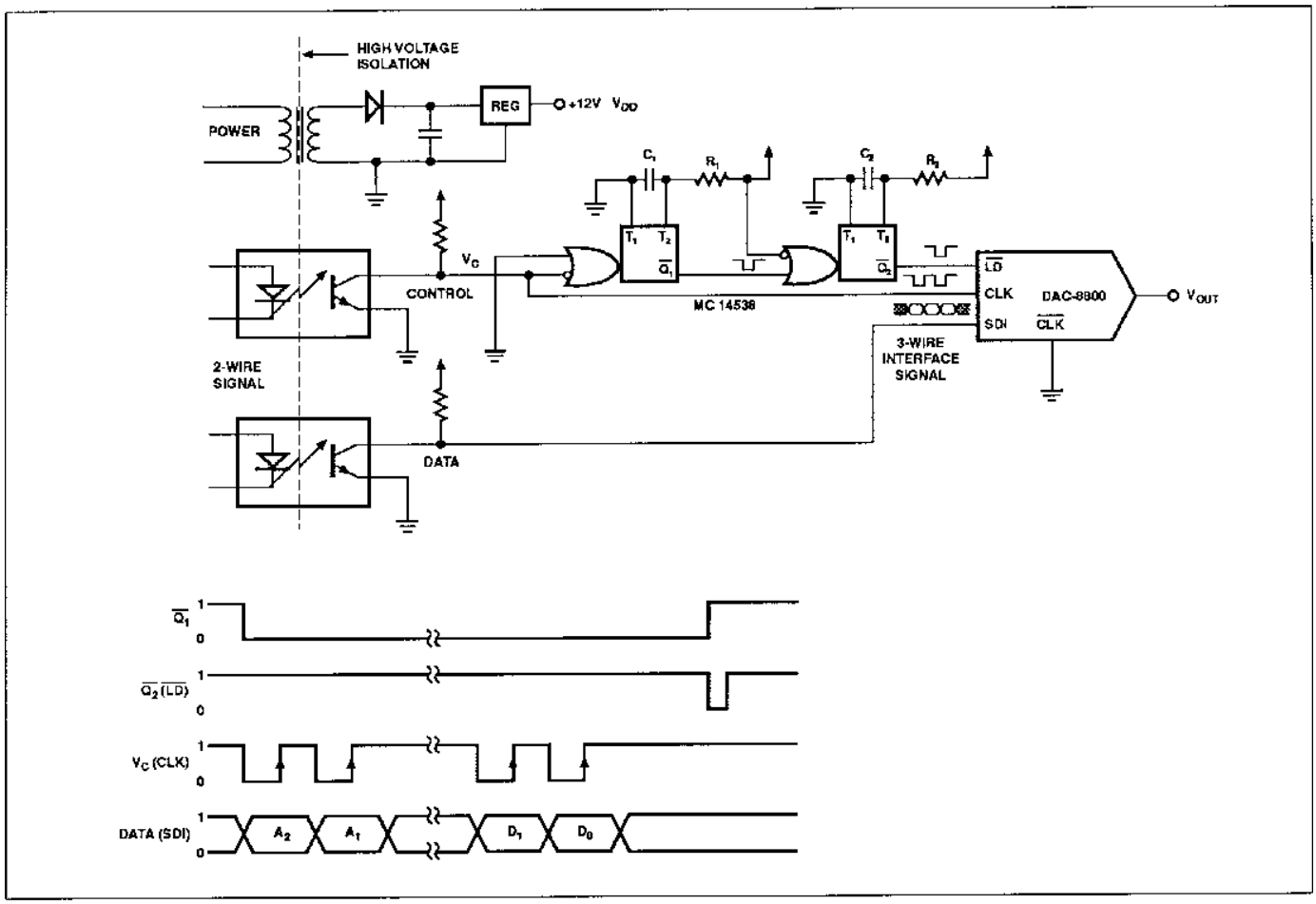
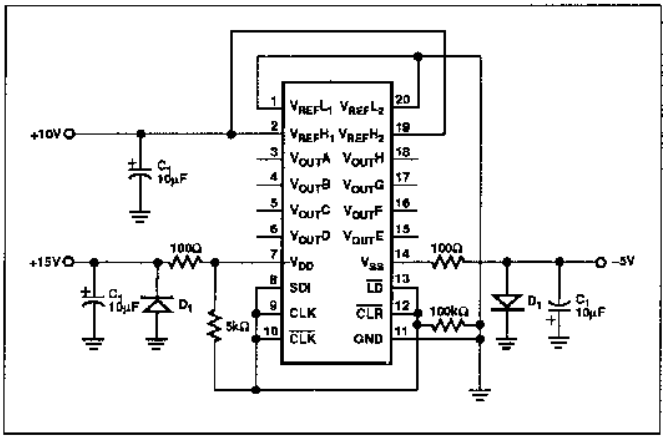


FIGURE 10: *Isolated Two-Wire Signal Interface for Serial Input DAC*

low, triggering the first one-shot ($\overline{Q_1}$). At this time valid data should also be applied to the DATA input optocoupler. Sufficient time must be allowed before the control (V_C) input returns to logic high to make sure the DAC-8800 input data is stabilized. When V_C changes to logic high, the first DATA bit shifts into the DAC-8800 serial data input register. The time constant of the first one-shot established by R_1 and C_1 should be at least twice as long as the basic CONTROL input clock period. This will prevent the $\overline{Q_1}$ output from returning to the high state. The next control input negative edge retriggers the first one-shot and sets up the DAC-8800 clock for the next DATA bit. All eleven positive clock edges will fill the DAC-8800 serial input register and each negative clock edge will retrigger the first one shot. As soon as the CONTROL line returns to the passive state, the first one shot will time out, triggering the second one shot ($\overline{Q_2}$), which will produce the required load $\overline{LD}$ pulse for the DAC-8800 to transfer its serial input register contents to the internal DAC register completing the DAC update. The R_1C_1 and R_2C_2 times need to be designed based on the system's CONTROL-input clock rate. The optocoupler clocking rate must also be considered in setting the system clock rate.

BURN-IN CIRCUIT



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PRINTED IN U.S.A.