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ON Semiconductor
NTD60N02RT4

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sales@integrated-circuit.com

NTD60N02R

Power MOSFET

62 A, 25 V, N−Channel, DPAK

ON Semiconductor®

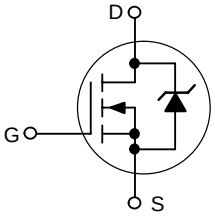
http://onsemi.com

$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
25 V	8.4 mΩ @ 10 V	62 A

Features

- Planar HD3e Process for Fast Switching Performance
- Low $R_{DS(on)}$ to Minimize Conduction Loss
- Low C_{iss} to Minimize Driver Loss
- Low Gate Charge
- Optimized for High Side Switching Requirements in High−Efficiency DC−DC Converters
- Pb−Free Packages are Available

N−Channel

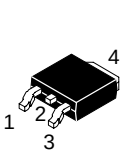


MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

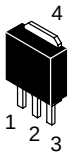
Rating	Symbol	Value	Unit
Drain−to−Source Voltage	V_{DSS}	25	Vdc
Gate−to−Source Voltage − Continuous	V_{GS}	±20	Vdc
Thermal Resistance Junction−to−Case Total Power Dissipation @ T_C = 25°C Drain Current Continuous @ T_C = 25°C, Chip Continuous @ T_C = 25°C, Limited by Package Continuous @ T_A = 25°C, Limited by Wires	 $R_{\theta JC}$ P_D I_D I_D I_D	 2.6 58 62 50 32	 °C/W W A A A
Thermal Resistance Junction−to−Ambient (Note 1) Total Power Dissipation @ T_A = 25°C Drain Current − Continuous @ T_A = 25°C	 $R_{\theta JA}$ P_D I_D	 80 1.87 10.5	 C/W W A
Thermal Resistance Junction−to−Ambient (Note 2) Total Power Dissipation @ T_A = 25°C Drain Current − Continuous @ T_A = 25°C	 $R_{\theta JA}$ P_D I_D	 120 1.25 8.5	 °C/W W A
Operating and Storage Temperature	T_J, and T_{stg}	−55 to 175	°C
Single Pulse Drain−to−Source Avalanche Energy − Starting T_J = 25°C (V_{DD} = 50 Vdc, V_{GS} = 10.0 Vdc, I_L = 11 Apk, L = 1.0 mH, R_G = 25 Ω)	E_{AS}	60	mJ
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

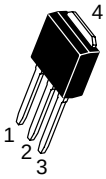
1. When surface mounted to an FR4 board using 0.5 in sq drain pad size.
2. When surface mounted to an FR4 board using the minimum recommended pad size.



CASE 369AA
DPAK
(Surface Mount)
STYLE 2

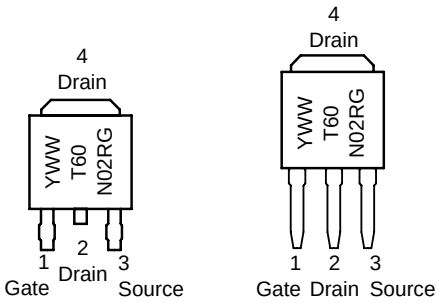


CASE 369AC
3 IPAK
(Straight Lead)



CASE 369D
DPAK
(Straight Lead)
STYLE 2

MARKING DIAGRAM
& PIN ASSIGNMENTS



Y	= Year
WW	= Work Week
T60N02R	= Device Code
G	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

NTD60N02R

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain−to−Source Breakdown Voltage (Note 3) (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)	$V_{(BR)DSS}$	 25 –	 27.5 25.5	 – –	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 20 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 20 Vdc, V_{GS} = 0 Vdc, T_J = 150°C)	I_{DSS}	 – –	 – –	 1.5 10	μAdc
Gate−Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	–	–	±100	nAdc
ON CHARACTERISTICS (Note 3)					
Gate Threshold Voltage (Note 3) (V_{DS} = V_{GS}, I_D = 250 μAdc) Threshold Temperature Coefficient (Negative)	$V_{GS(th)}$	 1.0 –	 1.5 4.1	 2.0 –	Vdc mV/°C
Static Drain−to−Source On−Resistance (Note 3) (V_{GS} = 4.5 Vdc, I_D = 15 Adc) (V_{GS} = 10 Vdc, I_D = 20 Adc) (V_{GS} = 10 Vdc, I_D = 31 Adc)	$R_{DS(on)}$	 – – –	 11.2 8.4 8.2	 12.5 10.5 –	mΩ
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 15 Adc) (Note 3)	g_{FS}	–	27	–	Mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 20 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	–	1000	1330	pF
Output Capacitance		C_{oss}	–	480	640	
Transfer Capacitance		C_{rss}	–	180	225	
SWITCHING CHARACTERISTICS (Note 4)					
Turn−On Delay Time	(V_{GS} = 10 Vdc, V_{DD} = 10 Vdc, I_D = 31 Adc, R_G = 3.0 Ω)	$t_{d(on)}$	–	7.0	–	ns
Rise Time		t_r	–	33	–	
Turn−Off Delay Time		$t_{d(off)}$	–	19	–	
Fall Time		t_f	–	9.0	–	
Gate Charge	(V_{GS} = 4.5 Vdc, I_D = 31 Adc, V_{DS} = 10 Vdc) (Note 3)	Q_T	–	9.5	14	nC
		Q_{GS}	–	2.2	–	
		Q_{GD}	–	5.0	–	
SOURCE−DRAIN DIODE CHARACTERISTICS					
Forward On−Voltage	(I_S = 20 Adc, V_{GS} = 0 Vdc) (Note 3) (I_S = 31 Adc, V_{GS} = 0 Vdc) (I_S = 15 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	 – –	 0.88 1.15 0.80	 1.2 – –	Vdc
Reverse Recovery Time	(I_S = 31 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs) (Note 3)	t_{rr}	–	29.1	–	ns
		t_a	–	13.6	–	
		t_b	–	15.5	–	
Reverse Recovery Stored Charge		Q_{rr}	–	0.02	–	μC

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

NTD60N02R

TYPICAL CHARACTERISTICS

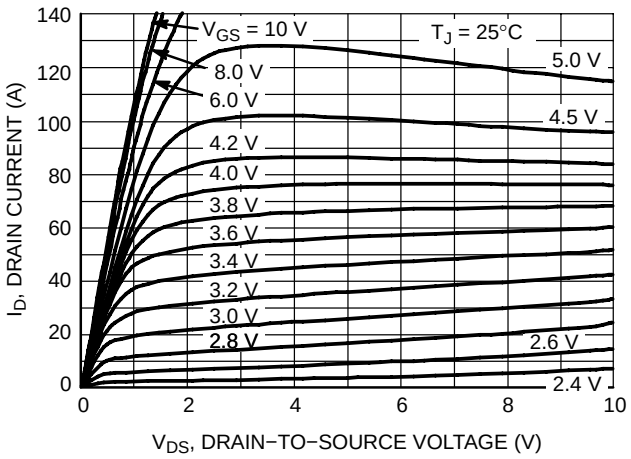


Figure 1. On−Region Characteristics

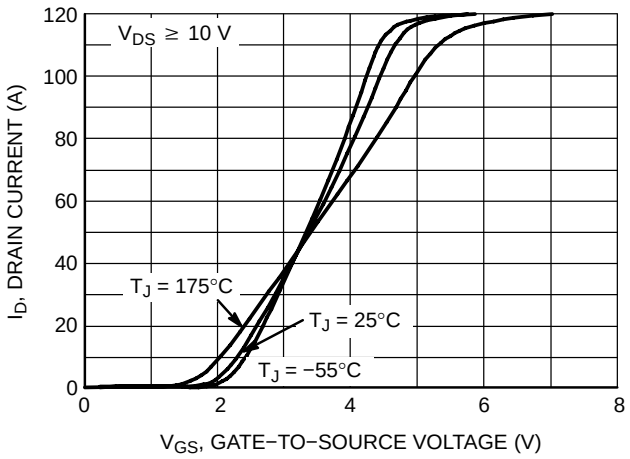


Figure 2. Transfer Characteristics

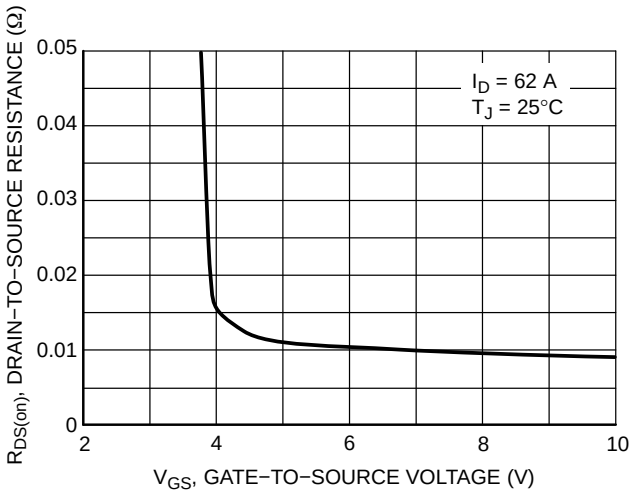


Figure 3. On−Resistance versus Gate−to−Source Voltage

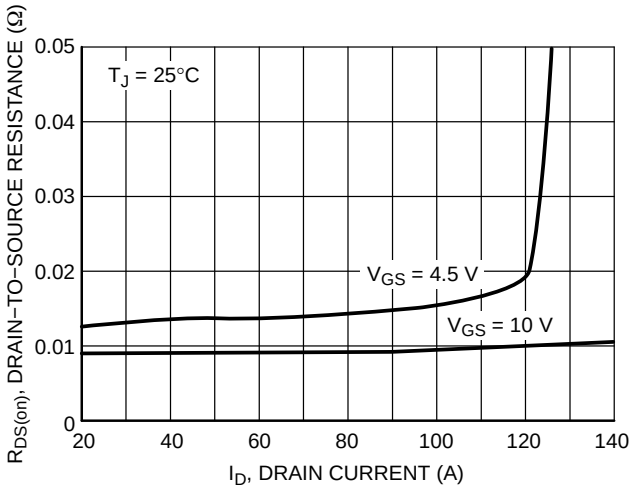


Figure 4. On−Resistance versus Drain Current and Gate Voltage

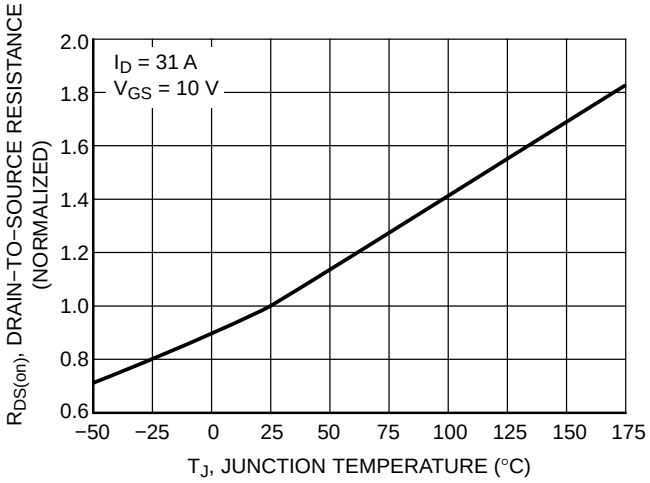


Figure 5. On−Resistance Variation with Temperature

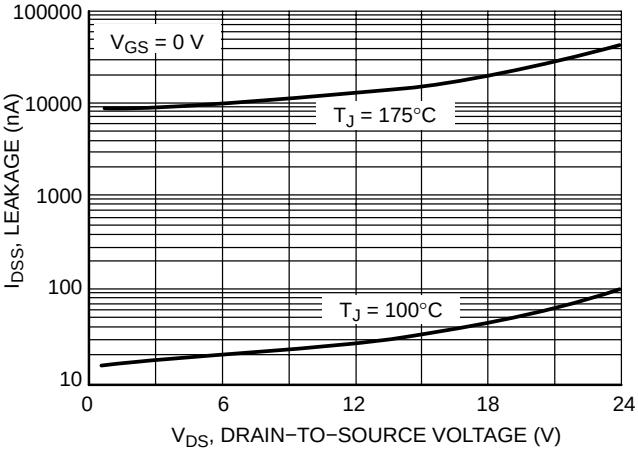


Figure 6. Drain−to−Source Leakage Current versus Voltage

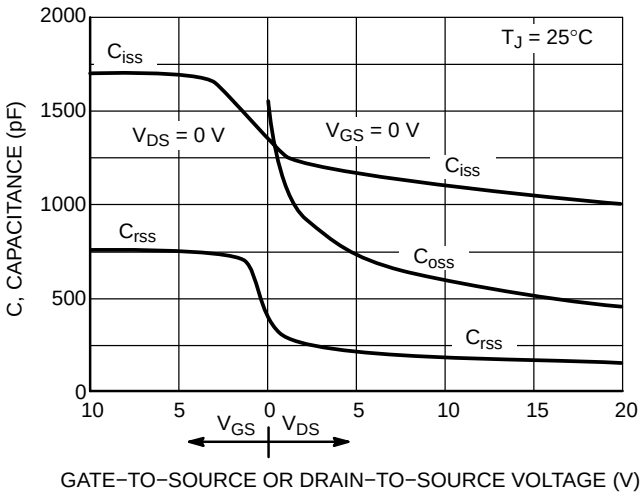


Figure 7. Capacitance Variation

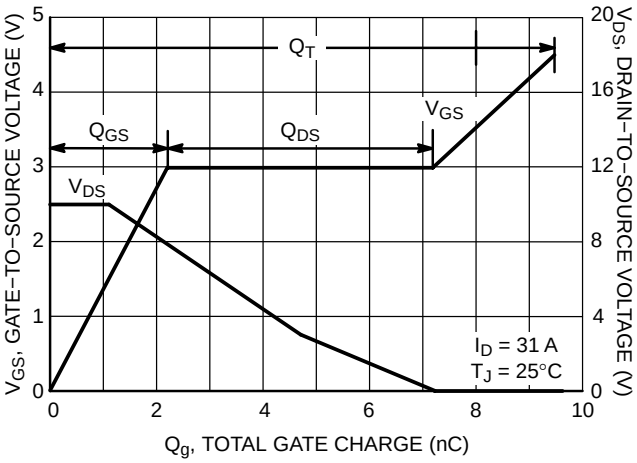


Figure 8. Gate−to−Source and Drain−to−Source Voltage versus Total Charge

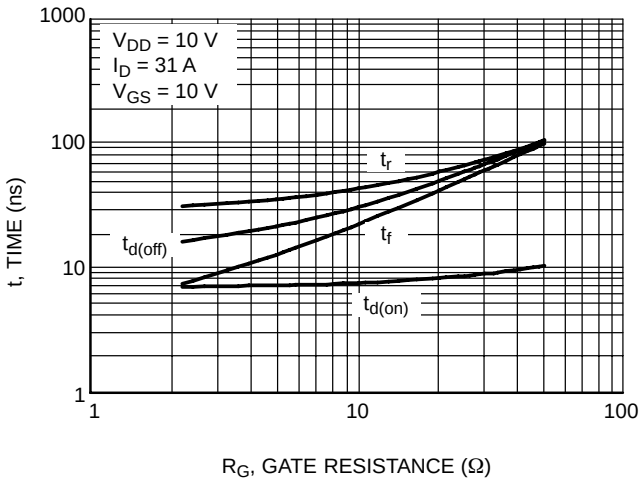


Figure 9. Resistive Switching Time Variation versus Gate Resistance

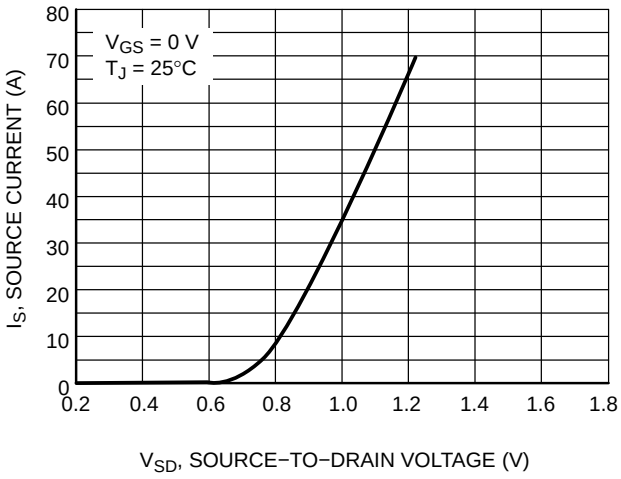


Figure 10. Diode Forward Voltage versus Current

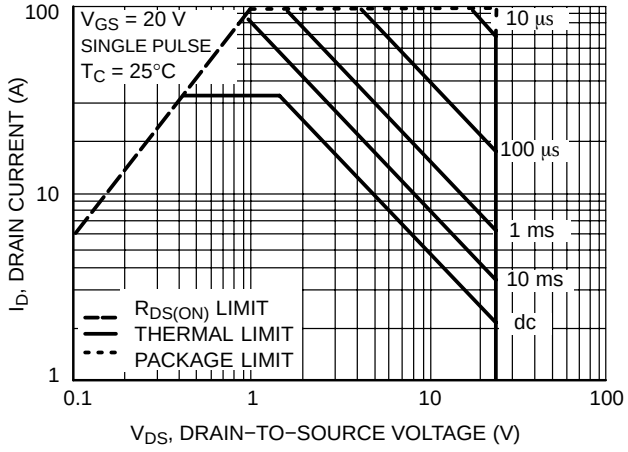


Figure 11. Maximum Rated Forward Biased Safe Operating Area

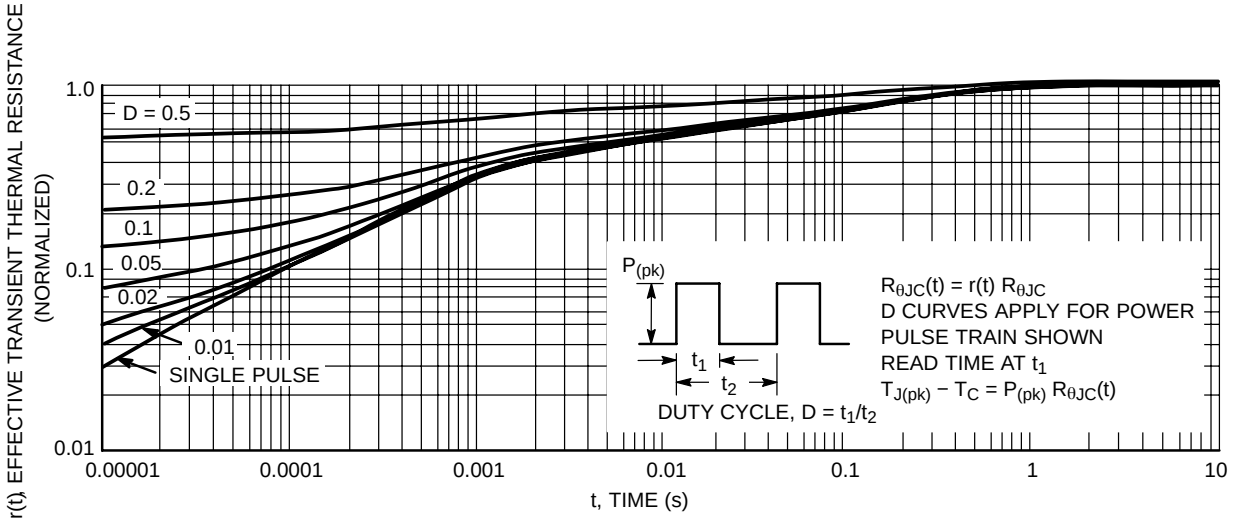


Figure 12. Thermal Response

ORDERING INFORMATION

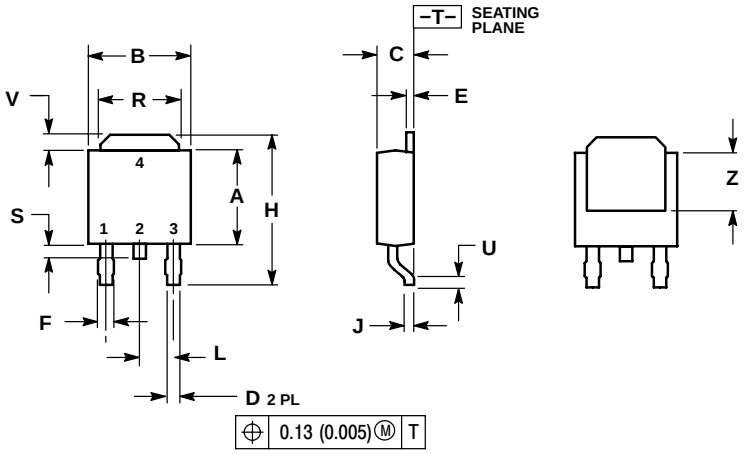
Order Number	Package	Shipping†
NTD60N02R	DPAK−3	75 Units / Rail
NTD60N02RG	DPAK−3 (Pb−Free)	75 Units / Rail
NTD60N02RT4	DPAK−3	2500 / Tape & Reel
NTD60N02RT4G	DPAK−3 (Pb−Free)	2500 / Tape & Reel
NTD60N02R−1	DPAK−3 Straight Lead	75 Units / Rail
NTD60N02R−1G	DPAK−3 Straight Lead (Pb−Free)	75 Units / Rail
NTD60N02R−35	DPAK−3 Straight Lead (3.5 ± 0.15 mm)	75 Units / Rail
NTD60N02R−35G	DPAK−3 Straight Lead (3.5 ± 0.15 mm) (Pb−Free)	75 Units / Rail

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NTD60N02R

PACKAGE DIMENSIONS

DPAK
CASE 369AA−01
ISSUE A

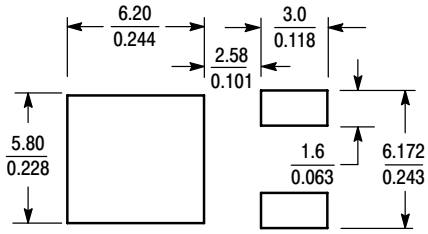


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.025	0.035	0.63	0.89
E	0.018	0.024	0.46	0.61
F	0.030	0.045	0.77	1.14
H	0.386	0.410	9.80	10.40
J	0.018	0.023	0.46	0.58
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.024	0.040	0.60	1.01
U	0.020	−−−	0.51	−−−
V	0.035	0.050	0.89	1.27
Z	0.155	−−−	3.93	−−−

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

SOLDERING FOOTPRINT*



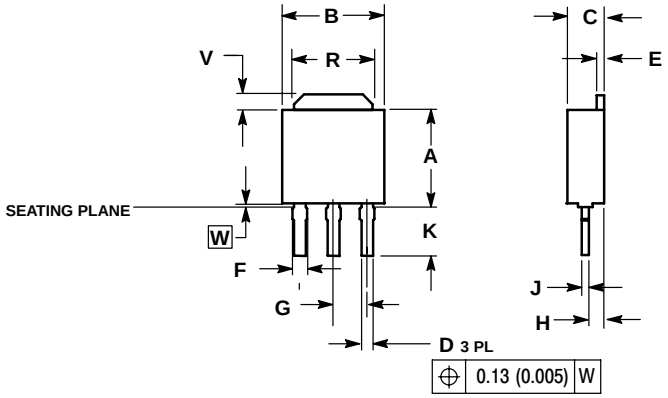
SCALE 3:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NTD60N02R

PACKAGE DIMENSIONS

3 IPAK, STRAIGHT LEAD
CASE 369AC−01
ISSUE O



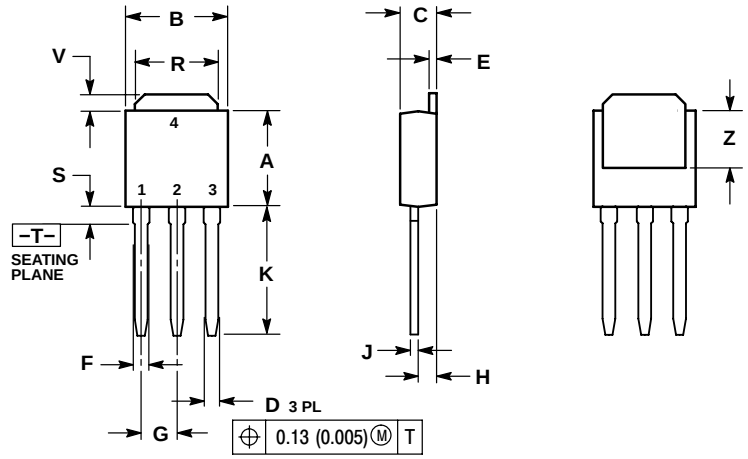
NOTES:
1.. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2.. CONTROLLING DIMENSION: INCH.
3. SEATING PLANE IS ON TOP OF DAMBAR POSITION.
4. DIMENSION A DOES NOT INCLUDE DAMBAR POSITION OR MOLD GATE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.043	0.94	1.09
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.134	0.142	3.40	3.60
R	0.180	0.215	4.57	5.46
V	0.035	0.050	0.89	1.27
W	0.000	0.010	0.000	0.25

NTD60N02R

PACKAGE DIMENSIONS

DPAK
CASE 369D−01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	−−−	3.93	−−−

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

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