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ON Semiconductor
CS9202YDFR8

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sales@integrated-circuit.com

CS9202

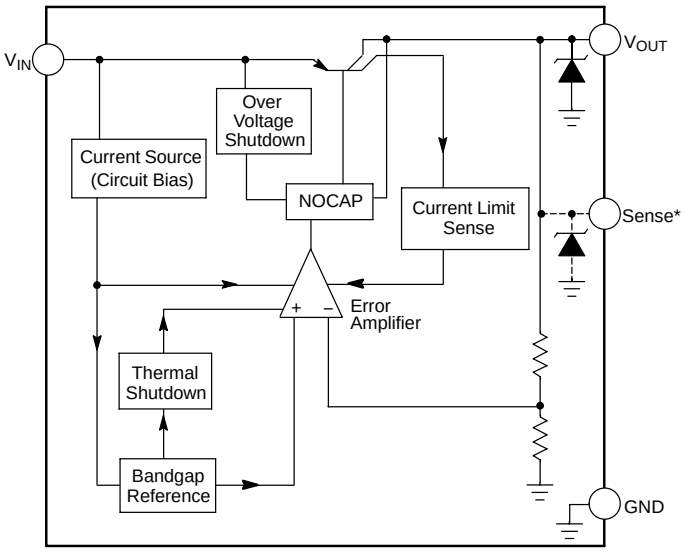
Micropower 3.3 V, 100 mA Linear Regulator with NOCAP™

The CS9202 is a precision 3.3 V, 100 mA voltage regulator with low quiescent current (450 µA typ @ 100 µA load). The 3.3 V output is accurate within ±2% and supplies 100 mA of load current.

The regulator is protected against reverse battery, short circuit, over voltage, and over temperature conditions. The device can withstand 74 V peak transients making it suitable for use in automotive environments. ON's proprietary NOCAP solution is the first technology which allows the output to be stable without the use of an external capacitor. NOCAP is suitable for slow switching or steady loads.

Features

- NOCAP
- Low Quiescent Current (450 µA typ @ 100 µA load)
- 3.3 V, ±2% Output
- 100 mA Output Current Capability
- Fault Protection
  - 74 V Peak Transient Voltage
  - −15 V Reverse Voltage
  - Short Circuit
  - Thermal Shutdown
  - Overvoltage Shutdown
- Internally Fused Leads
- Pb−Free Packages are Available



*Contact factory for optional Sense lead.

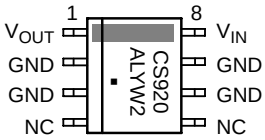
Figure 1. Block Diagram

ON Semiconductor®

http://onsemi.com

SOIC−8
DF SUFFIX
CASE 751

PIN CONNECTIONS AND MARKING DIAGRAM



CS9202 = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
CS9202YDF8	SOIC−8	98 Units/Rail
CS9202YDF8G	SOIC−8 (Pb−Free)	98 Units/Rail
CS9202YDFR8	SOIC−8	2500 Tape & Reel
CS9202YDFR8G	SOIC−8 (Pb−Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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CS9202

MAXIMUM RATINGS

Parameter	Value	Unit
Power Dissipation	Internally Limited	–
Input Voltage (V_{IN}): DC Peak Transient Voltage (60 V Load Dump @ V_{IN} = 14 V)	 −15 to 36 74	 V V
Output Current	Internally Limited	–
ESD Susceptibility (Human Body Model)	4.0	kV
Package Thermal Resistance: Junction−to−Case, $R_{\theta JC}$ Junction−to−Ambient, $R_{\theta JA}$	 25 110	 °C/W °C/W
Junction Temperature	−40 to +150	°C
Storage Temperature	−55 to +150	°C
Lead Temperature Soldering: Reflow (SMD styles only) (Note 1)	230 Peak	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. 60 second maximum above 183°C.

ELECTRICAL CHARACTERISTICS (4.5 V ≤ V_{IN} ≤ 26 V, I_{OUT} = 1.0 mA, −40°C ≤ T_J ≤ 125°C; unless otherwise stated.)

Parameter	Test Conditions	Min	Typ	Max	Unit
OUTPUT STAGE					
Output Voltage, V_{OUT}	9.0 V < V_{IN} < 16 V, 100 μA ≤ I_{OUT} ≤ 100 mA 4.5 V < V_{IN} < 26 V, 100 μA ≤ I_{OUT} ≤ 100 mA	3.234 3.201	3.300 3.300	3.366 3.399	V V
Load Regulation	V_{IN} = 14 V, 100 μA ≤ I_{OUT} ≤ 100 mA	–	5	50	mV
Line Regulation	4.5 V < V < 26 V, I_{OUT} = 1.0 mA	–	5	50	mV
Quiescent Current, (I_Q)	I_{OUT} = 100 μA, V_{IN} = 12 V I_{OUT} ≤ 50 mA I_{OUT} ≤ 100 mA	–	450 4 12	750 6 20	μA mA mA
Ripple Rejection	7.0 V ≤ VI_N ≤ 17 V, I_{OUT} = 100 mA, f = 120 Hz	60	75	–	dB
Current Limit	–	105	200	–	mA
Short Circuit Output Current	V_{OUT} = 0 V	25	125	–	mA
Thermal Shutdown (Note 2)	–	150	180	–	°C
Overvoltage Shutdown	V_{OUT} ≤ 1.0 V	28	32	36	V

2. This parameter is guaranteed by design, but not parametrically tested in production.

PACKAGE LEAD DESCRIPTION

Package Lead Number SOIC−8	Lead Symbol	Function
1	V_{OUT}	3.3 V, ± 2%, 100 mA output.
2, 3, 6, 7	GND	Ground.
4, 5	NC	No connection.
8	V_{IN}	Input voltage.

TYPICAL PERFORMANCE CHARACTERISTICS

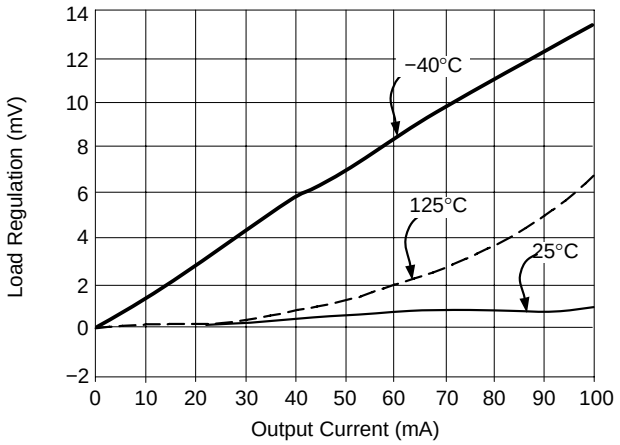


Figure 2. Load Regulation vs. Output Current V_{IN} = 14 V

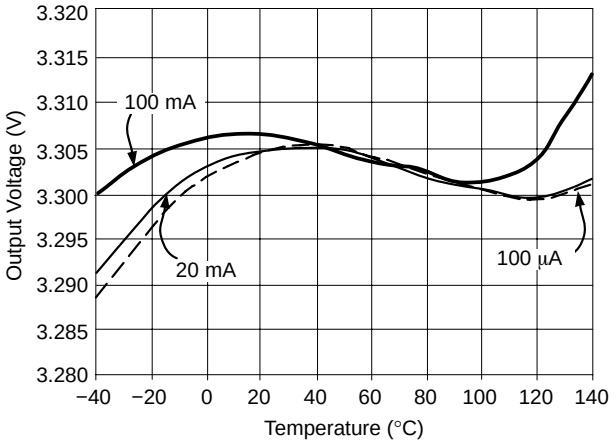


Figure 3. Output Voltage vs. Temperature V_{IN} = 14 V

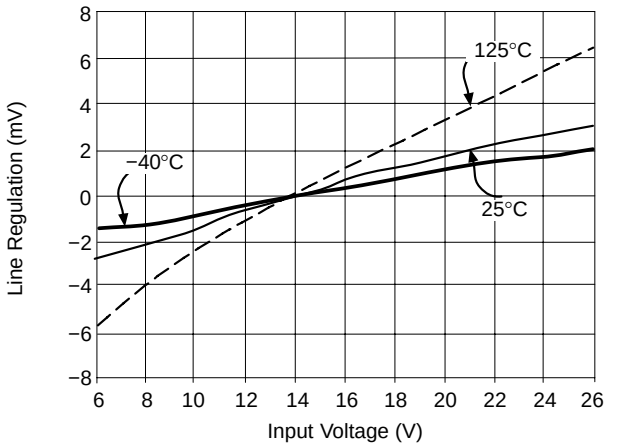


Figure 4. Line Regulation vs. Input Voltage I_{OUT} = 100 μA

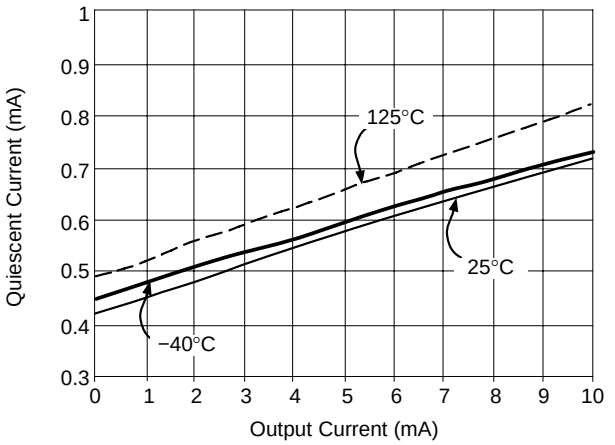


Figure 5. Quiescent Current vs. Output Current (Lightly Loaded) V_{IN} = 14 V

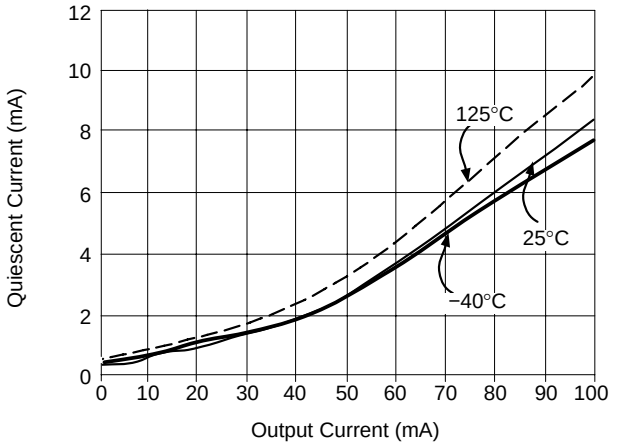


Figure 6. Quiescent Current vs. Output Current V_{IN} = 14 V

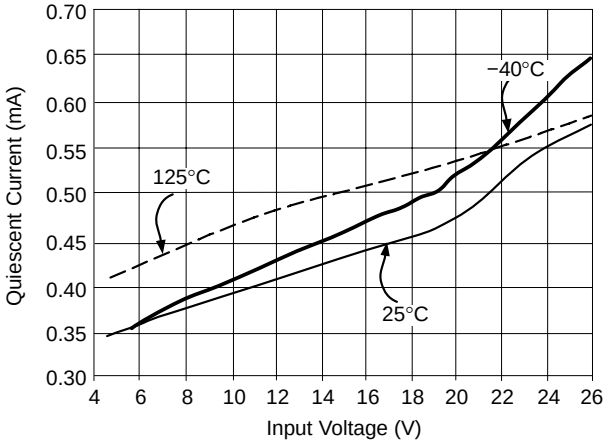


Figure 7. Quiescent Current vs. Input Voltage I_{OUT} = 100 μA

CIRCUIT DESCRIPTION

VOLTAGE REFERENCE AND OUTPUT CIRCUITRY

Output Stage Protection

The output stage is protected against overvoltage, short circuit and thermal runaway conditions (Figure 8).

If the input voltage rises above 32 V (typ), the output shuts down. This response protects the internal circuitry and enables the IC to survive unexpected voltage transients.

Should the junction temperature of the power device exceed 180°C (typ) the power transistor is turned off. Thermal shutdown is an effective means to prevent die overheating since the power transistor is the principle heat source in the IC.

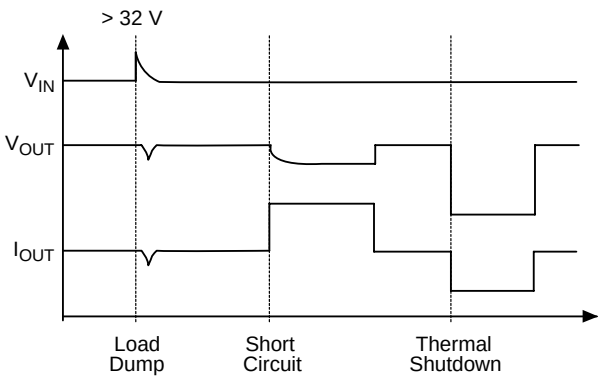
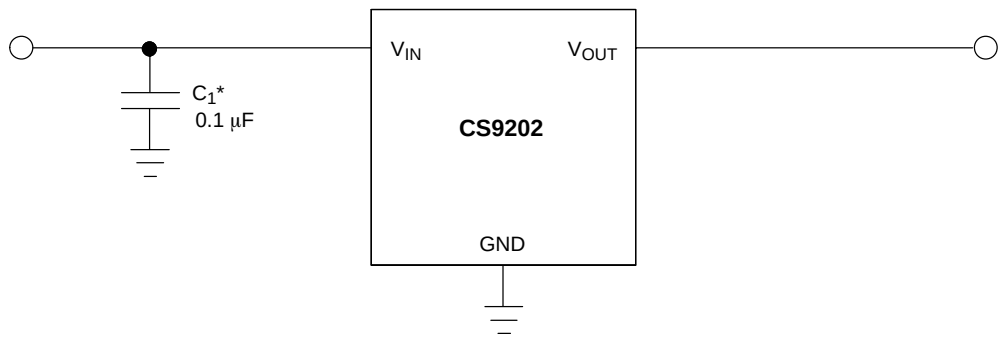


Figure 8. Typical Circuit Waveforms for Output Stage Protection



* C1 is required if regulator is distant from power source filter.

Figure 9. Application and Test Diagram

APPLICATION NOTES

STABILITY CONSIDERATIONS / NOCAP

Normally a linear regulator (with a slow lateral PNP in the control loop) necessitates a large external compensation capacitor at the output of the IC. The external capacitor is also used to curtail offshoot, determine startup delay time and load transient response.

Traditional regulators typically have low unity gain bandwidth, display overshoot and poor ripple rejection. Compensation is also an issue and depends on the external capacitor value, ESR (Equivalent Series Resistance) and board layout parasitics that all can create oscillations if not properly accounted for.

NOCAP is an ON Semiconductor exclusive output stage which internally compensates the regulator over temperature, load and line variations without the need for an expensive external capacitor.

NOCAP is ideally suited for slow switching or steady loads. If the load is characterized by transient current events, an output storage capacitor may be needed. If this is the case, the capacitor should be no larger than 100 nF. With loads that require greater transient suppression, a regulator with a traditional output stage (such as the CS8221) may be better suited for proper operation.

CALCULATING POWER DISSIPATION IN A SINGLE OUTPUT LINEAR REGULATOR

The maximum power dissipation for a single output regulator (Figure 10) is:

$$P_{D(max)} = \{V_{IN(max)} - V_{OUT(min)}\} I_{OUT(max)} + V_{IN(max)} I_Q \quad (1)$$

where:

$V_{IN(max)}$ is the maximum input voltage,
$V_{OUT(min)}$ is the minimum output voltage,
$I_{OUT(max)}$ is the maximum output current for the application, and
I_Q is the quiescent current the regulator consumes at $I_{OUT(max)}$.

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\theta JA}$ can be calculated:

$$R_{\theta JA} = \frac{150^\circ C - T_A}{P_D} \quad (2)$$

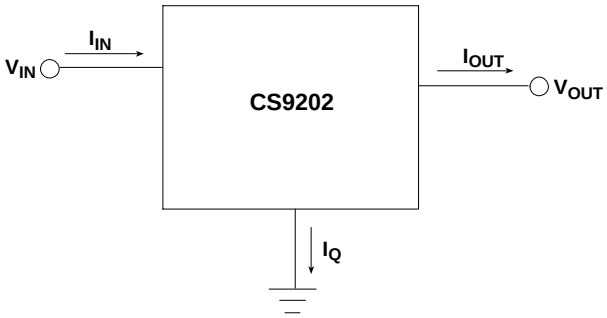


Figure 10. Single output regulator with key performance parameters labeled.

The value of $R_{\theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\theta JA}$'s less than the calculated value in equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

HEAT SINKS

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\theta JA}$:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad (3)$$

where:

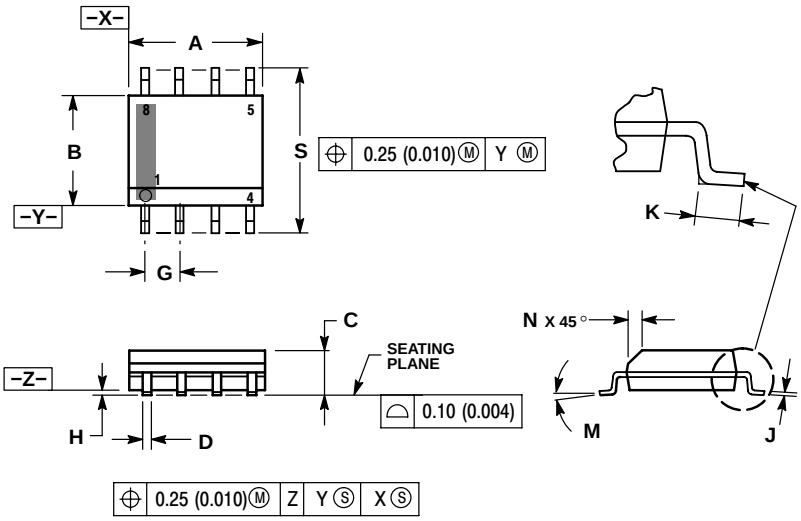
$R_{\theta JC}$ = the junction−to−case thermal resistance,
$R_{\theta CS}$ = the case−to−heatsink thermal resistance, and
$R_{\theta SA}$ = the heatsink−to−ambient thermal resistance.

$R_{\theta JC}$ appears in the package section of the data sheet. Like $R_{\theta JA}$, it too is a function of package type. $R_{\theta CS}$ and $R_{\theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.

CS9202

PACKAGE DIMENSIONS

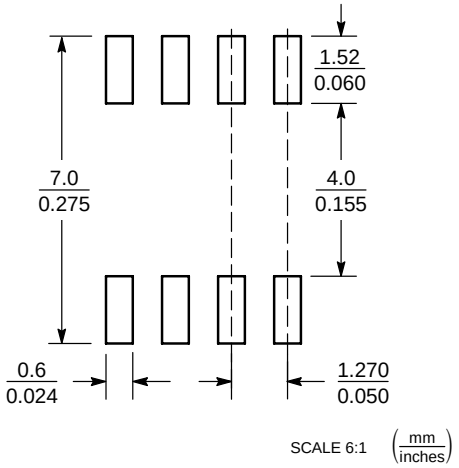
SOIC−8 NB
CASE 751−07
ISSUE AH



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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