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# 74ALVC16374

## Low-Voltage 1.8/2.5/3.3 V 16-Bit D-Type Flip-Flop With 3.6 V-Tolerant Inputs and Outputs (3-State, Non-Inverting)

The 74ALVC16374 is an advanced performance, non-inverting 16-bit D-type flip-flop. It is designed for very high-speed, very low-power operation in 1.8 V, 2.5 V or 3.3 V systems. The ALVC16374 is byte controlled, with each byte functioning identically, but independently. Each byte has separate Output Enable and Clock Pulse inputs. These control pins can be tied together for a full 16-bit operation.

The 74ALVC16374 consists of 16 edge-triggered flip-flops with individual D-type inputs and 3.6 V-tolerant 3-state outputs. The clocks (CPn) and Output Enables ( $\overline{OE}n$ ) are common to all flip-flops within the respective byte. The flip-flops will store the state of individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the  $\overline{OE}$  LOW, the contents of the flip-flops are available at the outputs. When the  $\overline{OE}$  is HIGH, the outputs go to the high impedance state. The  $\overline{OE}$  input level does not affect the operation of the flip-flops.

- Designed for Low Voltage Operation:  $V_{CC} = 1.65\text{--}3.6\text{ V}$
- 3.6 V Tolerant Inputs and Outputs
- High Speed Operation: 3.6 ns max for 3.0 to 3.6 V  
 4.5 ns max for 2.3 to 2.7 V  
 7.8 ns max for 1.65 to 1.95 V
- Static Drive:  $\pm 24\text{ mA}$  Drive at 3.0 V  
 $\pm 12\text{ mA}$  Drive at 2.3 V  
 $\pm 4\text{ mA}$  Drive at 1.65 V
- Supports Live Insertion and Withdrawal
- $I_{OFF}$  Specification Guarantees High Impedance When  $V_{CC} = 0\text{ V}^\dagger$
- Near Zero Static Supply Current in All Three Logic States (40  $\mu\text{A}$ )  
 Substantially Reduces System Power Requirements
- Latchup Performance Exceeds  $\pm 250\text{ mA}$  @ 125°C
- ESD Performance: Human Body Model >2000 V; Machine Model >200 V
- Second Source to Industry Standard 74ALVC16374

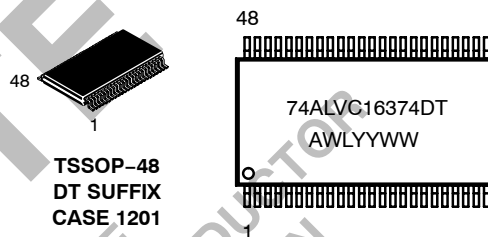
$^\dagger$ To ensure the outputs activate in the 3-state condition, the output enable pins should be connected to  $V_{CC}$  through a pull-up resistor. The value of the resistor is determined by the current sinking capability of the output connected to the  $\overline{OE}$  pin.



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### MARKING DIAGRAM



A = Assembly  
 Location  
 WL = Wafer Lot  
 YY = Year  
 WW = Work Week

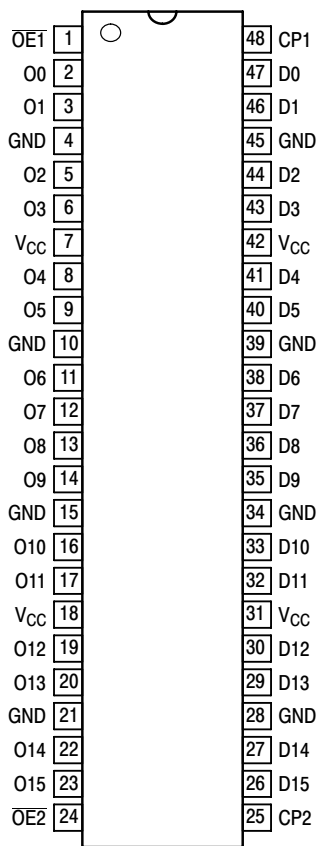
### PIN NAMES

Pins	Function
$\overline{OE}n$	Output Enable Inputs
CPn	Clock Pulse Inputs
D0-D15	Inputs
O0-O15	Outputs

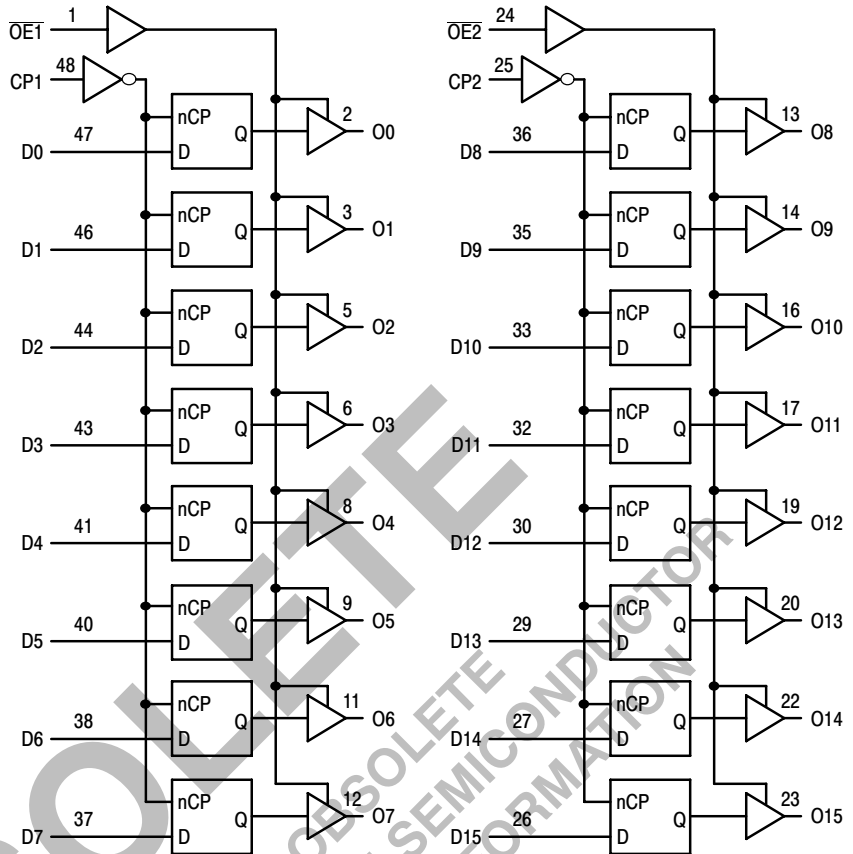
### ORDERING INFORMATION

Device	Package	Shipping
74ALVC16374DTR	TSSOP	2500/Tape & Reel

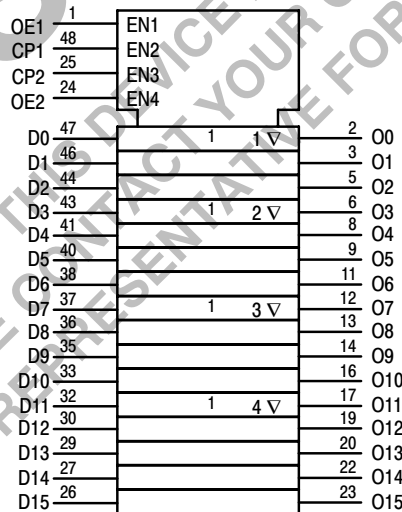
**74ALVC16374**



**Figure 1. 48-Lead Pinout (Top View)**



**Figure 2. Logic Diagram**



**Figure 3. IEC Logic Diagram**

Inputs			Outputs	Inputs			Outputs
CP1	OE1	D0:7	O0:7	CP2	OE2	D8:15	O8:15
↑	L	H	H	↑	L	H	H
↑	L	L	L	↑	L	L	L
X	L	X	O0	X	L	X	O0
X	H	X	Z	X	H	X	Z

H = High Voltage Level; L = Low Voltage Level; Z = High Impedance State; ↑ = Low-to-High Transition; X = High or Low Voltage Level and Transitions Are Acceptable, for I<sub>CC</sub> reasons, DO NOT FLOAT Inputs. O0 = No Change.

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### MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage	-0.5 to +4.6	V
V <sub>I</sub>	DC Input Voltage	-0.5 to +4.6	V
V <sub>O</sub>	DC Output Voltage	-0.5 to +4.6	V
I <sub>IK</sub>	DC Input Diode Current V <sub>I</sub> < GND	-50	mA
I <sub>OK</sub>	DC Output Diode Current V <sub>O</sub> < GND	-50	mA
I <sub>O</sub>	DC Output Sink/Source Current	±50	mA
I <sub>CC</sub>	DC Supply Current per Supply Pin	±100	mA
I <sub>GND</sub>	DC Ground Current per Ground Pin	±100	mA
T <sub>STG</sub>	Storage Temperature Range	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
T <sub>J</sub>	Junction Temperature Under Bias	+150	°C
θ <sub>JA</sub>	Thermal Resistance (Note 2)	90	°C/W
MSL	Moisture Sensitivity	Level 1	
F <sub>R</sub>	Flammability Rating Oxygen Index: 30% - 35%	UL-94-V0 (0.125 in)	
V <sub>ESD</sub>	ESD Withstand Voltage Human Body Model (Note 3) Machine Model (Note 4) Charged Device Model (Note 5)	>2000 >200 N/A	V
I <sub>LATCH-UP</sub>	Latch-Up Performance Above V <sub>CC</sub> and Below GND at 125°C (Note 6)	±250	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. I<sub>O</sub> absolute maximum rating must be observed.
2. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2-ounce copper trace with no air flow.
3. Tested to EIA/JESD22-A114-A.
4. Tested to EIA/JESD22-A115-A.
5. Tested to JESD22-C101-A.
6. Tested to EIA/JESD78.

### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit	
V <sub>CC</sub>	Supply Voltage	Operating	1.65	3.3	3.6	V
		Data Retention Only	1.2	3.3	3.6	
V <sub>I</sub>	Input Voltage (Note 7)	-0.5		3.6	V	
V <sub>O</sub>	Output Voltage (Active State) (3-State)	0		V <sub>CC</sub>	V	
		0		3.6		
T <sub>A</sub>	Operating Free-Air Temperature	-40		+85	°C	
Δt/ΔV	Input Transition Rise or Fall Rate, V <sub>IN</sub> from 0.8 V to 2.0 V, V <sub>CC</sub> = 2.5 V ±0.2 V V <sub>CC</sub> = 3.0 V ±0.3 V	0		20	ns/V	
		0		10		

7. Unused inputs may not be left open. All inputs must be tied to a high-logic voltage level or a low-logic input voltage level.

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### DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T <sub>A</sub> = -40°C to +85°C		Unit
			Min	Max	
V <sub>IH</sub>	HIGH Level Input Voltage (Note 8)	1.65 V ≤ V <sub>CC</sub> < 2.3 V	0.65 × V <sub>CC</sub>		V
		2.3 V ≤ V <sub>CC</sub> ≤ 2.7 V	1.7		
		2.7 V < V <sub>CC</sub> ≤ 3.6 V	2.0		
V <sub>IL</sub>	LOW Level Input Voltage (Note 8)	1.65 V ≤ V <sub>CC</sub> < 2.3 V		0.35 × V <sub>CC</sub>	V
		2.3 V ≤ V <sub>CC</sub> ≤ 2.7 V		0.7	
		2.7 V < V <sub>CC</sub> ≤ 3.6 V		0.8	
V <sub>OH</sub>	HIGH Level Output Voltage	1.65 V ≤ V <sub>CC</sub> ≤ 3.6 V; I <sub>OH</sub> = -100 μA	V <sub>CC</sub> - 0.2		V
		V <sub>CC</sub> = 1.65 V; I <sub>OH</sub> = -4 mA	1.2		
		V <sub>CC</sub> = 2.3 V; I <sub>OH</sub> = -6 mA	2.0		
		V <sub>CC</sub> = 2.3 V; I <sub>OH</sub> = -12 mA	1.7		
		V <sub>CC</sub> = 2.7 V; I <sub>OH</sub> = -12 mA	2.2		
		V <sub>CC</sub> = 3.0 V; I <sub>OH</sub> = -12 mA	2.4		
		V <sub>CC</sub> = 3.0 V; I <sub>OH</sub> = -24 mA	2.0		
V <sub>OL</sub>	LOW Level Output Voltage	1.65 V ≤ V <sub>CC</sub> ≤ 3.6 V; I <sub>OL</sub> = 100 μA		0.2	V
		V <sub>CC</sub> = 1.65 V; I <sub>OL</sub> = 4 mA		0.45	
		V <sub>CC</sub> = 2.3 V; I <sub>OL</sub> = 6 mA		0.4	
		V <sub>CC</sub> = 2.3 V; I <sub>OL</sub> = 12 mA		0.7	
		V <sub>CC</sub> = 2.7 V; I <sub>OL</sub> = 12 mA		0.4	
		V <sub>CC</sub> = 3.0 V; I <sub>OL</sub> = 24 mA		0.55	
I <sub>I</sub>	Input Leakage Current	1.65 V ≤ V <sub>CC</sub> ≤ 3.6 V; 0 V ≤ V <sub>I</sub> ≤ 3.6 V		±5.0	μA
I <sub>OZ</sub>	3-State Output Current	1.65 V ≤ V <sub>CC</sub> ≤ 3.6 V; 0 V ≤ V <sub>O</sub> ≤ 3.6 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>		±10	μA
I <sub>OFF</sub>	Power-Off Leakage Current	V <sub>CC</sub> = 0 V; V <sub>I</sub> or V <sub>O</sub> = 3.6 V		10	μA
I <sub>CC</sub>	Quiescent Supply Current (Note 9)	1.65 V ≤ V <sub>CC</sub> ≤ 3.6 V; V <sub>I</sub> = GND or V <sub>CC</sub>		40	μA
		1.65 V ≤ V <sub>CC</sub> ≤ 3.6 V; 3.6 V ≤ V <sub>I</sub> , V <sub>O</sub> ≤ 3.6 V		±40	μA
ΔI <sub>CC</sub>	Increase in I <sub>CC</sub> per Input	2.7 V < V <sub>CC</sub> ≤ 3.6 V; V <sub>IH</sub> = V <sub>CC</sub> - 0.6 V		750	μA

8. These values of V<sub>I</sub> are used to test DC electrical characteristics only.

9. Outputs disabled or 3-state only.

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### AC CHARACTERISTICS (Note 10; $t_R = t_F = 2.0$ ns; $C_L = 30$ pF; $R_L = 500$ $\Omega$ )

Symbol	Parameter	Waveform	Limits						Unit
			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$						
			$V_{CC} = 3.0$ V to $3.6$ V		$V_{CC} = 2.3$ V to $2.7$ V		$V_{CC} = 1.65$ to $1.95$ V		
			Min	Max	Min	Max	Min	Max	
$f_{max}$	Clock Pulse Frequency	1	250		200		100		MHz
$t_{PLH}$ $t_{PHL}$	Propagation Delay CP to On	1	1.1 1.1	3.6 3.6	1.0 1.0	4.5 4.5	1.5 1.5	7.8 7.8	ns
$t_{PZH}$ $t_{PZL}$	Output Enable Time to High and Low Level	2	1.0 1.0	4.7 4.7	1.0 1.0	6.0 6.0	1.5 1.5	9.2 9.2	ns
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time From High and Low Level	2	1.4 1.4	4.1 4.1	1.2 1.2	5.1 5.1	1.5 1.5	6.8 6.8	ns
$t_s$	Setup Time, High or Low Dn to CP	3	1.1		1.0		2.5		ns
$t_h$	Hold Time, High or Low Dn to CP	3	1.4		1.5		1.0		ns
$t_w$	CP Pulse Width, High	3	3.3		3.3		4.0		ns
$t_{OSHL}$ $t_{OSLH}$	Output-to-Output Skew (Note 11)			0.5 0.5		0.5 0.5		0.75 0.75	ns

10. For  $C_L = 50$  pF, add approximately 300 ps to the AC maximum specification.

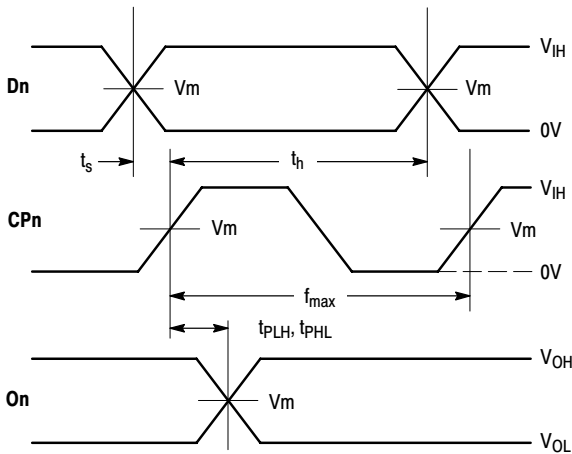
11. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW ( $t_{OSHL}$ ) or LOW-to-HIGH ( $t_{OSLH}$ ); parameter guaranteed by design.

### CAPACITIVE CHARACTERISTICS

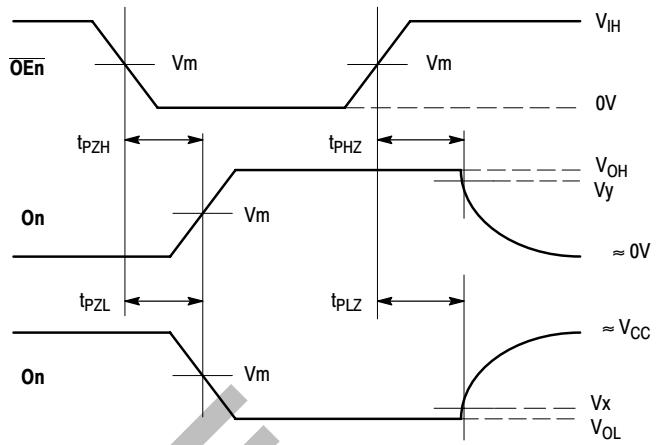
Symbol	Parameter	Condition	Typical	Unit
$C_{IN}$	Input Capacitance	Note 12	6	pF
$C_{OUT}$	Output Capacitance	Note 12	7	pF
$C_{PD}$	Power Dissipation Capacitance	Note 12, 10MHz	20	pF

12.  $V_{CC} = 1.8, 2.5$  or  $3.3$  V;  $V_I = 0$  V or  $V_{CC}$ .

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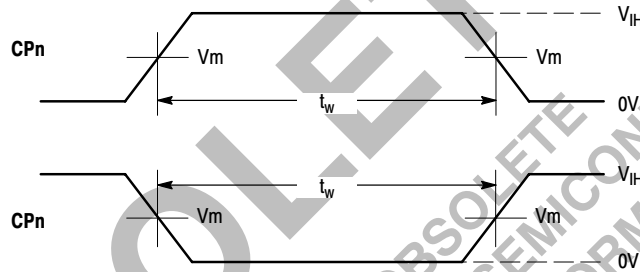


**WAVEFORM 1 - PROPAGATION DELAYS, SETUP AND HOLD TIMES**  
 $t_R = t_F = 2.0\text{ns}$ , 10% to 90%;  $f = 1\text{MHz}$ ;  $t_W = 500\text{ns}$



**WAVEFORM 2 - OUTPUT ENABLE AND DISABLE TIMES**  
 $t_R = t_F = 2.0\text{ns}$ , 10% to 90%;  $f = 1\text{MHz}$ ;  $t_W = 500\text{ns}$

**Figure 4. AC Waveforms**

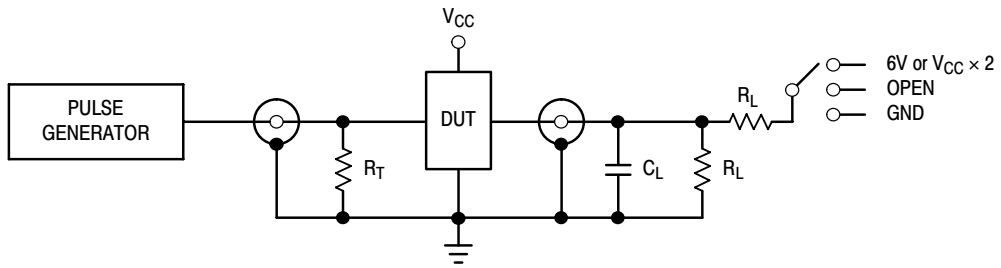


**WAVEFORM 3 - PULSE WIDTH**  
 $t_R = t_F = 2.0\text{ns}$  (or fast as required) from 10% to 90%

**Figure 5. AC Waveforms**

Symbol	V <sub>CC</sub>		
	3.3 V ±0.3 V	2.5 V ±0.2 V	1.8 V ±0.15 V
V <sub>IH</sub>	2.7 V	V <sub>CC</sub>	V <sub>CC</sub>
V <sub>m</sub>	1.5 V	V <sub>CC</sub> /2	V <sub>CC</sub> /2
V <sub>x</sub>	V <sub>OL</sub> + 0.3 V	V <sub>OL</sub> + 0.15 V	V <sub>OL</sub> + 0.15 V
V <sub>y</sub>	V <sub>OH</sub> - 0.3 V	V <sub>OH</sub> - 0.15 V	V <sub>OH</sub> - 0.15 V

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TEST	SWITCH
$t_{PLH}$ , $t_{PHL}$	Open
$t_{PZL}$ , $t_{PLZ}$	6 V at $V_{CC} = 3.3 \pm 0.3$ V; $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2$ V; 1.8 V $\pm 0.15$ V
$t_{PZH}$ , $t_{PHZ}$	GND

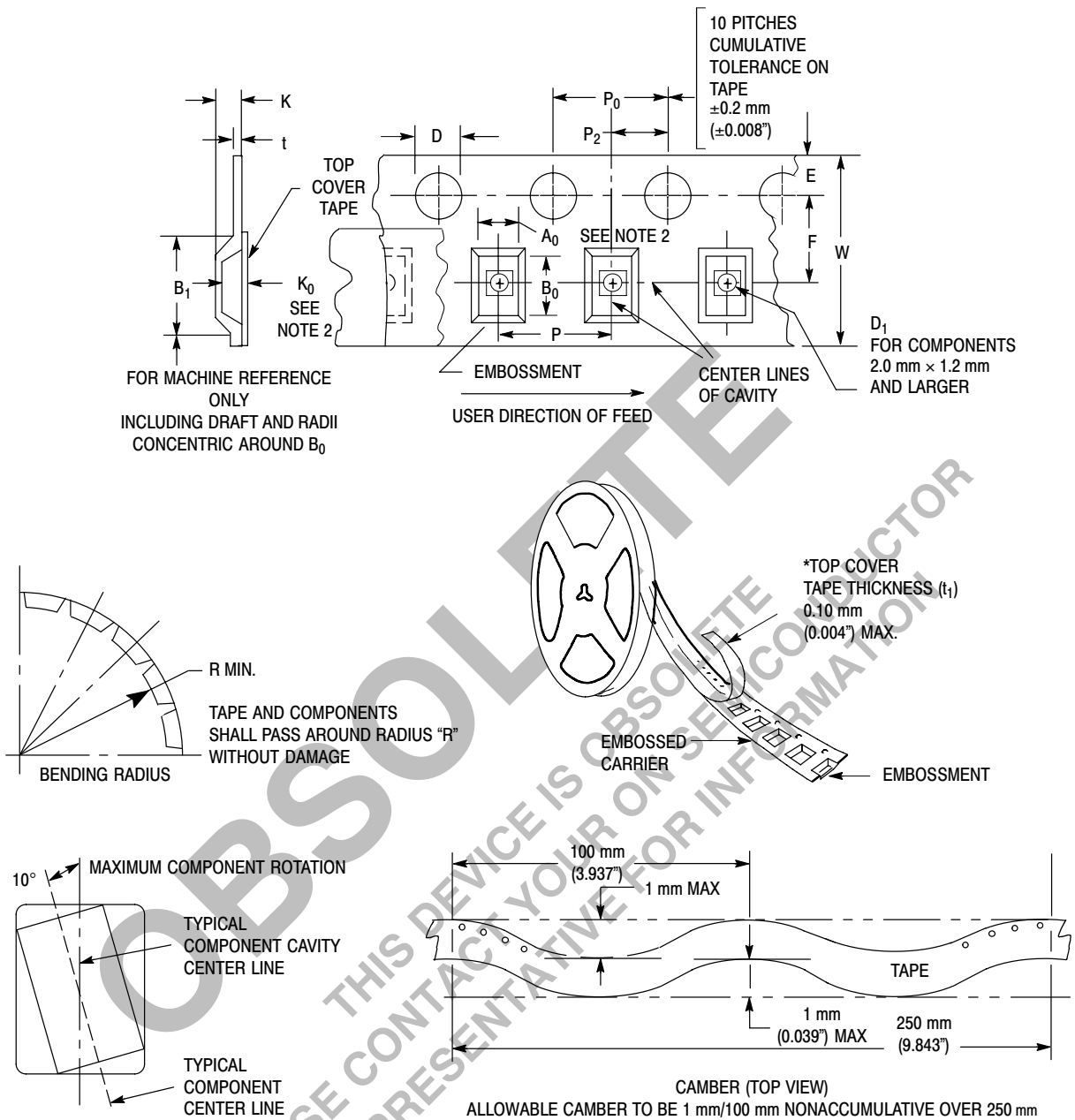
$C_L = 30$  pF or equivalent (Includes jig and probe capacitance)  
 $R_L = 500 \Omega$  or equivalent  
 $R_T = Z_{OUT}$  of pulse generator (typically  $50 \Omega$ )

**Figure 6. Test Circuit**

**OBSOLETE**  
 THIS DEVICE IS OBSOLETE  
 PLEASE CONTACT YOUR ON SEMICONDUCTOR  
 REPRESENTATIVE FOR INFORMATION



**74ALVC16374**



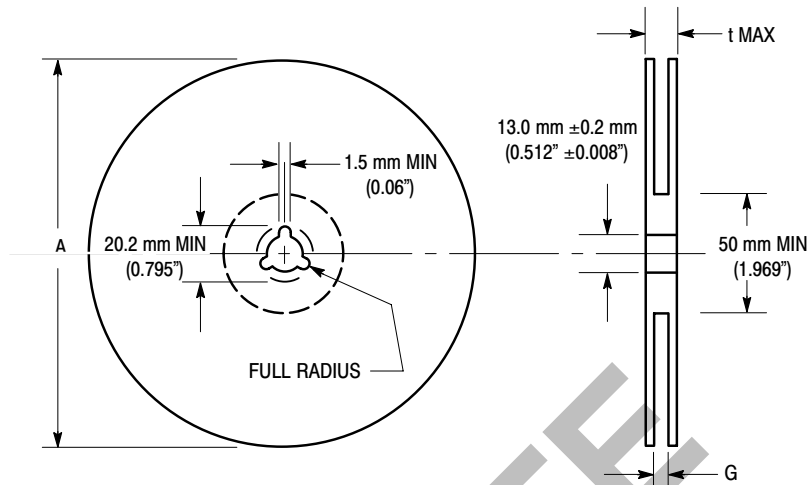
**Figure 7. Carrier Tape Specifications**

**EMBOSSED CARRIER DIMENSIONS** (See Notes 1 and 2)

Tape Size	B <sub>1</sub> Max	D	D <sub>1</sub>	E	F	K	P	P <sub>0</sub>	P <sub>2</sub>	R	T	W
24mm	20.1mm (0.791")	1.5 + 0.1mm -0.0 (0.059 +0.004" -0.0)	1.5mm Min (0.060")	1.75 ±0.1 mm (0.069 ±0.004")	11.5 ±0.10 mm (0.453 ±0.004")	11.9 mm Max (0.468")	16.0 ±0.1 mm (0.63 ±0.004")	4.0 ±0.1 mm (0.157 ±0.004")	2.0 ±0.1 mm (0.079 ±0.004")	30 mm (1.18")	0.6 mm (0.024")	24.3 mm (0.957")

1. Metric Dimensions Govern—English are in parentheses for reference only.
2. A<sub>0</sub>, B<sub>0</sub>, and K<sub>0</sub> are determined by component size. The clearance between the components and the cavity must be within 0.05 mm min to 0.50 mm max. The component cannot rotate more than 10° within the determined cavity.

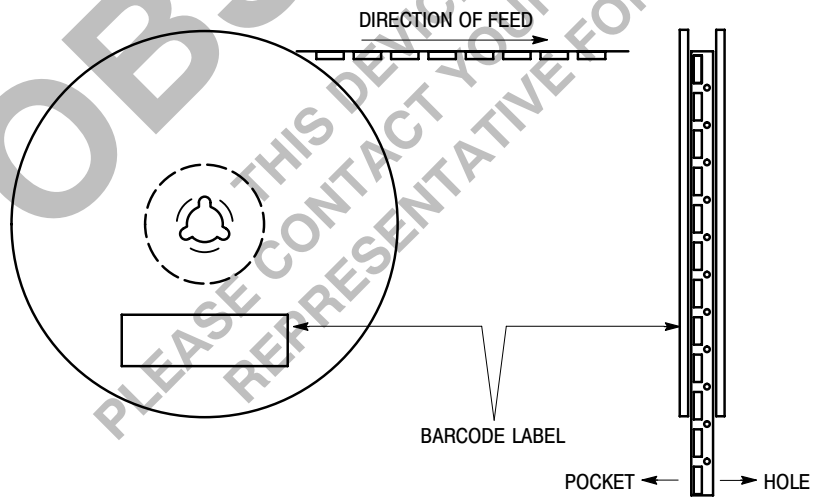
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**Figure 8. Reel Dimensions**

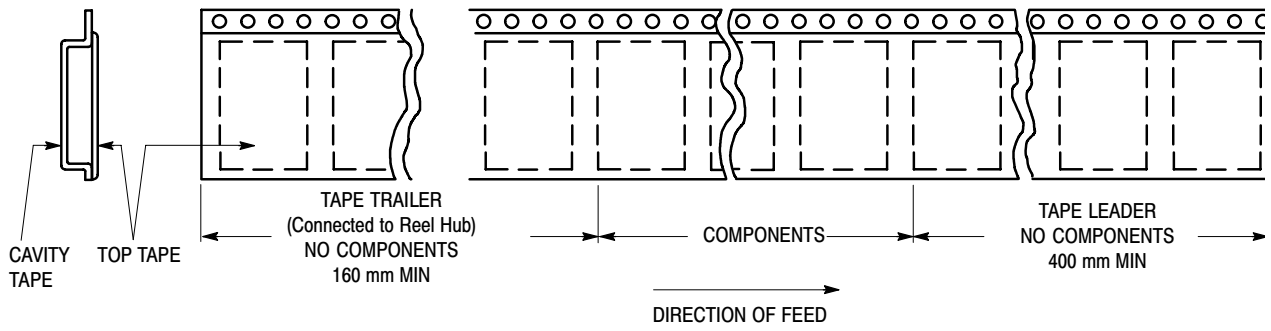
**REEL DIMENSIONS**

Tape Size	A Max	G	t Max
24 mm	360 mm (14.173")	24.4 mm + 2.0 mm, -0.0 (0.961" + 0.078", -0.00)	30.4 mm (1.197")

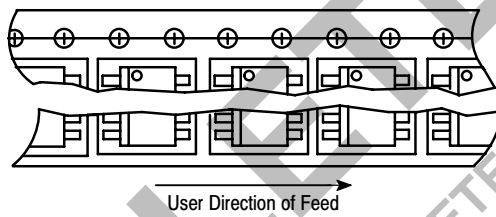


**Figure 9. Reel Winding Direction**

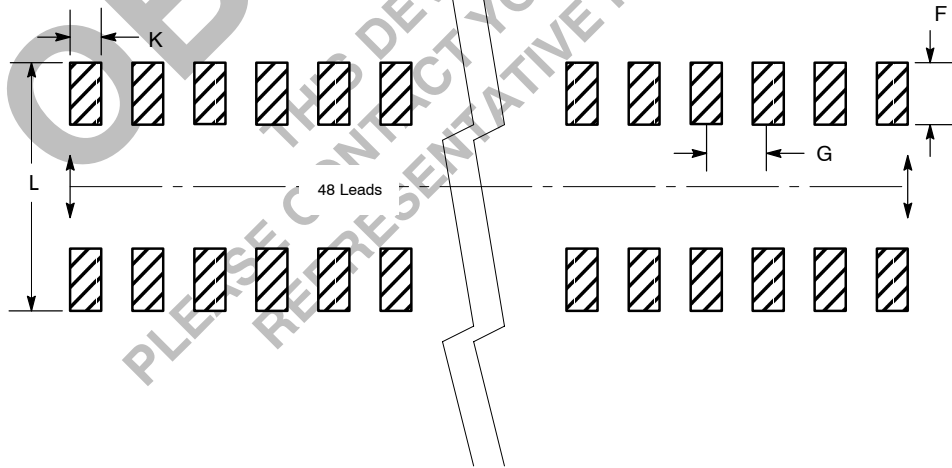
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**Figure 10. Tape Ends for Finished Goods**



**Figure 11. Reel Configuration**

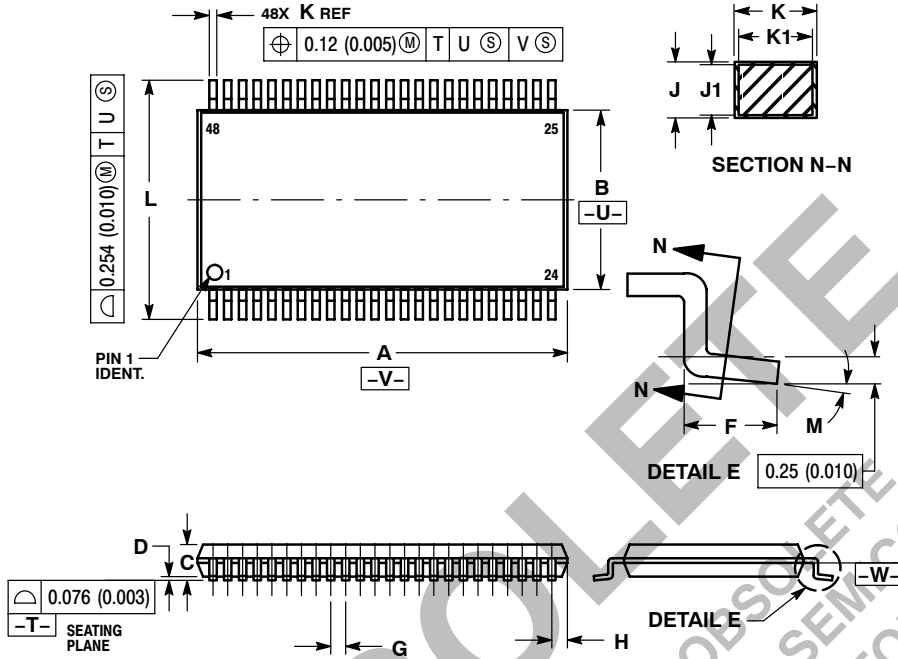


**Figure 12. Package Footprint**

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**PACKAGE DIMENSIONS**

**TSSOP  
DT SUFFIX  
CASE 1201-01  
ISSUE A**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
  4. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
  5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
  6. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.40	12.60	0.488	0.496
B	6.00	6.20	0.236	0.244
C	---	1.10	---	0.043
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.50 BSC		0.0197 BSC	
H	0.37	---	0.015	---
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.17	0.27	0.007	0.011
K1	0.17	0.23	0.007	0.009
L	7.95	8.25	0.313	0.325
M	0°	8°	0°	8°

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