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SCG102A-DFC-A1P6 V1.0

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SCG102A Synchronous Clock Generators

PLL

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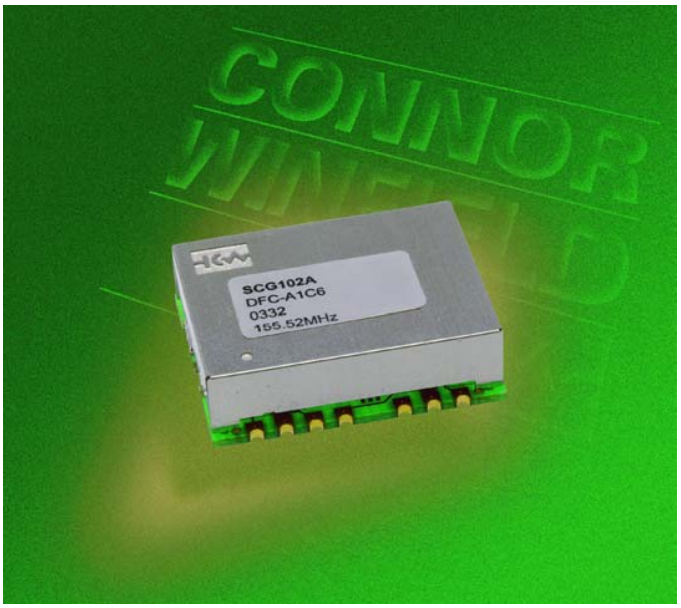

Applications

- SONET / SDH / ATM
- DWDM / FDM
- DSL-PON Interconnects
- FEC (Forward Error Correction)

Features

- 3.3V High Precision PLL
- Accepts 1 of 4 Selectable, Pre-determined Input Frequencies
- 77.76 MHz to 170 MHz Output Frequencies Available.
- Jitter Generation OC-192 Compliant
- 1.0” x 0.80” x 0.285”, Surface Mount

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General Description

The SCG102A provides high precision phase lock loop frequency translation for the telecommunication applications. The SCG102A product generates LVPECL outputs from an intrinsically low jitter, voltage controlled crystal oscillator.

SCG102A is well suited for use in line cards, service termination cards and similar functions to provide reliable reference, phase locked, synchronization for TDM, PDH, SONET and SDH network equipment . The SCG102A provides a jitter filtered, wander following output signal sychronized to a superior Stratum or peer input reference signal.

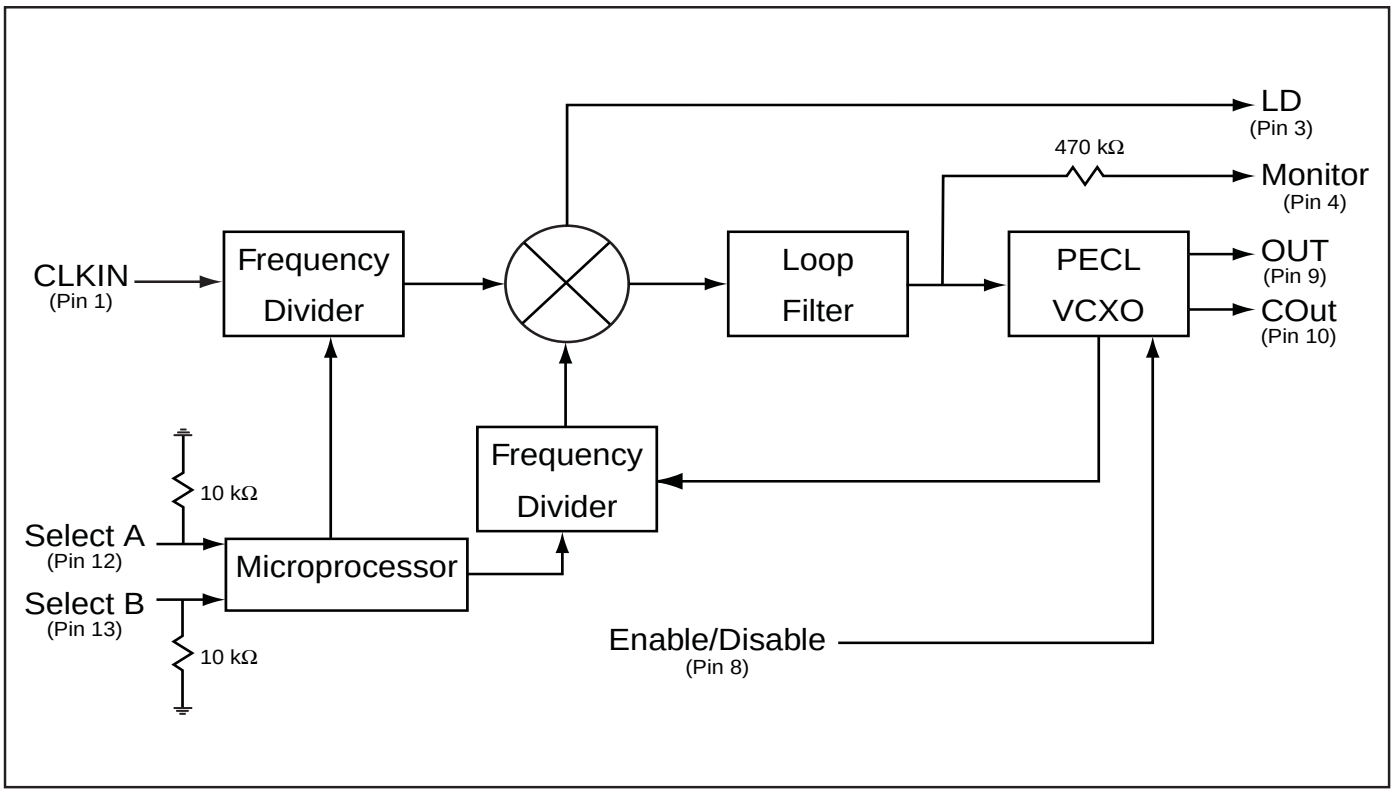
The SCG102A includes a lock detect alarm output. The PLL control voltage is brought out through a 470 kΩ restistor and can be used to determine when the pull range limits are reached.The LVPECL outputs may be put into the tri-state high impedance condition for external testing purposes by asserting a high signal to the Enable/Disable pin.

The SCG102A is a 3.3 Volt component that will typically draw 75mA. The SCG102A is designed to be used in applications that require temperature rating of -40°C - 85° C. The SCG102A package typical dimensions are 1.0" x 0.80" x 0.285" (See fig. 2 for maximum dimensions). Parts are assembled using high temperature solder to withstand surface mount reflow process.

The SCG102A locks to any one of four pred-determined input frequencies selected using the SELECT (A&B) lines (See Table 4). The output may be any single frequency from 77.76 MHz to 170 MHZ.

Functional Block Diagram

Figure 1



Absolute Maximum Rating

Table 1

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
Vcc	Power Supply Voltage	-0.3		5.5	Volts	
V_I	Input Voltage	-0.3		Vcc	Volts	
Ts	Storage Temperature	-55		125	°C	

Specifications

Table 2

Symbol	Parameter		Minimum	Nominal	Maximum	Units	Notes
f_{IN}	Available Input Frequencies	**CMOS** **PECL**	8 k 1 M		100 M 100 M	Hz Hz	
f_{OUT}	Output Frequencies(LVPECL)		77.76 M		170 M	Hz	
Vcc	Supply Voltage		3.135	3.3	3.465	Volts	
I_{CC}	Supply Current			75	100	mA	
CLKIN	Input Logic **A** = CMOS **D** = PECL			CMOS PECL			1
CLKOUT	Output Logic **F** = Comp. PECL			PECL			
V_{OH}			2.275			V	
V_{OL}					1.68	V	
T_R/T_F	Rise/Fall Time			0.5	1	ns	
SYM	Output Symmetry		45		55	%	
BW	Bandwidth			20		Hz	
J_{GEN}	Jitter Generation RMS (12 kHz - 20 MHz)			0.5	1	ps	
J_{TRAN}	Jitter Transfer				0.1	dB	2
APR	Input Frequency Tracking		±50			ppm	
T_{OP}	Operating Temperature	**F** = **C** =	-40 0		85 70	°C °C	

NOTES: 1.0: Only HCMOS and LVHCMOS is supported for input frequencies < 1MHz
2.0: GR-253-CORE, Sec. 5.6.2.1.2

Pin Description

Table 3

Pin #	Connection	Description
1	CLKIN	Input Frequency - The SCG102A AC couples the input , this means that the unit is capable of handling HCMOS, LVCMOS, PECL, LVPECL input signals.
2	GND	Ground
3	Lock Detector	Logic “1” indicates that the unit is locked to the input reference Logic “0” indicates that the reference is lost or out of lock range
4	VCXO Monitor	Control voltage level for the PECL oscillator (Between 0.3V and 3.0V when locked)
5	----	Missing
6	NC	No connection
7	GND	Ground
8	$\overline{\text{Enable}}$/Disable	Logic “0” (or no connect) = Output Enabled Logic “1” = Output Disabled (Tri-Stated)
9	Out	Output
10	COut	Complementary Output
11	NC	No connection
12	Select A	Input Frequency Select Control Pin. See Table 4.
13	Select B	Input Frequency Select Control Pin. See Table 4.
14	NC	No connection
15	GND	Ground
16	V_{CC}	Power supply voltage (3.3 Vdc ± 5%)

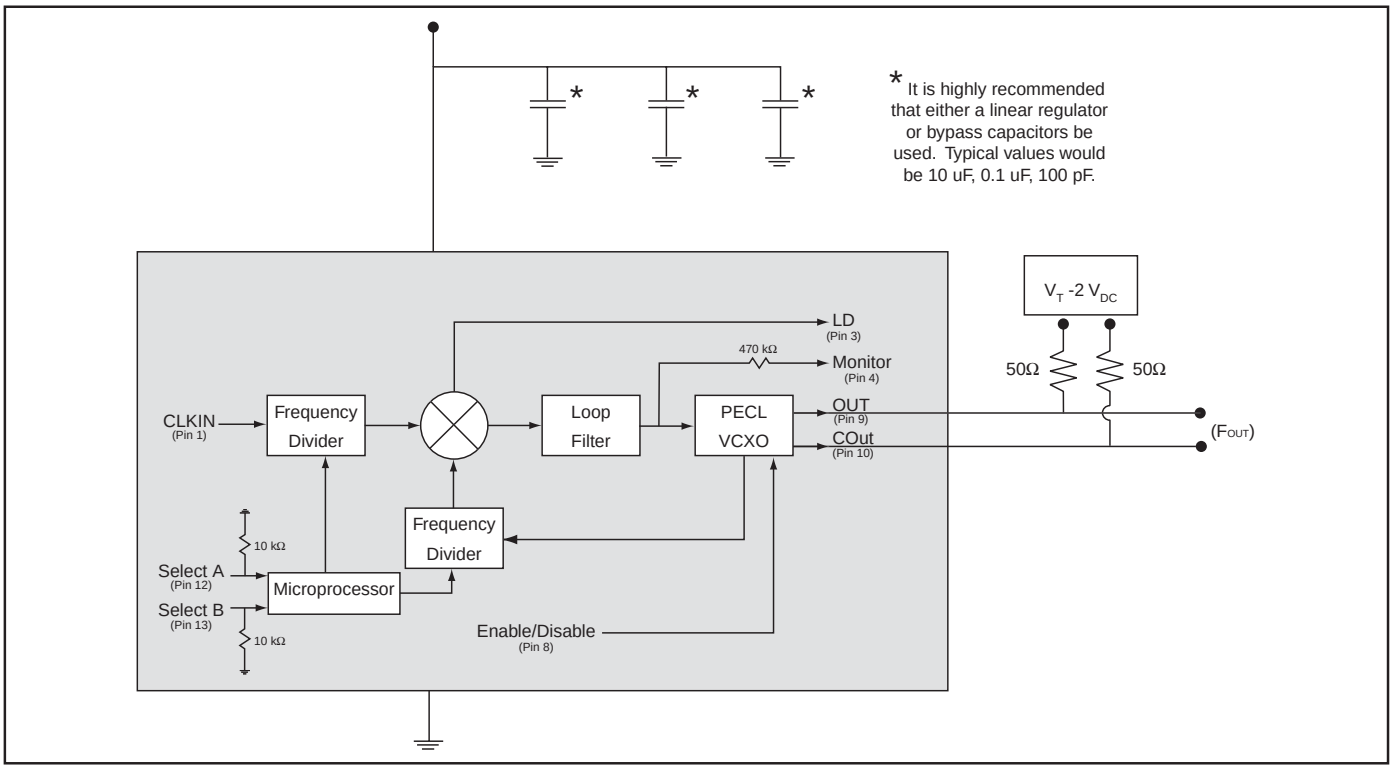
Input Frequency Selection

Table 4

Input Freq	SEL A	SEL B
f_1	0	0
f_2	0	1
f_3	1	0
f_4	1	1

Output Load and Power Supply Filtering Recommendations

Figure 2



Ordering Information

Table 5

10 MHz	A	8.192 MHz	L	51.84 MHz	0
10 kHz	B	13.00 MHz	M	61.44 MHz	1
8 kHz	C	16.384 MHz	N	77.76 MHz	2
16 kHz	D	19.44 MHz	P	82.944 MHz	3
64 kHz	E	20.48 MHz	R	112.00 MHz	4
1.024 MHz	F	26.00 MHz	T	139.264 MHz	5
1.048 MHz	G	27.00 MHz	W	155.52 MHz	6
1.544 MHz	H	38.88 MHz	X	166.6286 MHz	7
2.048 MHz	J	44.736 MHz	Y	114.0 MHz	8
4.096 MHz	K	53.10468 MHz	Z	125.0 MHz	9

For any model, the reference inputs and output frequency must have a common frequency of 2.667Hz (8kHz/3)
Ex 1: A Model with reference inputs of 8kHz, 16kHz, 32kHz and 64kHz with a Output frequency of 155.52MHz is valid due to the common frequency of 2.667kHz. Contact CW regarding models that do not have a input/output common frequency of 2.667kHz.

SCG102A- D F F - A 1 P 6

Supply Voltage
D = 3.3 V_{DC} ± 5%

Output Type
F = Comp. PECL

Temperature Range
C = 0°C to 70°C
F = -40°C to 85°C

Output Frequency (2 to 9)
See chart above. If a custom frequency is desired, enter **S** followed by the frequency. Contact a sales representative for the availabilty of custom frequencies.

Input Frequency (A to 9)
See chart above.
If more than one frequency is desired, enter **S** and list all desired frequencies. Contact a sales representative for the availabilty of custom frequencies.

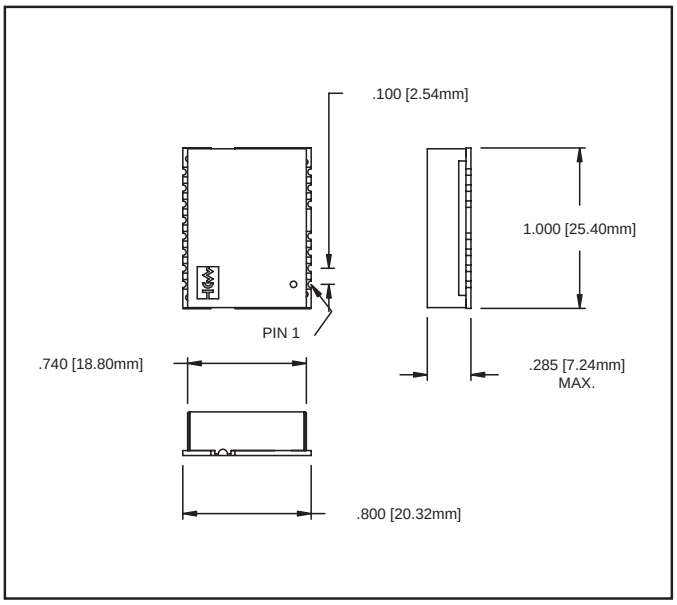
Number of Input Frequencies
1 = 1 Input Frequency
2 = 2 Input Frequencies
3 = 3 Input Frequencies
4 = 4 Input Frequencies

Input Logic
A = CMOS
D = PECL

Sample Part Number Examples:
SCG-102A- DFF-A1C2
SCG-102A- DFF-A4S2, S = 8 kHz, 16.384 MHz, 19.44 MHz, 38.88 MHz
SCG-102A-DFF-D1ZS, S = Custom Frequency

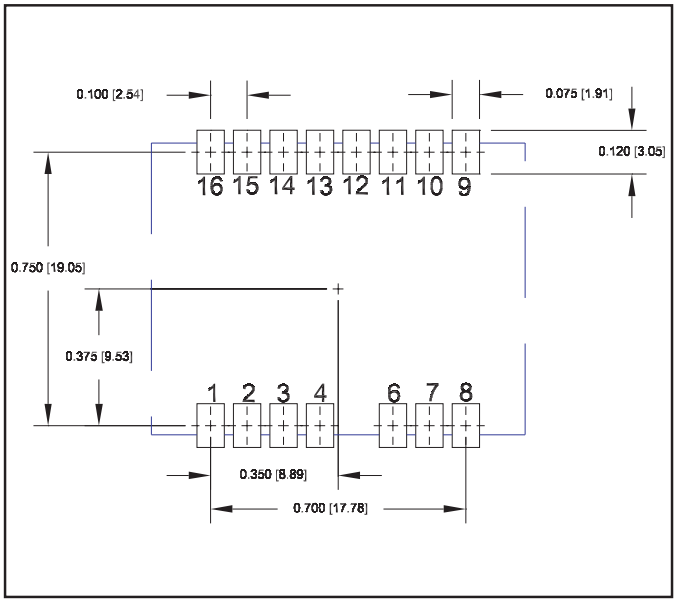
Package Dimensions

Figure 3



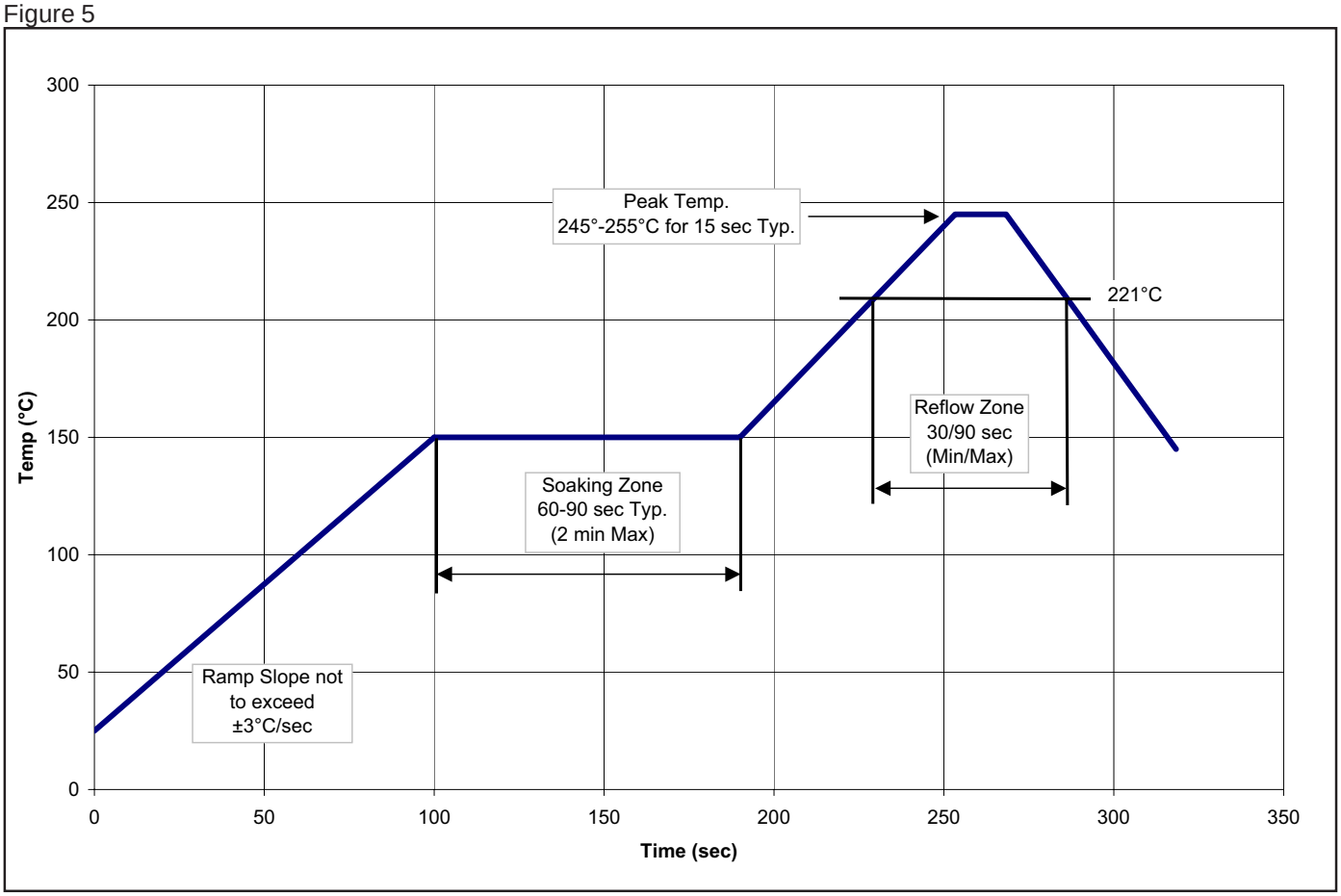
Recommended Footprint Dimensions

Figure 4



Solder Profile

Figure 5



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Revision	Revision Date	Note
00	4/11/07	Final Release