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LX1670CD](#)

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THE INFINITE POWER OF INNOVATION

LIN Doc #: 1670

**LX1670**

**5-BIT PROGRAMMABLE VOLTAGE REFERENCE**

**PRODUCTION DATA SHEET**

**DESCRIPTION**

The LX1670 is a complete precision reference and voltage monitor circuit for the Intel Pentium® Pro Processor and other high-end microprocessor supplies. It is designed for use in conjunction with the LX1660/1661 PWM controller. The LX1670 reads a 5-bit voltage identification (VID) code from

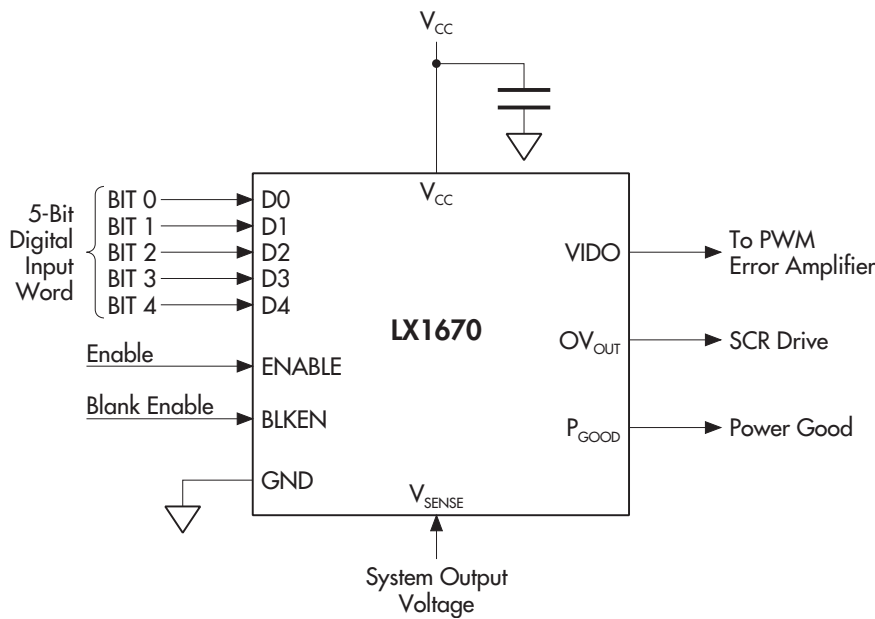
the microprocessor and sets the output voltage reference to be used by the LX1660/61 controller. Together, they convert +5 or 12V input power to an adjustable output ranging from 1.8VDC to 3.5VDC in 100mV steps (50mV steps below 2.1V) with 1% DC system accuracy.

**KEY FEATURES**

- ❑ 1% TOTAL OUTPUT ERROR
- ❑ POWER GOOD, UV, 0V COMPARATORS
- ❑ 0V COMPARATOR HAS SCR DRIVE
- ❑ UNDER-VOLTAGE LOCKOUT CAPABILITY
- ❑ 5-BIT INPUT FOR ADVANCED PENTIUM PRO PROCESSOR APPLICATIONS (5<sup>TH</sup> BIT IS FOR AUTOMATIC GAIN AND OFFSET SCALING)
- ❑ IMPLEMENTS 1% DC ACCURATE CONTROL SYSTEM
- ❑ 14-PIN NARROW BODY SOIC PACKAGE

**PRODUCT HIGHLIGHT**

TYPICAL APPLICATION OF THE LX1670



**APPLICATIONS**

- PENTIUM II & PENTIUM PRO VOLTAGE REGULATOR MODULES
- PROGRAMMABLE POWER SUPPLIES
- VOLTAGE REFERENCE
- ADVANCED MICROPROCESSOR SUPPLIES

**PACKAGE ORDER INFO**

T <sub>A</sub> (°C)	D Plastic SOIC 14-pin
0 to 70	LX1670CD

Note: All surface-mount packages are available in Tape & Reel. Append the letter "T" to part number. (i.e. LX1670CDT)

**FOR FURTHER INFORMATION CALL (714) 898-8121**

11861 WESTERN AVENUE, GARDEN GROVE, CA. 92841

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#### ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ( $V_{CC}$ )	-0.3V to +15V
$P_{GOOD}$ , D0-D3, D4, ENABLE, BLKEN	-0.3V to $V_{CC}+0.3$
VIDO, $OV_{OUT}$ , $V_{SENSE}$	-0.3V to +5V
$OV_{OUT}$	-35mA
VIDO	-5mA
Operating Junction Temperature	
Plastic (D Package)	150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 Seconds)	300°C

Note 1. Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal. Pin numbers refer to DIL packages only.

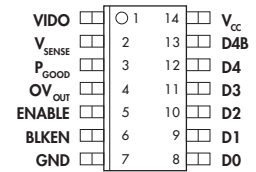
#### THERMAL DATA

##### D PACKAGE:

<b>THERMAL RESISTANCE-JUNCTION TO AMBIENT, <math>\theta_{JA}</math></b>	<b>120°C/W</b>
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Junction Temperature Calculation:  $T_J = T_A + (P_D \times \theta_{JA})$ .  
The  $\theta_{JA}$  numbers are guidelines for the thermal performance of the device/pc-board system.  
All of the above assume no ambient airflow

#### PACKAGE PIN OUTS



**D PACKAGE**  
(Top View)

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#### ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for LX1670C with  $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$  ;  $10.8\text{V} < V_{CC} < 13.2\text{V}$ , D0-D3 = Open, D4 = Open, ENABLE = 1, BLKEN = 1. Nominal conditions:  $V_{CC} = 12.0\text{V}$ ,  $T = 25^{\circ}\text{C}$ . Currents flowing into chip are positive. Current maximums are currents with the highest possible value.)

Parameter	Symbol	Test Conditions	LX1670			Units
			Min.	Typ.	Max.	
<b>Power Supply Current and Power Section</b>						
Positive 12V Supply Current	$I_{CC}$	All outputs, inputs unloaded		5		mA
<b>Digital-to-Analog Converter Section</b> (Includes DAC, I-V Converter and output scaling amplifier. $R_{LOAD} > 1k$ , $C_{LOAD} < 100pF$ )						
Voltage Set Point Accuracy	VSPA	D0-D3 = X, D4 = Open, $2.00 \leq VIDO \leq 3.50\text{V}$	-1.0		1.0	%
		D0-D3 = X, D4 = GND, $1.80 \leq VIDO \leq 2.05\text{V}$	-1.5		1.5	%
LSB	VSTP	D4 = Open		100		mV
		D4 = GND		50		mV
Coding		Binary, D0 = LSB, D3 = MSB				
<b>Under-Voltage Lockout Section</b>						
Power-up Reset	$V_{RES}$	$I_{GOOD} = 5\text{mA}$			1.0	V
Threshold	UVLOT	$V_{CC} = 5\text{V}$ , Supply ramping down	4.27	4.37	4.47	V
Hysteresis	UVLOH	$V_{CC} = 5\text{V}$ , Supply ramping up		50		mV
<b>Under/Over-Voltage Comparator Section</b>						
Percent of VIDO Threshold	UOVTH		$\pm 5.5$	$\pm 7$	$\pm 8.5$	%
$P_{GOOD}$ Low Voltage	VLG	$I_{GOOD} = 5\text{mA}$		0.2	0.4	V
<b>Over-Voltage Protection Comparator Section</b>						
Percent of VIDO Threshold	OVP TH		10	15	20	%
OVP Sourcing Current	IOVP	OVP = 3.0V	-20			mA
OVP Output Low	VLOVP	IOVP = 100 $\mu\text{A}$			100	mV
<b>TTL Inputs Section</b>						
Input Low Voltage	$V_{IL}$				0.8	V
Input High Voltage	$V_{IH}$		2.0			V
Input Low Current	$I_{IL}$	$V_{IL} = 0.8\text{V}$		-10		$\mu\text{A}$
Input High Current	$I_{IH}$	$V_{IH} = 2.0\text{V}$		0		$\mu\text{A}$
<b>Open Drain Inputs Section</b> (D0-D3, D4)						
Input Low Current	$I_{IL}$	Pin Ground		-37.5		$\mu\text{A}$
Input High Voltage	$V_{IH}$	Pin Open		2.0		V

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#### FUNCTION TABLES

Table 1 - Input vs. Output Functions

V <sub>CC</sub>	D4-D0	ENABLE	BLKEN	V <sub>SENSE</sub> (V <sub>S</sub> )	V <sub>IDO</sub> (V <sub>O</sub> )	P <sub>GOOD</sub>	OV <sub>OUT</sub>
V <sub>CC</sub> < 1.0	X	X	X	X	Undefined	Undefined	Undefined
1.0 < V <sub>CC</sub> < UVLOT	X	X	X	X	LOW	LOW	LOW
V <sub>CC</sub> > UVLOT	X	0	X	X	LOW	LOW	LOW
V <sub>CC</sub> > UVLOT	V <sub>IDO</sub> Table	1	0	V <sub>S</sub> < 0.93V <sub>O</sub>	V <sub>IDO</sub> Table 3	LOW	LOW
V <sub>CC</sub> > UVLOT	V <sub>IDO</sub> Table	1	0	0.93V <sub>O</sub> < V <sub>S</sub> < 1.07V <sub>O</sub>	V <sub>IDO</sub> Table 3	HIGH	LOW
V <sub>CC</sub> > UVLOT	V <sub>IDO</sub> Table	1	0	1.07V <sub>O</sub> < V <sub>S</sub> < 1.15V <sub>O</sub>	V <sub>IDO</sub> Table 3	LOW	LOW
V <sub>CC</sub> > UVLOT	V <sub>IDO</sub> Table	1	0	V <sub>S</sub> > 1.15V <sub>O</sub>	V <sub>IDO</sub> Table 3	LOW	HIGH
V <sub>CC</sub> > UVLOT	V <sub>IDO</sub> Table	1	1	V <sub>S</sub> < 0.93V <sub>O</sub>	V <sub>IDO</sub> Table 2	LOW	LOW
V <sub>CC</sub> > UVLOT	V <sub>IDO</sub> Table	1	1	0.93V <sub>O</sub> < V <sub>S</sub> < 1.07V <sub>O</sub>	V <sub>IDO</sub> Table 2	HIGH	LOW
V <sub>CC</sub> > UVLOT	V <sub>IDO</sub> Table	1	1	1.07V <sub>O</sub> < V <sub>S</sub> < 1.15V <sub>O</sub>	V <sub>IDO</sub> Table 2	LOW	LOW
V <sub>CC</sub> > UVLOT	V <sub>IDO</sub> Table	1	1	V <sub>S</sub> > 1.15V <sub>O</sub>	V <sub>IDO</sub> Table 2	LOW	HIGH

Table 2 - V<sub>IDO</sub> Output (BLKEN pulled high or left open)

D4	D3	D2	D1	D0	V <sub>IDO</sub>	D4	D3	D2	D1	D0	V <sub>IDO</sub>
0	1	1	1	1	0	1	1	1	1	1	2.00
0	1	1	1	0	0	1	1	1	1	0	2.10
0	1	1	0	1	0	1	1	1	0	1	2.20
0	1	1	0	0	0	1	1	1	0	0	2.30
0	1	0	1	1	0	1	1	0	1	1	2.40
0	1	0	1	0	0	1	1	0	1	0	2.50
0	1	0	0	1	0	1	1	0	0	1	2.60
0	1	0	0	0	0	1	1	0	0	0	2.70
0	0	1	1	1	0	1	0	1	1	1	2.80
0	0	1	1	0	0	1	0	1	1	0	2.90
0	0	1	0	1	1.800	1	0	1	0	1	3.00
0	0	1	0	0	1.850	1	0	1	0	0	3.10
0	0	0	1	1	1.900	1	0	0	1	1	3.20
0	0	0	1	0	1.950	1	0	0	1	0	3.30
0	0	0	0	1	2.000	1	0	0	0	1	3.40
0	0	0	0	0	2.050	1	0	0	0	0	3.50

Table 3 - V<sub>IDO</sub> Output (BLKEN pulled low)

D4	D3	D2	D1	D0	V <sub>IDO</sub>	D4	D3	D2	D1	D0	V <sub>IDO</sub>
0	1	1	1	1	1.300	1	1	1	1	1	2.00
0	1	1	1	0	1.350	1	1	1	1	0	2.10
0	1	1	0	1	1.400	1	1	1	0	1	2.20
0	1	1	0	0	1.450	1	1	1	0	0	2.30
0	1	0	1	1	1.500	1	1	0	1	1	2.40
0	1	0	1	0	1.550	1	1	0	1	0	2.50
0	1	0	0	1	1.600	1	1	0	0	1	2.60
0	1	0	0	0	1.650	1	1	0	0	0	2.70
0	0	1	1	1	1.700	1	0	1	1	1	2.80
0	0	1	1	0	1.750	1	0	1	1	0	2.90
0	0	1	0	1	1.800	1	0	1	0	1	3.00
0	0	1	0	0	1.850	1	0	1	0	0	3.10
0	0	0	1	1	1.900	1	0	0	1	1	3.20
0	0	0	1	0	1.950	1	0	0	1	0	3.30
0	0	0	0	1	2.000	1	0	0	0	1	3.40
0	0	0	0	0	2.050	1	0	0	0	0	3.50

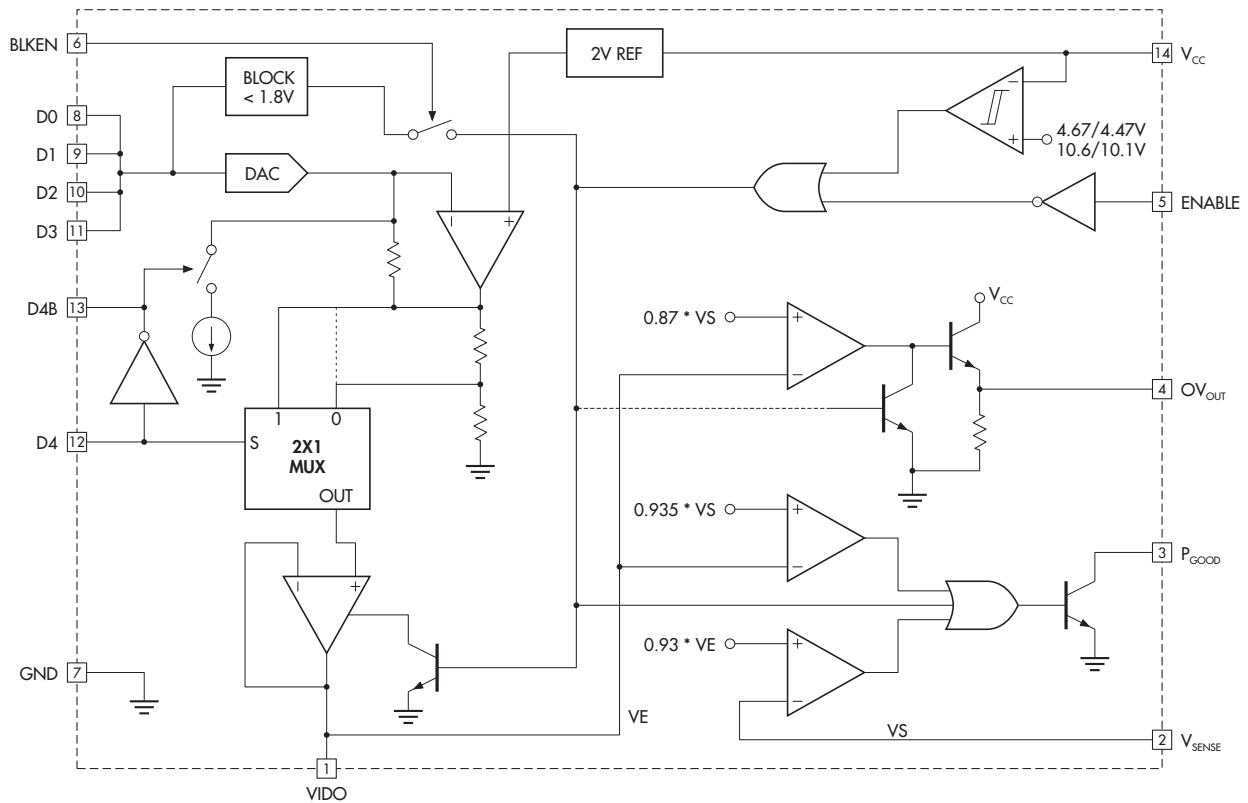
Table 4 - Mode Control

D4	ENABLE	BLKEN	Mode	State
X	0	X	Disable	V <sub>IDO</sub> is pulled low through 10k
0	1	0	Low	V <sub>IDO</sub> is scaled. Output 1.3V to 2.05V Normal Output 2.0 to 3.5V
1	1	0	Normal	
0	1	1	Low	V <sub>IDO</sub> is scaled. Output 1.8V to 2.05V Normal output 2.0 to 3.5V
1	1	1	Normal	

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**BLOCK DIAGRAM**



**FUNCTIONAL PIN DESCRIPTION**

Pin Name	Pin #	Description
V <sub>IDO</sub>	1	Output reference voltage used by PWM controller to set system voltage.
V <sub>SENSE</sub>	2	Connected directly to system output voltage.
P <sub>GOOD</sub>	3	Open collector output pulls low when the processor's supply is not good.
OV <sub>OUT</sub>	4	SCR Driver goes high when processor supply is over voltage.
ENABLE	5	TTL compatible chip enable. Internally pulled high.
BLKEN	6	Enables or disables blocking of codes with voltage blow 1.8V for CPU protection. Internally pulled high.
GND	7	Analog ground return.
D0	8	LSB DAC logic control. Internally pulled high.
D1	9	2nd LSB DAC logic control. Internally pulled high.
D2	10	3rd LSB DAC logic control. Internally pulled high.
D3	11	MSB DAC logic control. Internally pulled high.
D4	12	Scales V <sub>IDO</sub> output when low. Internally pulled high.
D4B	13	Inverting output of D4.
V <sub>CC</sub>	14	Analog power supply.

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#### THEORY OF OPERATION

##### UNDER-VOLTAGE LOCKOUT

This function keeps order to the IC until the power supply voltage reaches 85% of its nominal value. The output voltage is pulled low and P<sub>GOOD</sub> and OV<sub>OUT</sub> are pulled low. Once the power supply voltage crosses 85%, the output voltage, VIDO, is released, and P<sub>GOOD</sub> continues to be pulled low. When V<sub>SENSE</sub> (the microprocessor's power supply) is within ±7% of VIDO, P<sub>GOOD</sub> is released. The comparator has hysteresis to prevent transient oscillation.

##### 4-BIT DAC and 5th-BIT SCALER

This function generates a precise voltage from a binary, 5-bit digital word VID [0:4]. It uses a 4-bit, binary weighted current DAC, driving a precise current to voltage converter. This voltage is then op-amp buffered and sent out. The scaling is accomplished by multiplexing the buffer op-amp. The resulting transfer function is:

$$\text{VIDO (D0,D1,D2,D3)} = (2.00 + 0.1 * (1*D0 + 2*D1 + 4*D2 + 8*D3)) \quad \text{for } D4 = 1$$

$$\text{VIDO (D0,D1,D2,D3)} = (2.00 + 0.6 + 0.1 * (1*D0 + 2*D1 + 4*D2 + 8*D3)) * 0.5 \quad \text{for } D4 = 0$$

for the code VIDO < 1.8V will be blocked and VIDO = 0.

The zero-scale output voltage, full-scale output voltage and the scale factor are all trimmed on-chip using fusible links.

##### OVER- / UNDER-VOLTAGE COMPARATORS

This function generates an open collector Power Good signal when V<sub>SENSE</sub> is within ±7% of VIDO.

##### OVER-VOLTAGE PROTECTION

This function generates an OV<sub>OUT</sub> voltage signal when V<sub>SENSE</sub> is 15% higher than VIDO. This voltage can be used to drive an external SCR.

##### CHIP ENABLE

This function disables the chip when low. VIDO, P<sub>GOOD</sub> and OV<sub>OUT</sub> are all pulled low. When ENABLE is high, the chip's state is then determined by the other functions.

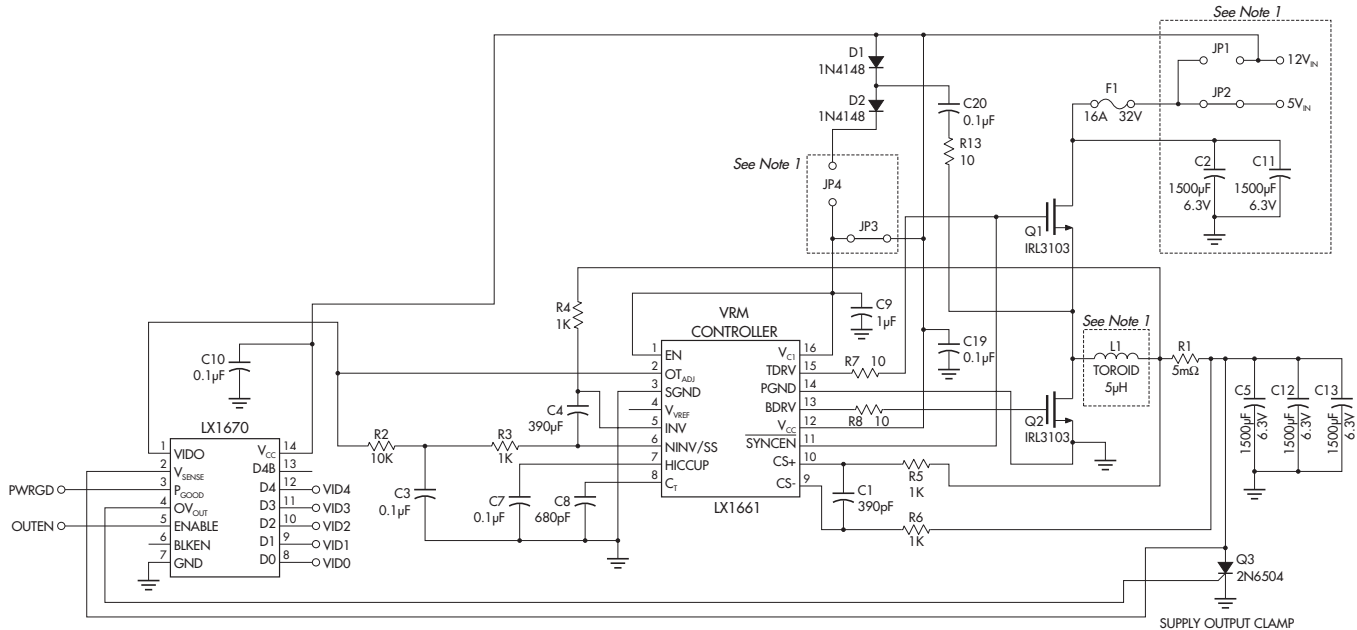
##### BLANK ENABLE

This function will disable VIDO for codes with voltages below 1.80V when this pin is high. When pulled low, this function will allow VIDO to accept codes for voltages of 1.30 to 3.50V.

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**APPLICATION INFORMATION**



Note 1. Setup shown is for 5V application. For 12V input change the following:

- Close JP1 and JP4
- Open JP2 and JP3
- For C2 and C11, use 16V/850µF capacitors instead
- Inductor L1 = 10µH

**FIGURE 1** — LX1660/61 CONTROLLER USED WITH THE LX1670 PROGRAMMABLE REFERENCE/DAC CHIP FOR PENTIUM PRO PROCESSOR OR PENTIUM II PROCESSOR APPLICATIONS. GUARANTEED TO MEET INTEL SPECIFICATIONS.

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