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SN65LVDS16DRFT

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2.5-V/3.3-V OSCILLATOR GAIN STAGE/BUFFERS

FEATURES

- **Low-Voltage PECL Input and Low-Voltage PECL or LVDS Outputs**
- **Clock Rates to 2 GHz**
  - **140-ps Output Transition Times**
  - **0.11 ps Typical Intrinsic Phase Jitter**
  - **Less than 630 ps Propagation Delay Times**
- **2.5-V or 3.3-V Supply Operation**
- **2-mm × 2-mm Small-Outline No-Lead Package**

APPLICATIONS

- **PECL-to-LVDS Translation**
- **Clock Signal Amplification**

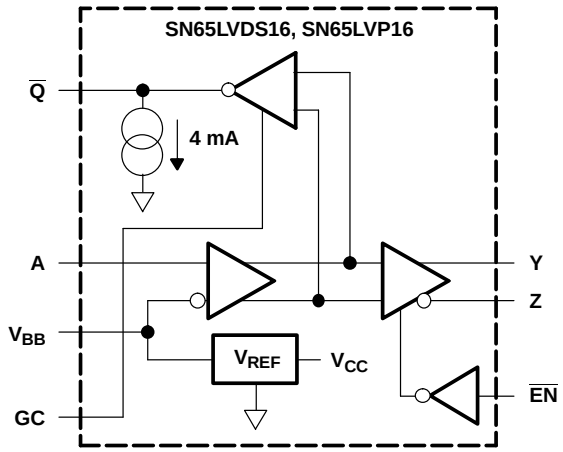
DESCRIPTION

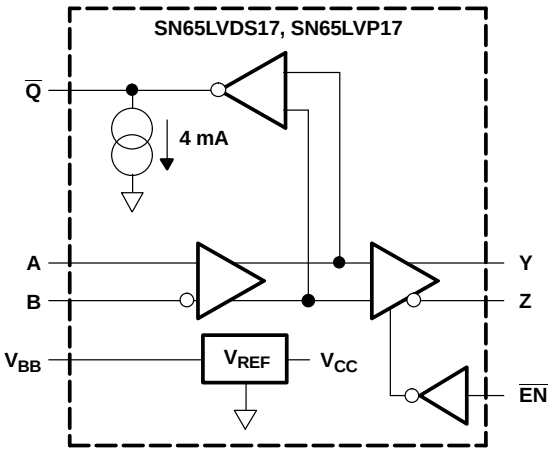
These four devices are high-frequency oscillator gain stages supporting both LVPECL or LVDS on the high gain outputs in 3.3-V or 2.5-V systems. Additionally, provides the option of both single-ended input (PECL levels on the SN65LVx16) and fully differential inputs on the SN65LVx17.

The SN65LVx16 provides the user a Gain Control (GC) for controlling the $\overline{Q}$ output from 300 mV to 860 mV either by leaving it open (NC), grounded, or tied to V_{CC}. (When left open, the $\overline{Q}$ output defaults to 575 mV.) The $\overline{Q}$ on the SN65LVx17 defaults to 575 mV as well.

Both devices provide a voltage reference (V_{BB}) of typically 1.35 V below V_{CC} for use in receiving single-ended PECL input signals. When not used, V_{BB} should be unconnected or open.

All devices are characterized for operation from –40°C to 85°C.





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE OPTIONS(1)

INPUT	OUTPUT	GAIN CONTROL	BASE PART NUMBER	PART MARKING
Single-ended	LVDS	Yes	SN65LVDS16	EL
Single-ended	LVPECL	Yes	SN65LVP16	EK
Differential	LVDS	No	SN65LVDS17	EN
Differential	LVPECL	No	SN65LVP17	EM

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		UNIT
V_{CC}	Supply voltage(2)	–0.5 V to 4 V
V_I	Input voltage	–0.5 V to V_{CC} + 0.5 V
V_O	Output voltage	–0.5 V to V_{CC} + 0.5 V
I_O	V_{BB} output current	±0.5 mA
	HBM electrostatic discharge(3)	±3 kV
	CDM electrostatic discharge(4)	±1500 V
	Continuous power dissipation	See Power Dissipation Ratings Table

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground see Figure 1).
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A-7
(4) Tested in accordance with JEDEC Standard 22, Test Method C101

DISSIPATION RATINGS

PACKAGE	CIRCUIT BOARD MODEL	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$(1)	$T_A = 85°C$ POWER RATING
DRF	Low-K(2)	403 mW	4.0 mW/°C	161 mW
	High-K(3)	834 mW	8.3 mW/°C	333 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.
(2) In accordance with the Low-K thermal metric definitions of EIA/JESD51-3.
(3) In accordance with the High-K thermal metric definitions of EIA/JESD51-7.

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	VALUE	UNIT
θ_{JB}	Junction-to-board thermal resistance			93.3	°C/W
θ_{JC}	Junction-to-case thermal resistance			101.7	
P_D	Device power dissipation	Typical	V_{CC} = 3.3 V, T_A = 25°C, 2 GHz, LVDS	132	mW
			V_{CC} = 3.3 V, T_A = 25°C, 2 GHz, LVPECL	83	
		Maximum	V_{CC} = 3.6 V, T_A = 85°C, 2 GHz, LVDS	173	
			V_{CC} = 3.6 V, T_A = 85°C, 2 GHz, LVPECL	108	

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2.375	2.5 or 3.3	3.6	V
V_{IC}	Common-mode input voltage $(V_{IA} + V_{IB})/2$	SN65LVDS17 or SN65LVP17	1.2		$V_{CC} – (V_{ID}/2)$	V
$\|V_{ID}\|$	Differential input voltage magnitude $\|V_{IA} - V_{IB}\|$	SN65LVDS17 or SN65LVP17	0.08		1	V
V_{IH}	High-level input voltage to $\overline{EN}$	$\overline{EN}$	2		V_{CC}	V
		SN65LVDS16 or SN65LVP16	V_{CC}– 1.17		V_{CC}– 0.44	
V_{IL}	Low-level input voltage to $\overline{EN}$	$\overline{EN}$	0		0.8	V
		SN65LVDS16 or SN65LVP16	V_{CC}– 2.25		V_{CC}– 1.52	
I_O	Output current to V_{BB}		–400 (1)		400	µA
R_L	Differential load resistance,		90		132	Ω
T_A	Operating free-air temperature		-40		85	°C

(1) The algebraic convention, where the least positive (more negative) value is designated minimum, is used in this data sheet.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP (1)	MAX	UNIT
I_{CC}	Supply current	R_L = 100 Ω, $\overline{EN}$ at 0 V, Other inputs open		40	48	mA
		Outputs unloaded, $\overline{EN}$ at 0 V, Other inputs open		25	30	
V_{BB}	Reference voltage (2)	I_{BB} = –400 µA	V_{CC}– 1.44	V_{CC}– 1.35	V_{CC}– 1.25	V
I_{IH}	High-level input current, $\overline{EN}$	V_I = 2 V	–20		20	µA
I_{IAH} or I_{IBH}	High-level input current, A or B	$V_I = V_{CC}$	–20		20	
I_{IL}	Low-level input current, $\overline{EN}$	V_I = 0.8 V	–20		20	
I_{IAL} or I_{IBL}	Low-level input current, A or B	V_I = GND	–20		20	
SN65LVDS16/17 Y AND Z OUTPUT CHARACTERISTICS						
$\|V_{OD}\|$	Differential output voltage magnitude, $\|V_{OY} – V_{OZ}\|$	See Figure 1 and Figure 2	247	340	454	mV
$\Delta\|V_{OD}\|$	Change in differential output voltage magnitude between logic states				50	
$V_{OC(SS)}$	Steady-state common-mode output voltage (see Figure 3)		1.125		1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states	See Figure 3	-50		50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage			50	100	
I_{OYZ} or I_{OZZ}	High-impedance output current	$\overline{EN}$ at V_{CC}, V_O = 0 V or V_{CC}	–1		1	µA
I_{OYS} or I_{OZS}	Short-circuit output current	$\overline{EN}$ at 0 V, V_{OY} or V_{OZ} = 0 V	–62		62	mA
$I_{OS(D)}$	Differential short-circuit output current, $\|I_{OY} – I_{OZ}\|$	$\overline{EN}$ at 0 V, $V_{OY} = V_{OZ}$	–12		12	

(1) Typical values are at room temperature and with a V_{CC} of 3.3 V.
(2) Single-ended input operation is limited to $V_{CC} \geq$ 3.0 V.

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
SN65LVP16/17 Y AND Z OUTPUT CHARACTERISTICS						
V_{OYH} or V_{OZH}	High-level output voltage	3.3 V; 50 Ω from Y and Z to V_{CC}– 2 V	V_{CC}– 1.05		V_{CC}– 0.82	V
V_{OYL} or V_{OZL}	Low-level output voltage	3.3 V; 50 Ω from Y and Z to V_{CC}– 2 V	V_{CC}– 1.83		V_{CC}– 1.57	V
V_{OYL} or V_{OZL}	Low-level output voltage	2.5 V; 50 Ω from Y and Z to V_{CC}– 2 V	V_{CC}– 1.88		V_{CC}– 1.57	V
$\lvert V_{OD}\rvert$	Differential output voltage magnitude, $\lvert V_{OH} - V_{OL}\rvert$		0.6	0.8	1	V
I_{OYZ} or I_{OZZ}	High-impedance output current	$\overline{EN}$ at V_{CC}, V_O = 0 V or V_{CC}	–1		1	µA
$\overline{Q}$ OUTPUT CHARACTERISTICS (see Figure 1)						
V_{OH}	High-level output voltage	No load	V_{CC}– 0.94			V
V_{OL}	Low-level output voltage	GC Tied to GND, No load	V_{CC}– 1.22			V
		GC Open, No load	V_{CC}– 1.52			
		GC Tied to V_{CC}, No load	V_{CC}– 1.82			
$V_{O(pp)}$	Peak-to-peak output voltage	GC Tied to GND		300		mV
		GC Open		575		
		GC Tied to V_{CC}		860		

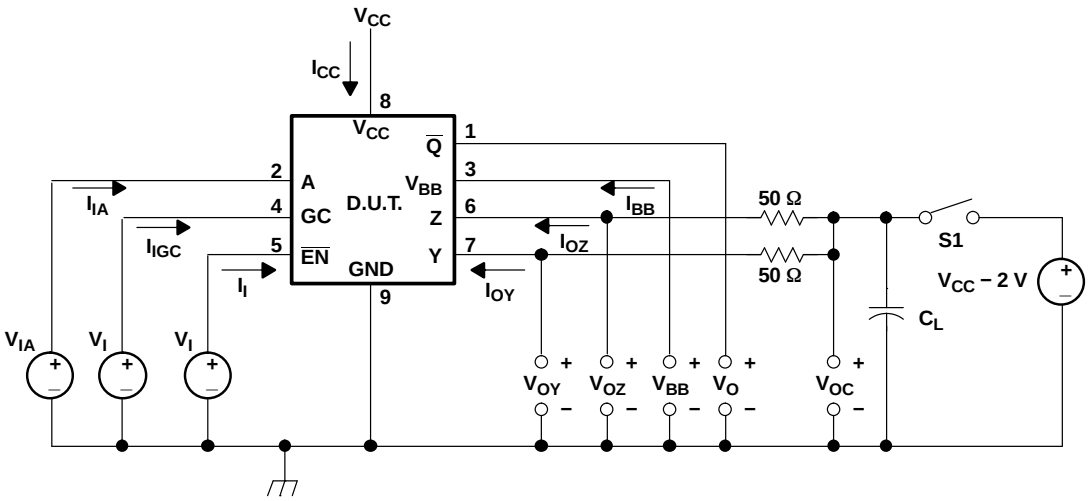
SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PD}	Propagation delay time, t_{PLH} or t_{PHL}	A to $\overline{Q}$	See Figure 4		340	460	ps
		D to Y or Z			460	630	
$t_{SK(P)}$	Pulse skew, $\lvert t_{PLH} - t_{PHL}\rvert$					20	ps
$t_{SK(PP)}$	Part-to-part skew(2)		V_{CC} = 3.3 V			80	ps
			V_{CC} = 2.5 V			130	
t_r	20%-to-80% differential signal rise time		See Figure 4		85	140	ps
t_f	20%-to-80% differential signal fall time				85	140	ps
$t_{jit(per)}$	RMS period jitter(3)		2-GHz 50%-duty-cycle square-wave input, See Figure 5		2	3	ps
$t_{jit(cc)}$	Peak cycle-to-cycle jitter(4)				15	23	
$t_{jit(ph)}$	Intrinsic phase jitter		2 GHz		0.11		ps
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output		See Figure 6			30	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output					30	
t_{PZH}	Propagation delay time, high-impedance-to-high-level output					30	
t_{PZL}	Propagation delay time, high-impedance-to-low-level output					30	

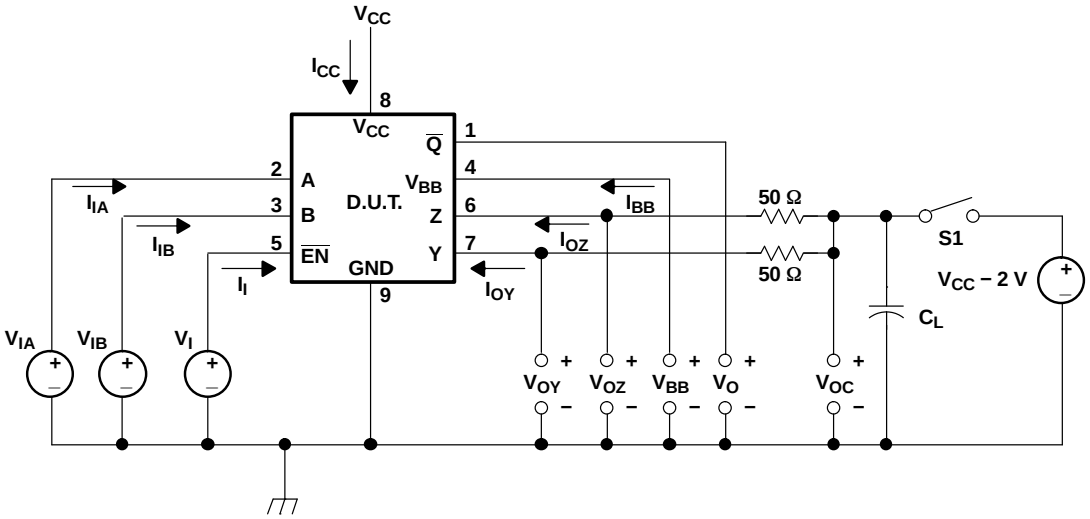
(1) Typical values are at room temperature and with a V_{CC} of 3.3 V.
(2) Part-to-part skew is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) Period jitter is the deviation in cycle time of a signal with respect to the ideal period over a random sample of 100,000 cycles.
(4) Cycle-to-cycle jitter is the variation in cycle time of a signal between adjacent cycles, over a random sample of 1,000 adjacent cycle pairs.

PARAMETER MEASUREMENT INFORMATION



(1) C_L is the instrumentation and test fixture capacitance.
(2) S1 is open for the SN65LVDS16 and closed for the SN65LVP16.

Figure 1. Output Voltage Test Circuit and Voltage and Current Definitions for LVDS/LVP16



(1) C_L is the instrumentation and test fixture capacitance.
(2) S1 is open for the SN65LVDS17 and closed for the SN65LVP17.

Figure 2. Output Voltage Test Circuit and Voltage and Current Definitions for LVDS/LVP17

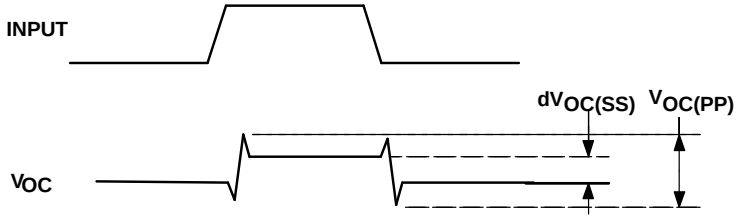


Figure 3. V_{OC} Definitions

PARAMETER MEASUREMENT INFORMATION (continued)

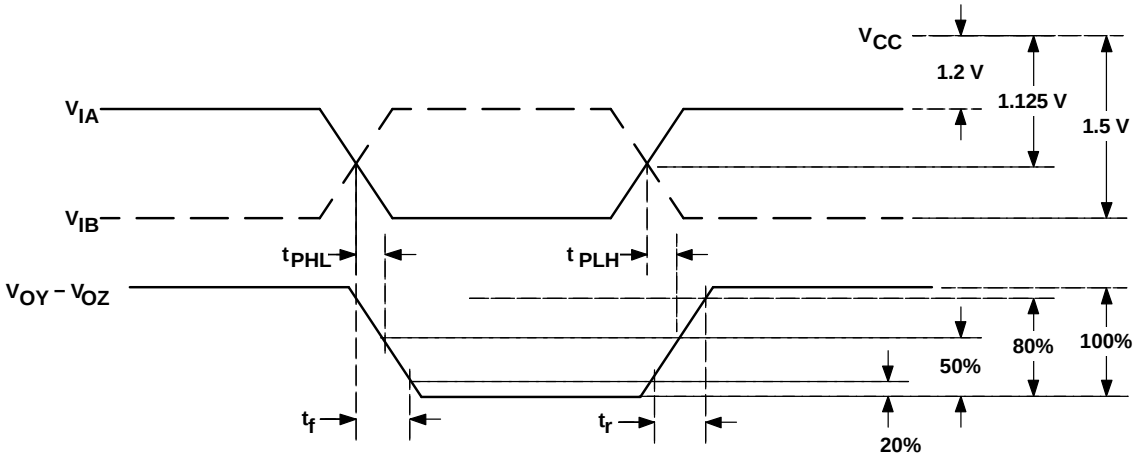


Figure 4. Propagation Delay and Transition Time Test Waveforms

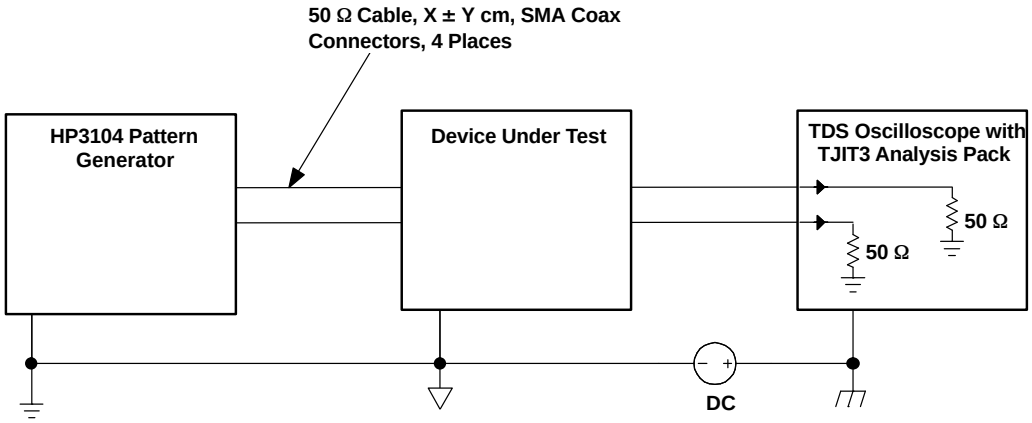


Figure 5. Jitter Measurement Setup

PARAMETER MEASUREMENT INFORMATION (continued)

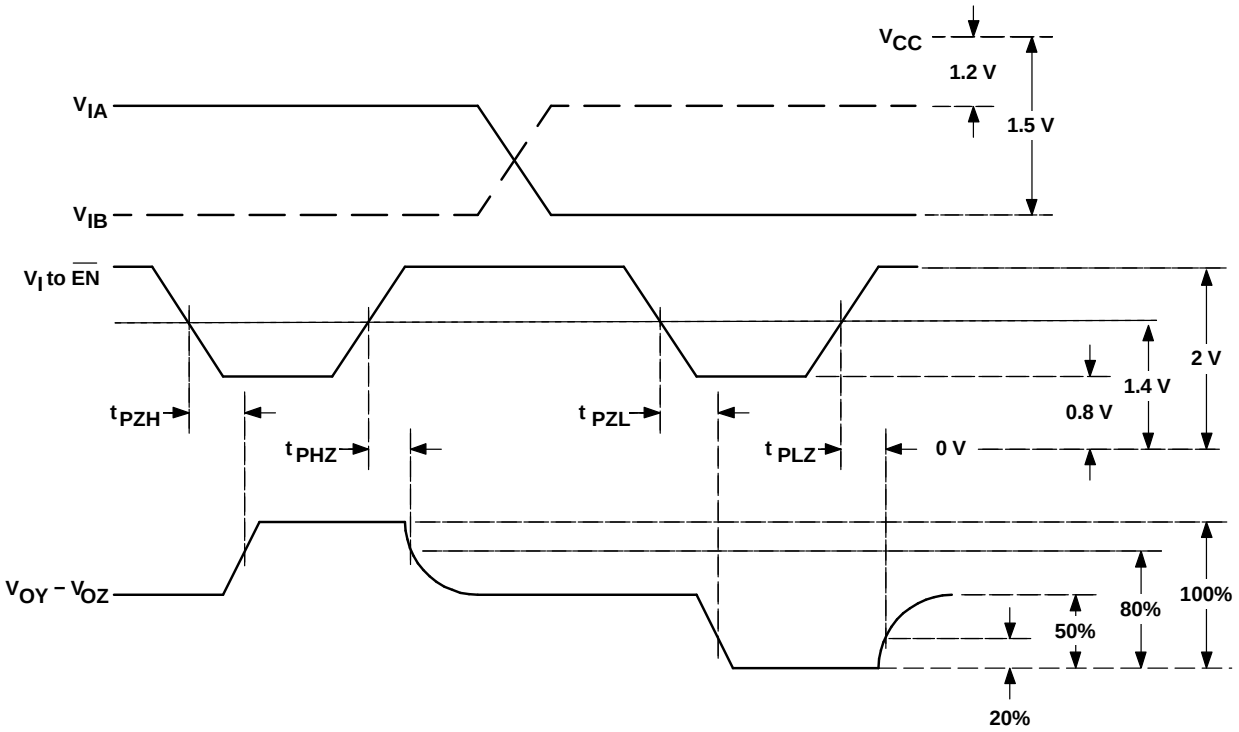


Figure 6. Enable and Disable Time Test Waveforms

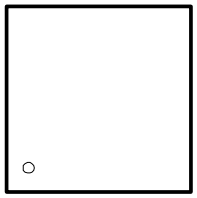
DEVICE INFORMATION

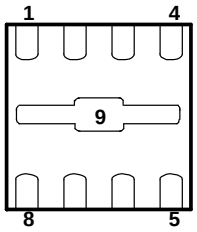
FUNCTION TABLE

SN65LVDS16, SN65LVP16 (1)					SN65LVDS17, SN65LVP17 (1)					
A	$\overline{EN}$	$\overline{Q}$	Y	Z	A	B	$\overline{EN}$	$\overline{Q}$	Y	Z
H	L	L	H	L	H	H	L	?	?	?
L	L	H	L	H	L	H	L	H	L	H
X	H	?	Z	Z	H	L	L	L	H	L
Open	L	?	?	?	L	L	L	?	?	?
X	Open	?	?	?	X	X	H	?	Z	Z
					Open	Open	L	?	?	?
					X	X	Open	?	?	?

(1) H = high, L = low, Z = high impedance, ? = indeterminate

DRF PACKAGE
TOP VIEW





BOTTOM VIEW

Package Pin Assignments - Numerical Listing

SN65LVDS16, SN65LVP16		SN65LVDS17, SN65LVP17	
PIN	SIGNAL	PIN	SIGNAL
1	$\overline{Q}$	1	$\overline{Q}$
2	A	2	A
3	V_{BB}	3	B
4	GC	4	V_{BB}
5	$\overline{EN}$	5	$\overline{EN}$
6	Z	6	Z
7	Y	7	Y
8	V_{CC}	8	V_{CC}
9	GND	9	GND

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs FREQUENCY

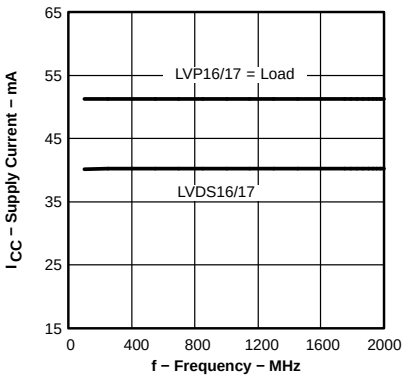


Figure 7.

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

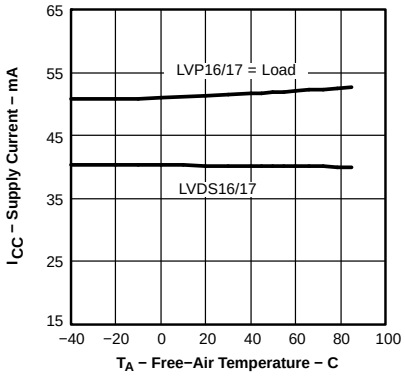


Figure 8.

LVDS16/17 RISE/FALL TIME vs FREE-AIR TEMPERATURE

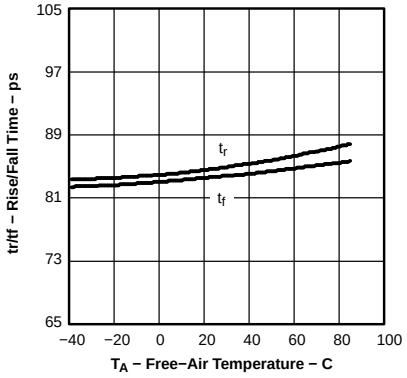


Figure 9.

LVP16/17 RISE/FALL TIME vs FREE-AIR TEMPERATURE

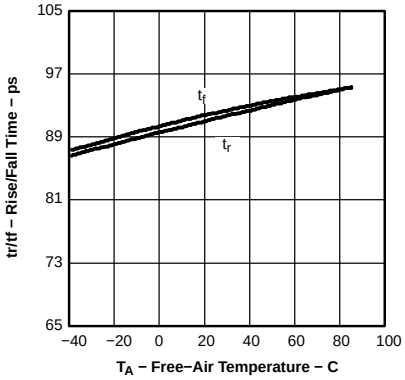


Figure 10.

LVDS16/17 PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

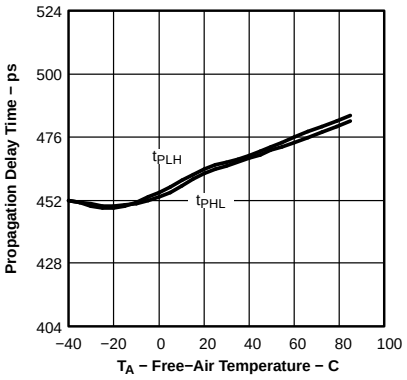


Figure 11.

PERIOD JITTER vs FREQUENCY

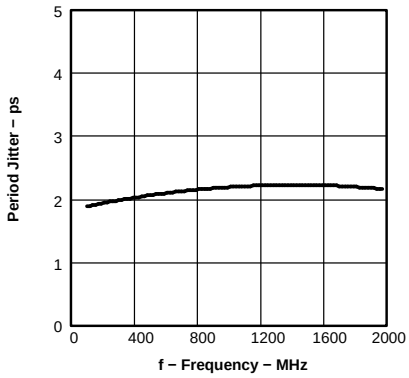


Figure 12.

CYCLE-TO-CYCLE JITTER vs FREQUENCY

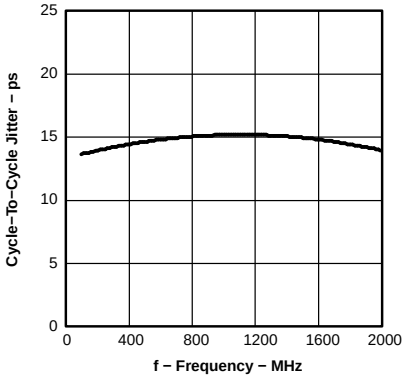
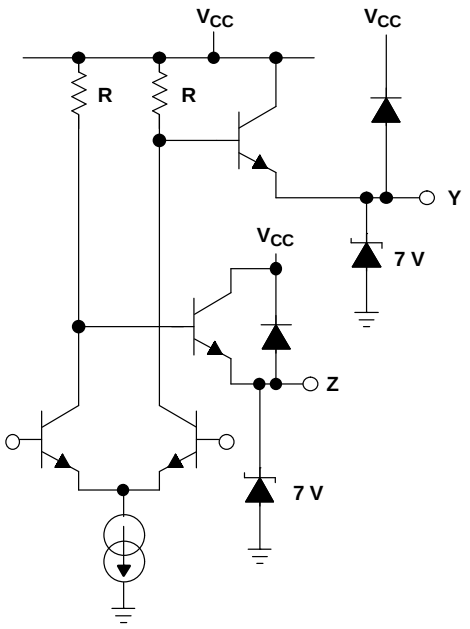


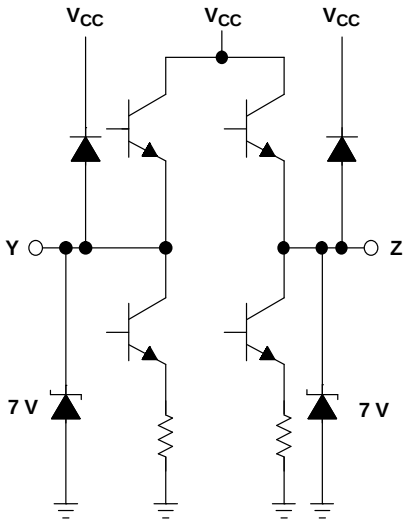
Figure 13.

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

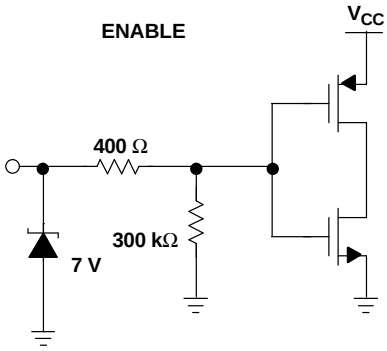
OUTPUT LVP16/17



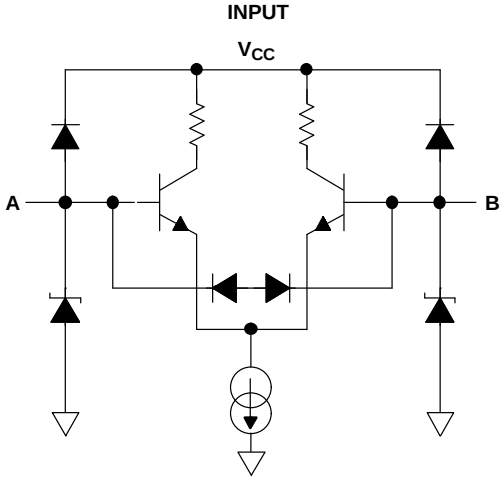
OUTPUT LVDS16/17



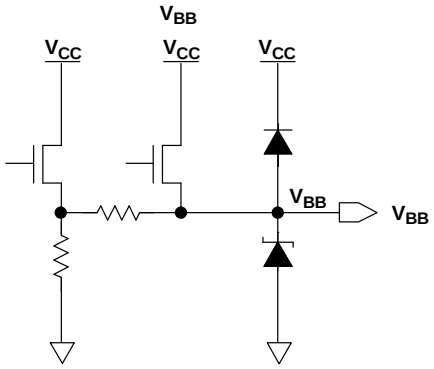
ENABLE



INPUT



OUTPUT



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LVDS16DRFT	ACTIVE	WSON	DRF	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	EL	Samples
SN65LVDS17DRFR	ACTIVE	WSON	DRF	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	EN	Samples
SN65LVDS17DRFT	ACTIVE	WSON	DRF	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	EN	Samples
SN65LVDS17DRFTG4	ACTIVE	WSON	DRF	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	EN	Samples
SN65LVP16DRFT	ACTIVE	WSON	DRF	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	EK	Samples
SN65LVP17DRFR	OBSOLETE	WSON	DRF	8		TBD	Call TI	Call TI	-40 to 85	EM	
SN65LVP17DRFRG4	OBSOLETE	WSON	DRF	8		TBD	Call TI	Call TI	-40 to 85		
SN65LVP17DRFT	ACTIVE	WSON	DRF	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	EM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

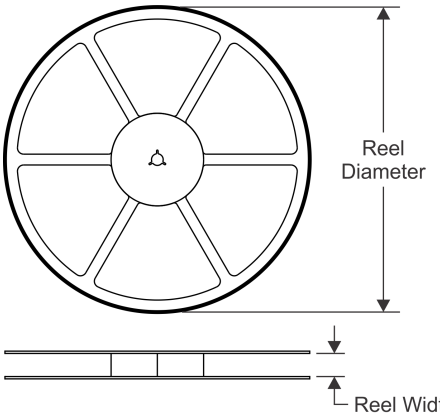
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

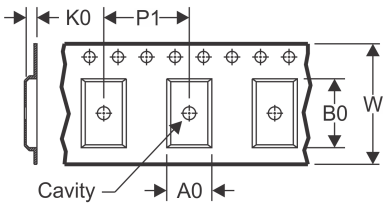
PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

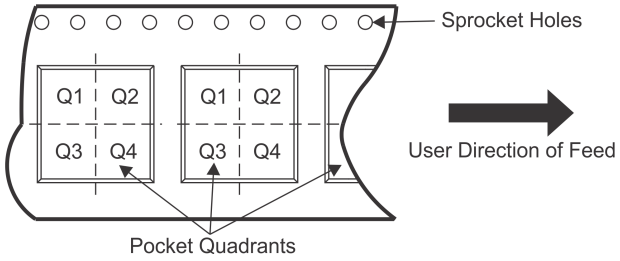


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

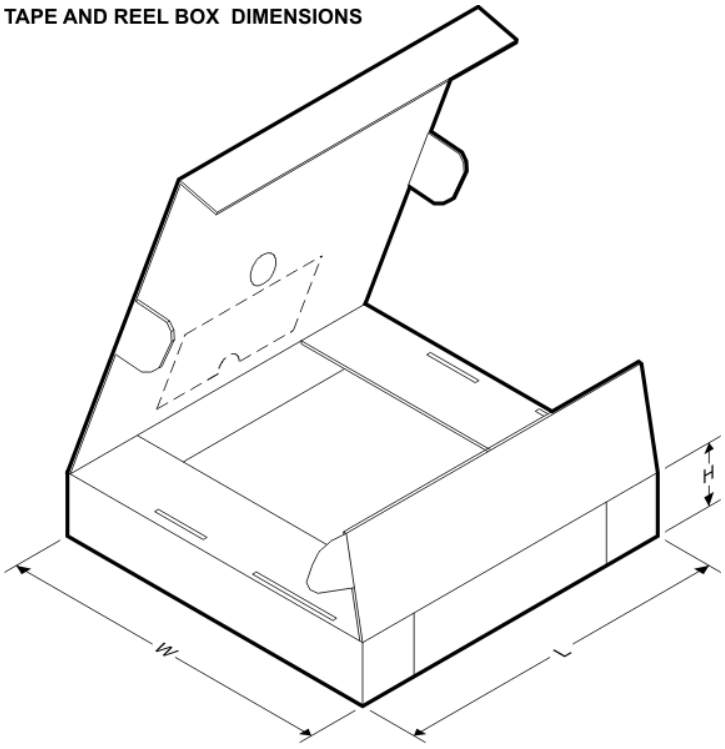


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDS16DRFT	WSON	DRF	8	250	330.0	8.8	2.3	2.3	1.0	4.0	8.0	Q2
SN65LVDS17DRFR	WSON	DRF	8	3000	330.0	8.8	2.3	2.3	1.0	4.0	8.0	Q2
SN65LVDS17DRFT	WSON	DRF	8	250	330.0	8.8	2.3	2.3	1.0	4.0	8.0	Q2
SN65LVP16DRFT	WSON	DRF	8	250	330.0	8.8	2.3	2.3	1.0	4.0	8.0	Q2
SN65LVP17DRFT	WSON	DRF	8	250	330.0	8.8	2.3	2.3	1.0	4.0	8.0	Q2

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

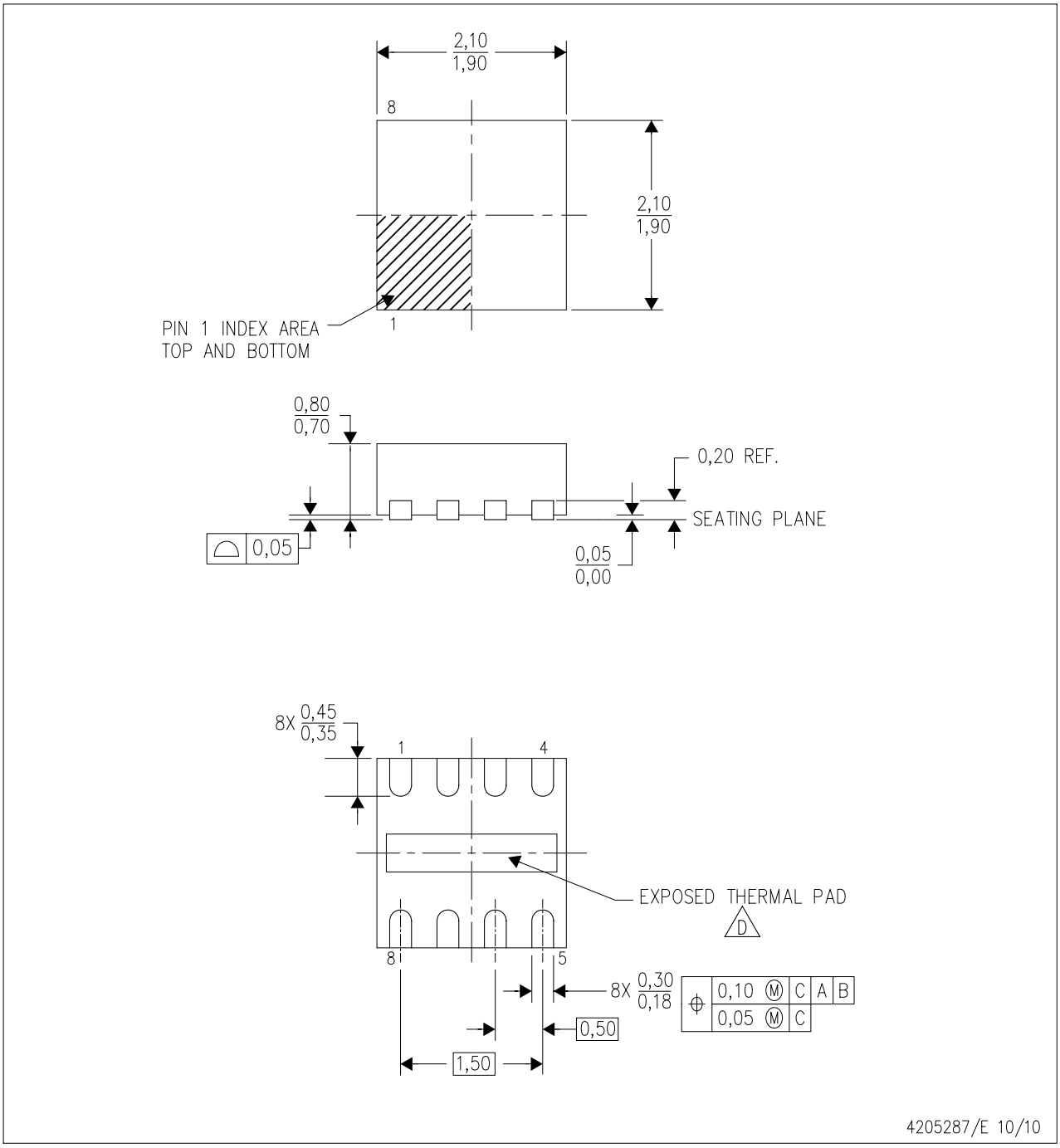


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDS16DRFT	WSON	DRF	8	250	337.0	343.0	29.0
SN65LVDS17DRFR	WSON	DRF	8	3000	337.0	343.0	29.0
SN65LVDS17DRFT	WSON	DRF	8	250	337.0	343.0	29.0
SN65LVP16DRFT	WSON	DRF	8	250	337.0	343.0	29.0
SN65LVP17DRFT	WSON	DRF	8	250	337.0	343.0	29.0

MECHANICAL DATA

DRF (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The Package thermal pad must be soldered to the board for thermal and mechanical performance. See product data sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–229.

THERMAL PAD MECHANICAL DATA

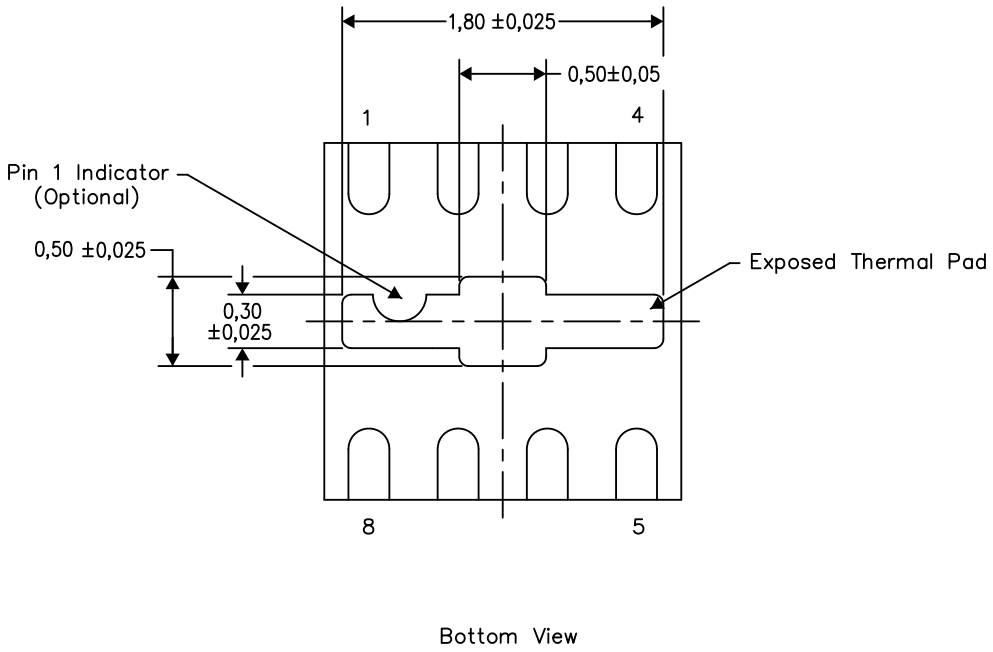
DRF (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

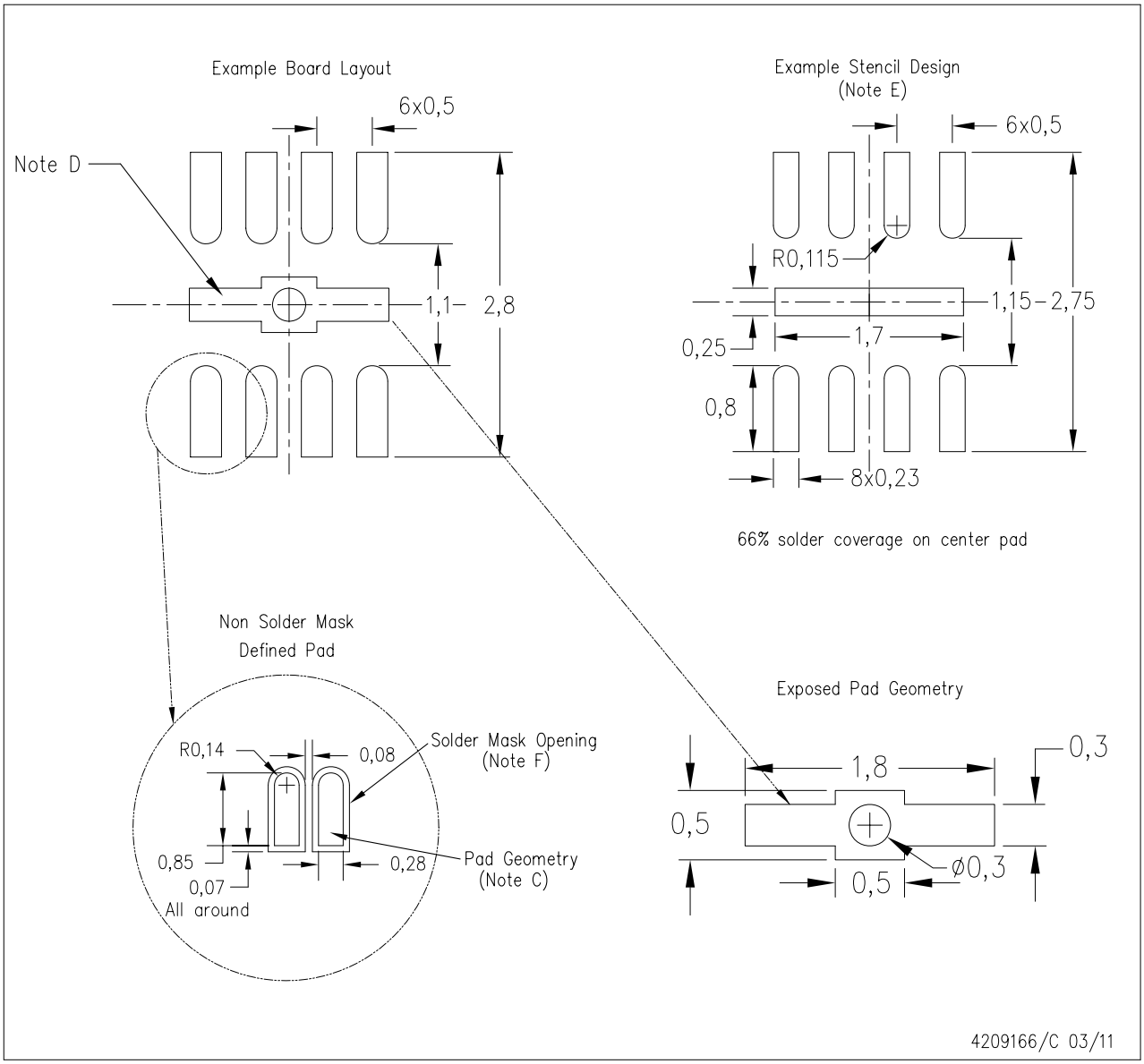
Exposed Thermal Pad Dimensions

4206840/H 12/14

NOTE: A. All linear dimensions are in millimeters

LAND PATTERN DATA

DRF (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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