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L9386MD

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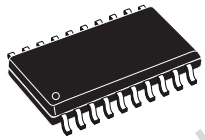
L9386

Dual intelligent power low side switch

Features

- Multipower BCD technology
- Dual power low side driver with 2 x 5 A
- Low R_{DSON} typically 200 mΩ @ T_J = 25 °C
- Internal output clamping diodes V_{FB} = 50 V for inductive recirculation
- Limited output voltage slew rate for low EMI
- µP compatible enable and input
- Wide operating supply voltage range 4.5 V to 45 V
- Real time diagnostic functions:
  - Output shorted to GND
  - Output shorted to V_{SS}
  - Open load
  - Load bypass
  - Over temperature
- Device protection functions:
  - Overload disable
  - Reverse battery up to -16 V @ V_S
  - Thermal shutdown



SO20

Description

The L9386 is a monolithic integrated dual low side driver realized in an advanced Multipower BCD mixed technology.

It is especially intended to drive valves in automotive environment. Its inputs are µP compatible for easy driving. Particular care has been taken to protect the device against failures, to avoid electro-magnetic interferences and to offer extensive real time diagnostic.

Table 1. Device summary

Part number	Order code	Package	Packing
L9386	L9386MD	SO20 (12+4+4)	Tube

Contents

1 Block and pins connection diagrams

Figure 1. Block diagram

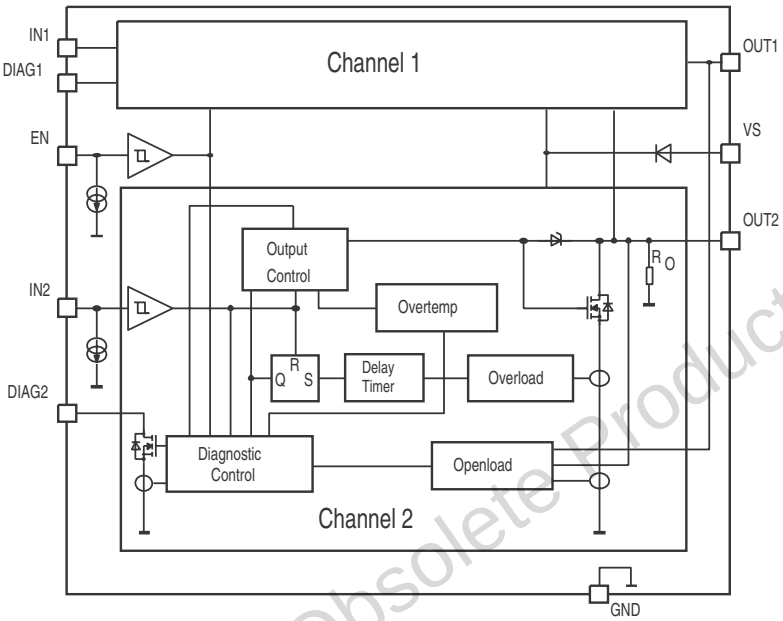
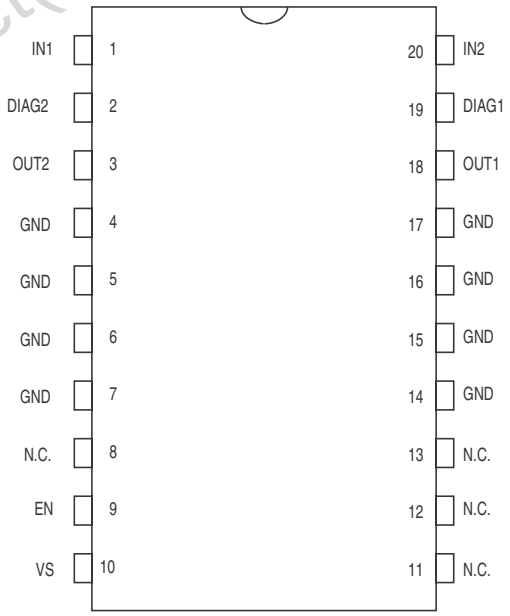


Figure 2. Pins connection (top view)



2 Electrical specifications

2.1 Absolute maximum ratings

Table 2. Absolute maximum ratings (no damage or latch)

Symbol	Parameter	Value	Unit
V_{SDC}	DC supply voltage	-16 to 45	V
V_{STR}	Transient supply voltage ($t \leq 500$ ms)	60	V
V_{IN},EN	Input voltage ($\lvert I \rvert \leq \lvert 10$ mA $\rvert$)	-1.5 to 6	V
V_{DDC}	Diagnostic DC output voltage ($\lvert I \rvert \leq \lvert 50$ mA $\rvert$)	-0.3 to 16	V
V_{ODC}	DC output voltage	45	V
V_{OTR}	Transient output voltage ($R_L \geq 4\ \Omega$)	60	V
I_O	Output load current	internal limited	
I_{OR}	Reverse output current limited by load	-4	A
EO	Switch-off energy for inductive loads (t_{EO} = 250 µs, T = 5 ms)	50	mJ
T_{jEO}	Junction temperature during switch-off Σt = 30 min	175	°C
T_j	Junction temperature	-40 to +150	°C
T_{stg}	Storage temperature	-55 to +150	°C

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
T_{jDIS}	Thermal disable junction temperature threshold	160 to 190	°C
$R_{th\ j\text{-}pins}$	Thermal resistance junction to pins	14	°C/W

2.3 Electrical characteristics

Table 4. Electrical characteristics

(The electrical characteristics are valid within the below defined operative range, unless otherwise specified.)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_S	Board supply voltage		4.5	12	32	V
V_D	Stabilized diagnostic output voltage		-0.3	5	16	V
T_j	Junction temperature		-40		150	°C
IS_{SB}	Static standby supply current	(1) (2) V_{EN} = L, VO ≤ VO_{uv}		0.73	1.5 15	mA
IS	DC supply current	(1) (2) V_{EN} = V_{IN} = H		1.3	5 15	mA
VD_L	Diagnostic output low voltage	(1) I_D = 2 mA (2) I_D = 1 mA		0.35	0.5	V
ID_{LE}	Diagnostic output leakage current	V_S = 0 V or V_S = open; V_D = 5.5 V T_j ≤ 125 °C		0.1	2	mA
ID	Diagnostic output current capability	V_D ≤ 16 V DIAG = L	2	6	30	mA
VO_{UV}	Open load voltage threshold	V_{EN} = X, V_{IN} = L	0.51 xVS	0.55 xVS	0.59 xVS	V
$\Delta VO_{UV1,2}$	Open load difference voltage threshold	(1) V_{EN} = X, $V_{IN1,2}$ = L V_S ≥ VO_C ≥ VO_{UV} VO_C = output voltage of other channel (2)	VO_C-0.9V VO_C-0.7V	VO_C-1.25V VO_C-1.25V	VO_C-1.6V VO_C-1.8V	V
IO_{UC}	Open load current threshold	(3) V_{EN} = V_{IN} = H (2)	100 20	320	480	mA
IO_{OC}	Over load current threshold	b)	5	7		A
V_{OCL}	Output voltage during clamping	IO_{CL} ≥ 100mA	45	52	60	V
$S_{ON,OFF}$	Output (fall, rise) slew rate	(3) see *Figure 4*	200	1500	3200	V/ms
R_{IO}	Internal output pull down resistor	V_{EN} = L	10	20	40	KΩ
R_{DSON}	Output on resistance	V_S > 9.5 V I_O = 2 A T_j = 25 °C T_j = 150 °C		200	300 500	mΩ
$V_{(EN,IN)L}$	Logic input low voltage	I_{EN}, I_N ≤ 10 mA (1) (2)	-1.5 -1.5		1 0.5	V
$V_{(EN,IN)H}$	Logic input high voltage		2.2		5.5	V

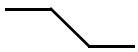
Table 4. Electrical characteristics (continued)

(The electrical characteristics are valid within the below defined operative range, unless otherwise specified.)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{(EN,IN)hys}$	Logic input hysteresis		0.2	0.4	1	V
I_{EN}	Enable input sink current	1 V ≤ V_{EN} ≤ 5.5 V	10	30	60	µA
I_{IN}	Logic input sink current	1 V ≤ V_{IN} ≤ 5.5 V	40	95	180	µA
t_{DON}	Output delay ON time	(3) see *Figure 4*		4	25	µs
t_{DOFF}	Output delay OFF time	(3) see *Figure 4*	5	15	30	µs
$t_{DH-L,Diag.}$	Diag. delay output OFF time	(3) see *Figure 4*	5	30	65	µs
t_{DIOu}	Diagnostic open load delay time	(3) see *Figure 6*		8	50	µs
t_{DOL}	Diagnostic overload delay switch-off time	(3) see *Figure 3*	50	160	300	µs

1. 6.5 V ≤ V_S ≤ 16 V (Diagnostic operation range).
2. 4.5 V ≤ V_S < 6.5 V and 16 V < V_S ≤ 32 V (Extended operation range).
3. 9 V ≤ V_S ≤ 16 V (Nominal operating range)
   R_L ≤ 6 Ω, I_O ≤ IO_{OC}.

Table 5. Diagnostic table (operating range: 4.5 V ≤ V_S ≤ 32 V)

Conditions		EN	IN	Out	Diag.
Normal function		L H H	X L H	off off on(1)	L L H
GND short	VO_{typ} < 0.55 V	L	X	off	H
Load bypass	$\Delta VO_{1,2}$ ≥ 1.25 V	H	L	off	H
Open load	IO_{typ} < 320 mA	H	H	on(1)	L
$T_{j\ typ}$ ≥ 175 °C overtemperature(2)		X X	L H	off off	H L
Latched overload IO_{min} > 5 A		X	H	off	L
Reset overload latch		X		D.C.	D.C.

1. for 4.5 V ≤ V_S < 6.5 V, I_O ≤ 2 A diag. table is valid.
2. If one diag. status shows the overtemperature recognition, in parallel this output will be switched OFF internally. The corresponding channel should be switched OFF additional by its Input or ENABLE signal, otherwise the overload latch will be set after t_{DOL} is passed. This behavior will be related to the overdrop sensing which will be used as over load recognition.

Figure 3. Diagnostic overload delay time

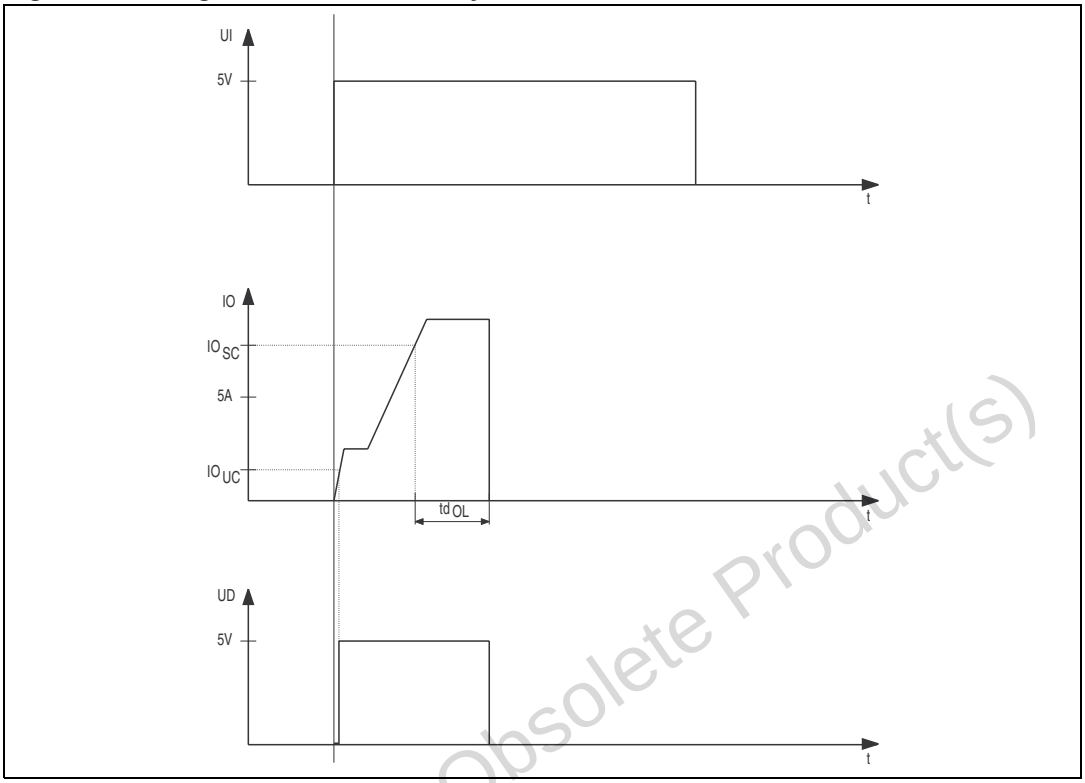


Figure 4. Output slope

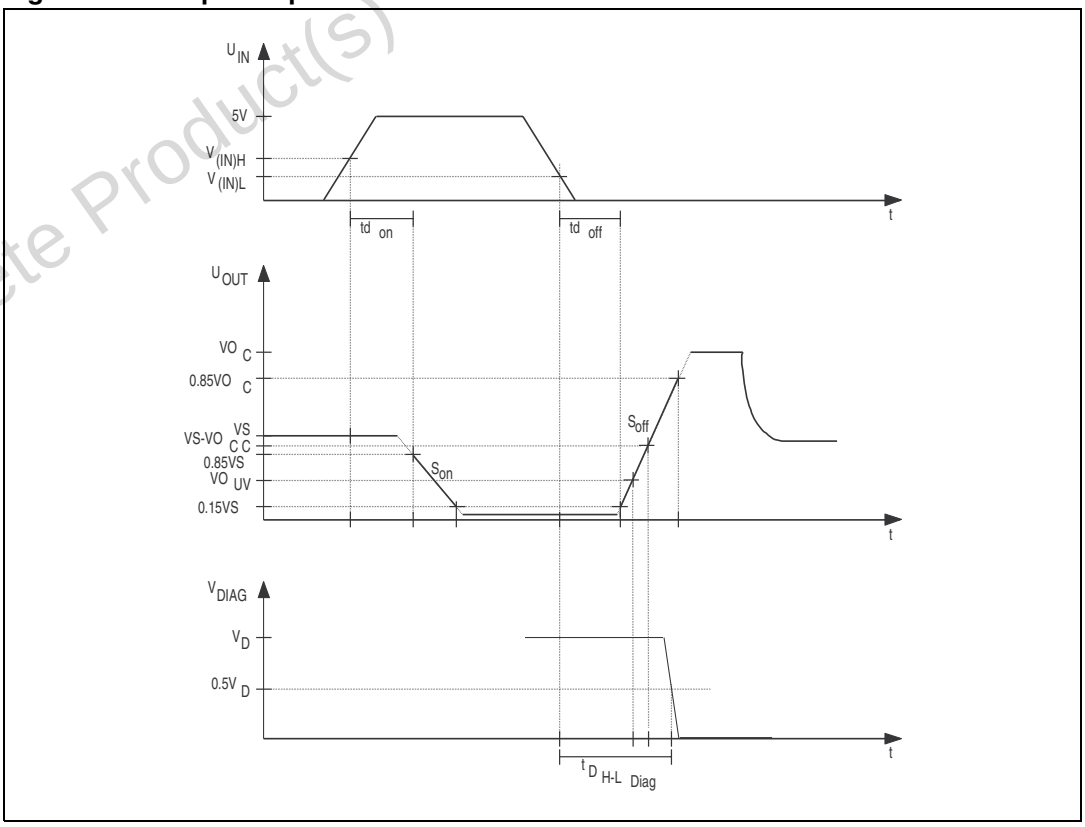


Figure 5. Open load voltage detection block diagram

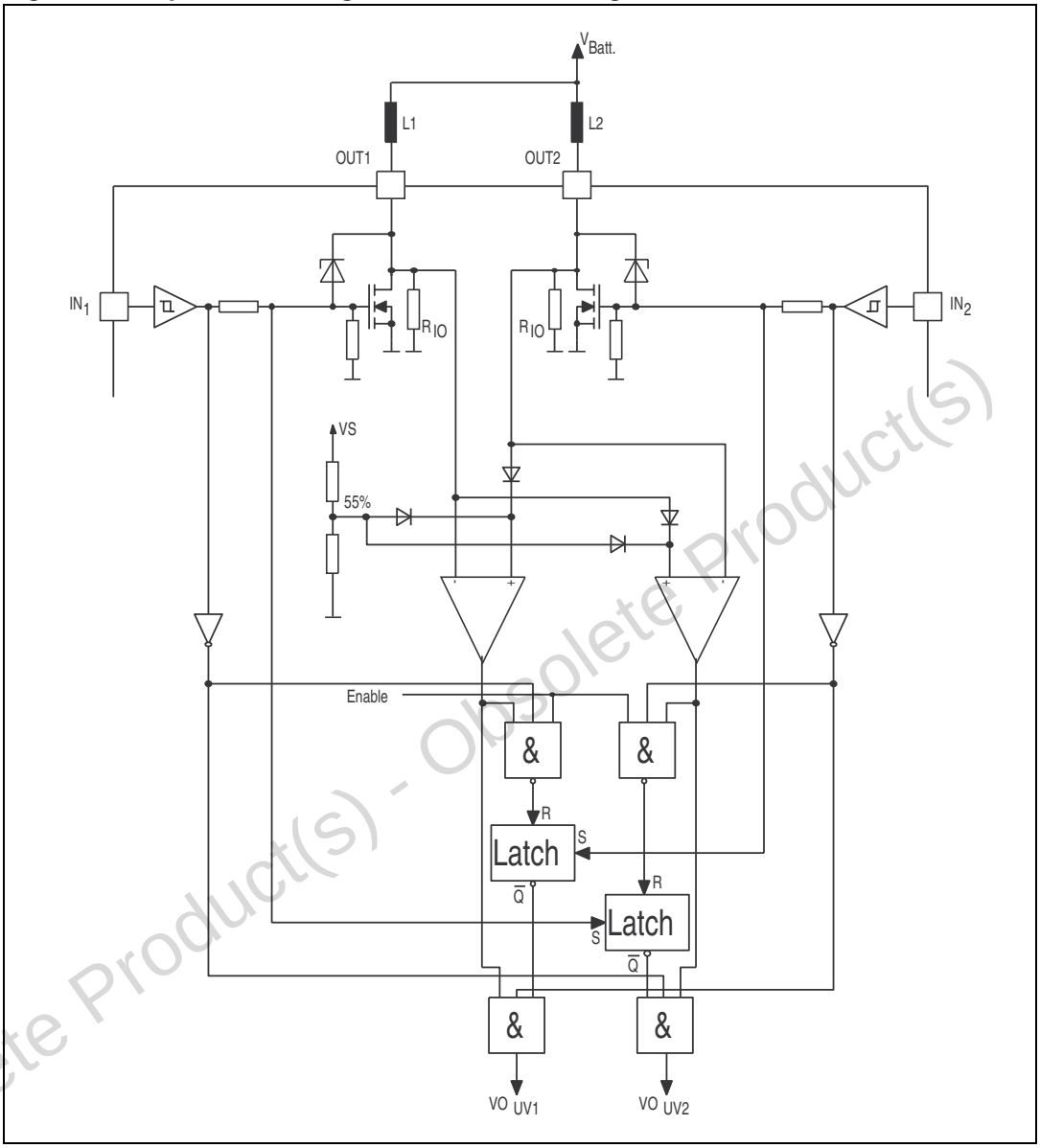
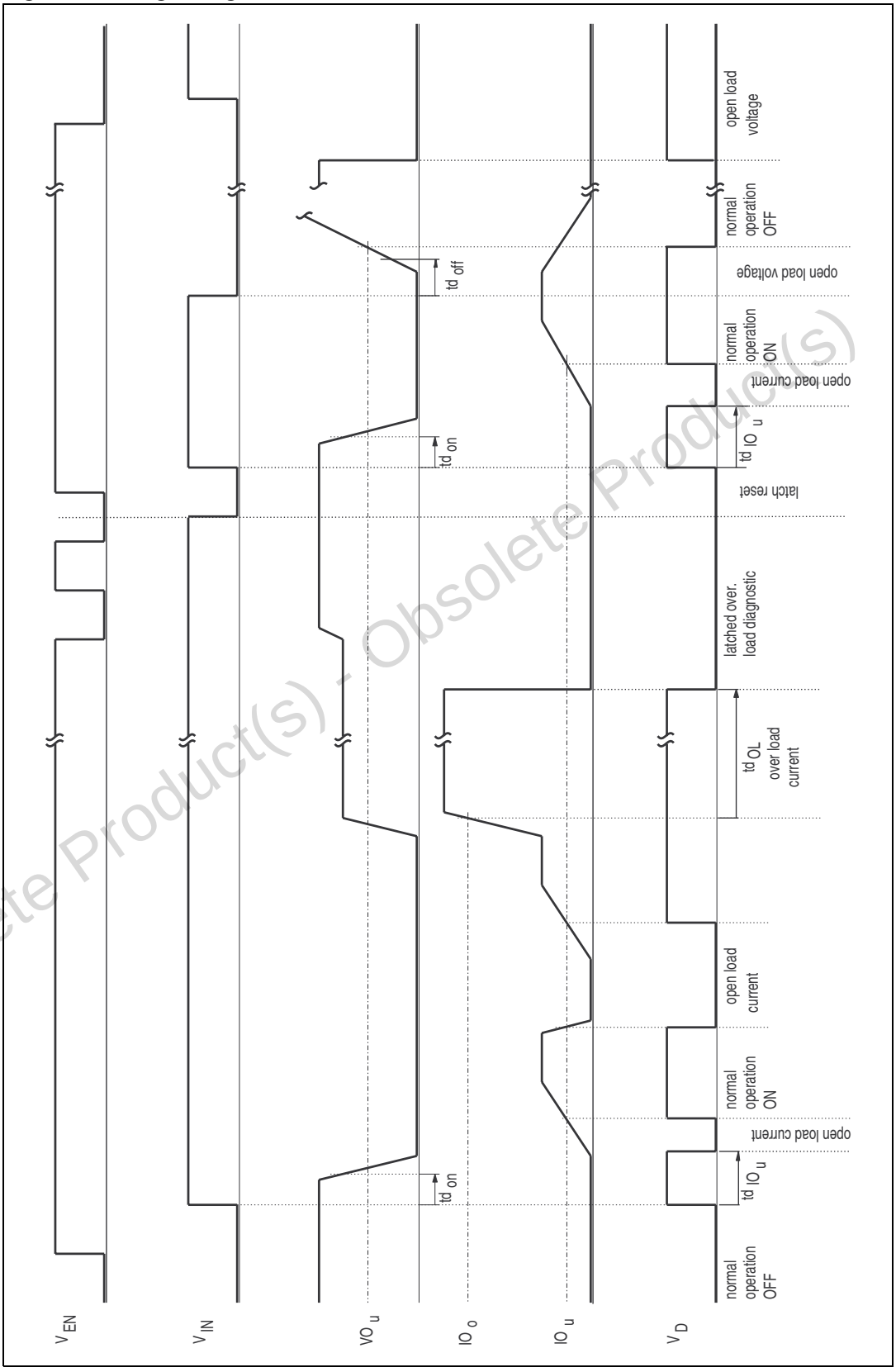


Figure 6. Logic diagram



2.4 Circuit description

The L9386 is a dual low side driver for inductive loads like valves in automotive environment.

The device is enabled by a common CMOS compatible ENABLE high signal. The internal pull down current sources at the ENABLE and INPUT pins protect the device in open input conditions against malfunctions. An output slope limitation for du/dt is implemented to reduce the EMI. An integrated active flyback voltage limitation clamps the output voltage during the flyback phase to 50V.

Each driver is protected against short circuit and thermal overload. In short circuit condition the output will be disabled after a short delay time t_{DOL} to suppress spikes. This disable is latched until a negative slope occur at the correspondent input pin. The thermal disable for $T_J > 175$ °C of the output will be resetted if the junction temperature decreases about 20 °C below the disable threshold temperature.

For the real time error diagnosis the voltage and the current of the outputs are compared with internal fixed values V_{OUV} for OFF and I_{OUC} for ON conditions to recognize open load ($R_L \geq 20$ kΩ, $R_L > 38$Ω) in ON and OFF conditions. The diagnostic operates also in the extended supply voltage range of $4.5\ V \leq V_S \leq 32\ V$.

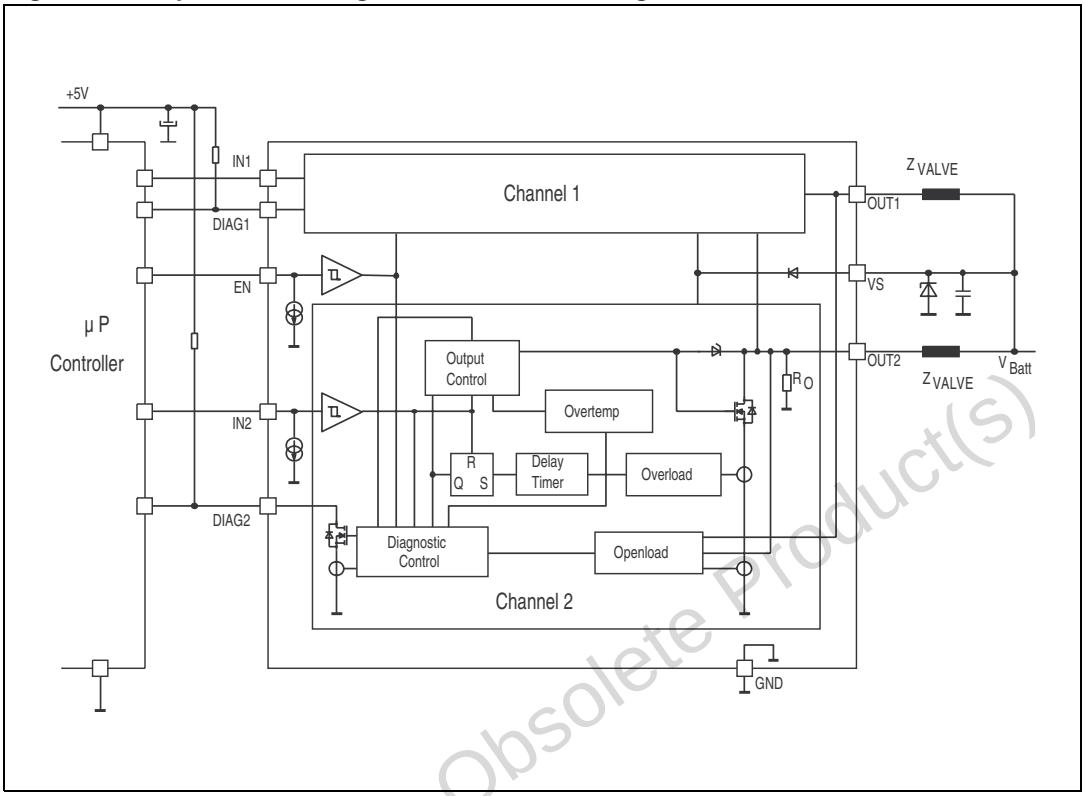
Also the output voltages $VO_{1,2}$ are compared against each other in OFF condition with a fixed offset of $\Delta VO_{UV\ 1,2}$ to recognize GND bypasses. To suppress mail ΔVO diagnoses during the flyback phases of the compared output, the ΔVO diagnostic

includes a latch function. Reaching the flyback clamping voltage VO_C the diagnostic signal is resetted by a latch. To activate again this kind of diagnostic a low signal at the correspondent INPUT or the ENABLE pin must occur (see also *Figure 5*).

The diagnostic output level in connection with different ENABLE and INPUT conditions allows to recognize different fail states, like overtemperature, short to VSS, short to GND, bypass to GND and disconnected load (see also *Table 5 on page 6*).

The diagnostic output is also protected against short to UD_{max}. Oversteping the over load current threshold IO_o, the output current will be limited internally during the diagnostic overload delay switch-off time t_{DOL}.

Figure 7. Open load voltage detection block diagram



3 Package information

In order to meet environmental requirements, ST (also) offers these devices in ECOPACK® packages. ECOPACK® packages are lead-free. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

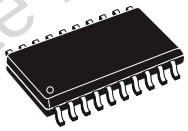
ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 8. SO20 mechanical data and package dimensions

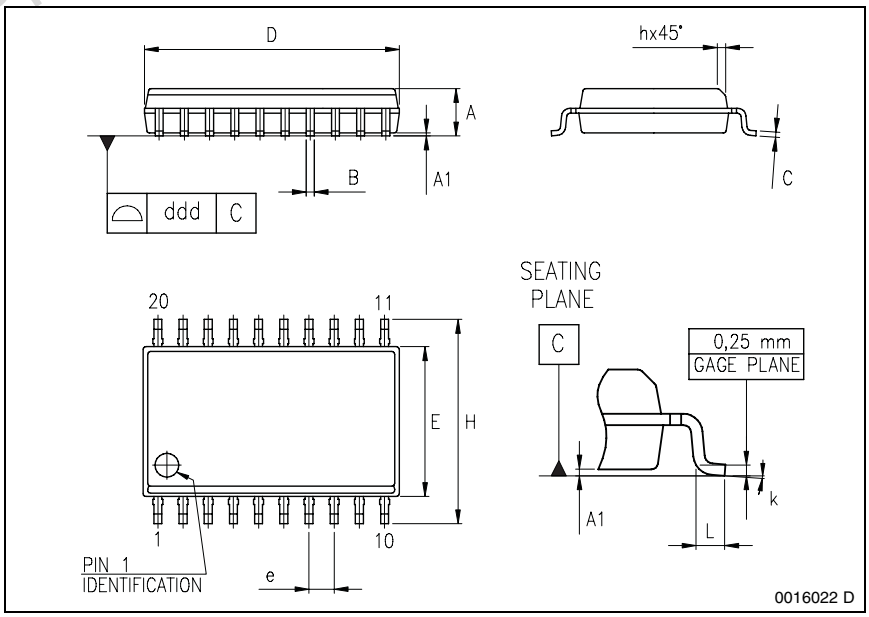
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.35		2.65	0.093		0.104
A1	0.10		0.30	0.004		0.012
B	0.33		0.51	0.013		0.200
C	0.23		0.32	0.009		0.013
D (1)	12.60		13.00	0.496		0.512
E	7.40		7.60	0.291		0.299
e		1.27			0.050	
H	10.0		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

(1) "D" dimension does not include mold flash, protusions or gate burrs. Mold flash, protusions or gate burrs shall not exceed 0.15mm per side.

OUTLINE AND MECHANICAL DATA



SO20



4 Revision history

Table 6. Document revision history

Date	Revision	Changes
16-Jan-2002	1	Initial release.
20-Sep-2003	2	Changed company name and logo.
16-Jul-2008	3	Document reformatted. Added *Table 1: Device summary on page 1*.

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