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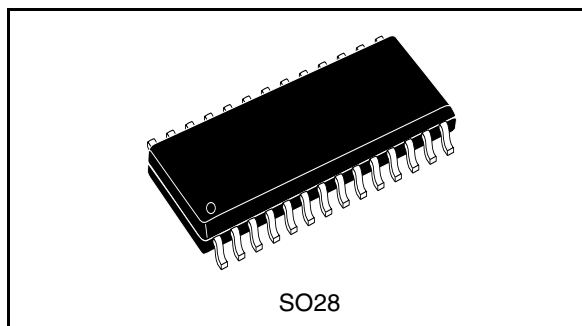


# TDA7439DS

## Three-band digitally-controlled audio processor

### Features

- Input multiplexer
  - four stereo inputs
  - selectable input gain for optimal adaptation to different sources
- Single stereo output
- Treble, mid-range and bass control in 2-dB steps
- Volume control in 1-dB steps
- Two speaker attenuators:
  - two independent speaker controls in 1-dB steps for balance facility
  - independent mute function
- All functions are programmable via serial bus.



SO28

processor for quality audio applications in car-radio and Hi-Fi systems. Selectable input gain is provided. All the functions are controlled by serial bus.

The AC signal setting is obtained by resistor networks and switches combined with operational amplifiers.

The TDA7439DS employs BIPOLAR/CMOS technology to provide low distortion, low noise and DC stepping.

### Description

The TDA7439DS is a volume, tone (bass, mid-range and treble) and balance (left/right)

**Table 1. Device summary**

Order codes	Package	Packaging
TDA7439DS	SO28	Tube
TDA7439DS13TR	SO28	Tape and Reel

# Contents

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# 1 Block diagram and pin out

Figure 1. Block diagram

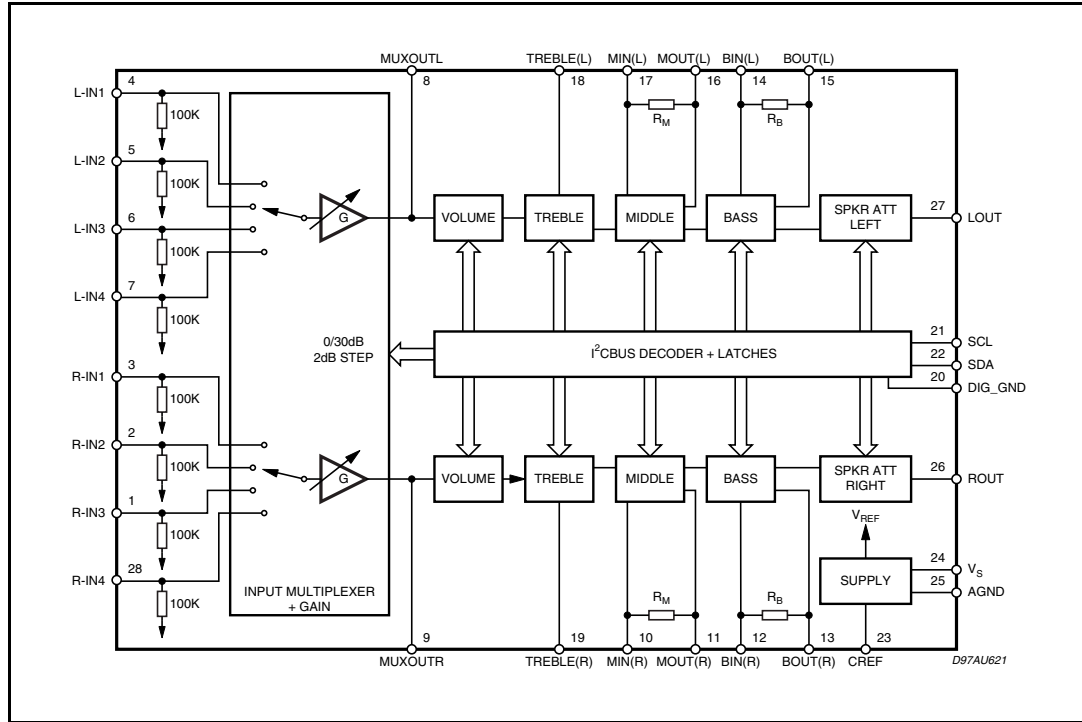
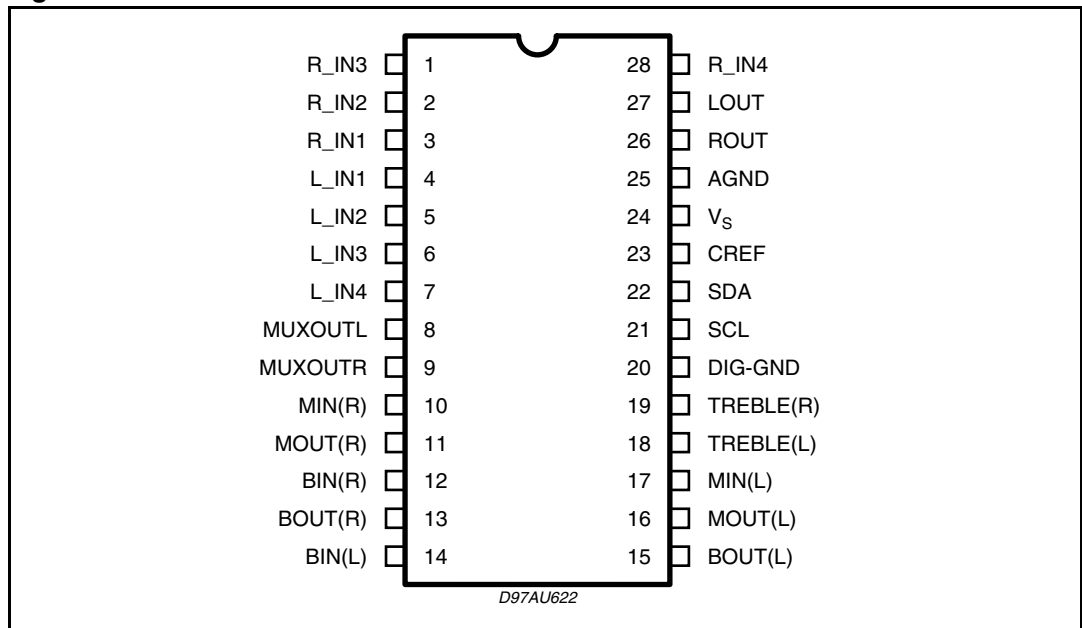


Figure 2. Pin connections



Electrical specifications

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## 2 Electrical specifications

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_S$	Operating supply voltage	10.5	V
$T_{amb}$	Operating ambient temperature	0 to 70	°C
$T_{stg}$	Storage temperature range	-55 to 150	°C

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{th\ j-pin}$	Thermal resistance junction-pins	85	°C/W

**Table 4. Quick reference data**

Symbol	Parameter	Min.	Typ	Max	Unit
$V_S$	Supply voltage	7	9	10.2	V
$V_{CL}$	Max. input signal handling	2			V RMS
THD	Total harmonic distortion $V = 1\text{ V RMS}$ , $f = 1\text{ kHz}$		0.01	0.1	%
S/N	Signal to noise ratio $V_{out} = 1\text{ V RMS}$ (mode = OFF)		106		dB
$S_C$	Channel separation $f = 1\text{ kHz}$		90		dB
	Input gain (in 2 dB steps)	0		30	dB
	Volume control (in 1 dB steps)	-47		0	dB
	Treble control (in 2 dB steps)	-14		+14	dB
	Middle control (in 2 dB steps)	-14		+14	dB
	Bass control (in 2 dB steps)	-14		+14	dB
	Balance control (in 1 dB steps)	-79		0	dB
	Mute attenuation		100		dB

*Table 5.* shows the electrical characteristics. Refer to the test circuit in *Figure 3*,  $T_{amb} = 25^\circ\text{C}$ ,  $V_S = 9\text{ V}$ ,  $R_L = 10\text{ k}\Omega$ , generator resistance  $R_g = 600\ \Omega$ , all controls flat ( $G = 0\text{ dB}$ ), unless otherwise specified.

**Table 5. Electrical characteristics**

Symbol	Parameter	Test condition	Min.	Typ	Max	Unit
<b>Supply</b>						
$V_S$	Supply voltage		7	9	10.2	V
$I_S$	Supply current		4	7	10	mA
SVR	Ripple rejection		60	90		dB

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Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ	Max	Unit
<b>Input stage</b>						
R <sub>IN</sub>	Input resistance		70	100	130	kΩ
V <sub>CL</sub>	Clipping level	THD = 0.3%	2	2.5		V RMS
S <sub>IN</sub>	Input separation	The selected input is grounded through a 2.2 μF capacitor	80	100		dB
G <sub>in_min</sub>	Minimum input gain		-1	0	1	dB
G <sub>in_max</sub>	Maximum input gain		29	30	31	dB
G <sub>step</sub>	Step resolution		1.5	2	2.5	dB
<b>Volume control</b>						
R <sub>i</sub>	Volume control input resistance		20	33	50	kΩ
C <sub>range</sub>	Volume control range		45	47	49	dB
A <sub>v_max</sub>	Max. attenuation		45	47	49	dB
A <sub>step</sub>	Step resolution		0.5	1	1.5	dB
E <sub>A</sub>	Attenuation set error	A <sub>V</sub> = 0 to -24 dB	-1.0	0	1.0	dB
		A <sub>V</sub> = -24 to -47 dB	-1.5	0	1.5	dB
ET	Tracking error	A <sub>V</sub> = 0 to -24 dB		0	1	dB
		A <sub>V</sub> = -24 to -47 dB		0	2	dB
V <sub>DC</sub>	DC step	adjacent attenuation steps from 0 dB to A <sub>v_max</sub>		0 0.5	3	mV mV
A <sub>mute</sub>	Mute attenuation		80	100		dB
<b>Bass control (1)</b>						
G <sub>b</sub>	Control range	Max. boost/cut	±12.0	±14.0	±16.0	dB
B <sub>step</sub>	Step resolution		1	2	3	dB
R <sub>B</sub>	Internal feedback resistance		33	44	55	kΩ
<b>Treble control (1)</b>						
G <sub>t</sub>	Control range	Max. boost/cut	±13.0	±14.0	±15.0	dB
T <sub>step</sub>	Step resolution		1	2	3	dB
<b>Mid-range control (1)</b>						
G <sub>m</sub>	Control range	Max. boost/cut	±12.0	±14.0	±16.0	dB
M <sub>step</sub>	Step resolution		1	2	3	dB
R <sub>M</sub>	Internal feedback resistance		18.75	25	31.25	kΩ

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Table 5. Electrical characteristics (continued)

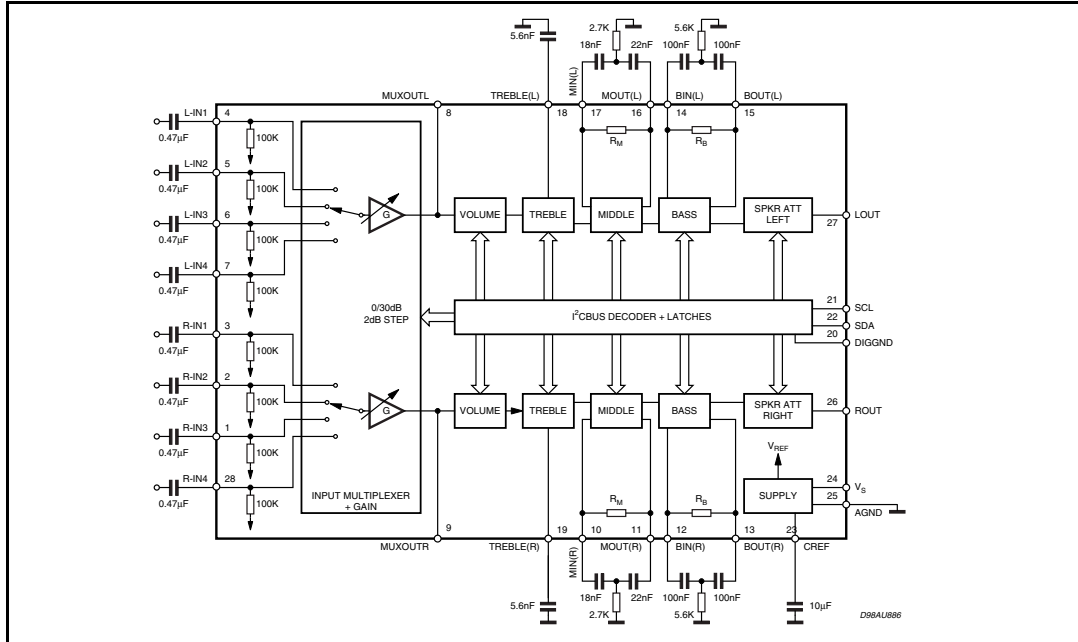
Symbol	Parameter	Test condition	Min.	Typ	Max	Unit
<b>Speaker attenuators</b>						
$C_{range}$	Control range		70	76	82	dB
$S_{step}$	Step resolution		0.5	1	1.5	dB
$E_A$	Attenuation set error	$A_V = 0$ to $-20$ dB	-1.5	0	1.5	dB
		$A_V = -20$ to $-56$ dB	-2	0	2	dB
$V_{DC}$	DC step	Adjacent attenuation steps		0	3	mV
$A_{mute}$	Mute attenuation		80	100		dB
<b>Audio outputs</b>						
$V_{CLIP}$	Clipping level	$d = 0.3\%$	2.1	2.6		V <sub>rms</sub>
$R_L$	Output load resistance		2			k $\Omega$
$R_O$	Output impedance		10	40	70	$\Omega$
$V_{OUTDC}$	DC voltage level		3.5	3.8	4.1	V
<b>General</b>						
$E_{NO}$	Output noise	All gains = 0 dB; BW = 20 Hz to 20 kHz flat		5	15	$\mu$ V
$E_t$	Total tracking error	$A_V = 0$ to $-24$ dB		0	1	dB
		$A_V = -24$ to $-47$ dB		0	2	dB
S/N	Signal to noise ratio	All gains 0 dB, $V_O = 1$ V RMS	95	106		dB
$S_C$	Channel separation, left/right		80	100		dB
d	Distortion	$A_V = 0$ , $V_I = 1$ V RMS		0.01	0.08	%
<b>Bus input</b>						
$V_{IL}$	Input low voltage				1	V
$V_{IH}$	Input high voltage		3			V
$I_{IN}$	Input current	$V_{IN} = 0.4$ V	-5	0	5	$\mu$ A
$V_O$	Output voltage SDA acknowledge	$I_O = 1.6$ mA		0.4	0.8	V

- For bass, mid-range and treble response: the center frequency and the response quality can be set by the external circuitry.

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Electrical specifications

Figure 3. Test circuit





### 3 Application suggestions

The first and the last stages are volume control blocks. The control range is 0 to -47 dB and mute for the first stage and 0 to -79 dB and mute for the last one. Both control blocks have a step resolution of 1 dB.

This very high resolution allows the implementation of systems free from any noisy acoustical effect.

The TDA7439DS audio processor provides 3 bands of tone control (bass, mid-range and treble).

#### 3.1 Tone control

##### 3.1.1 Bass, mid-range stages

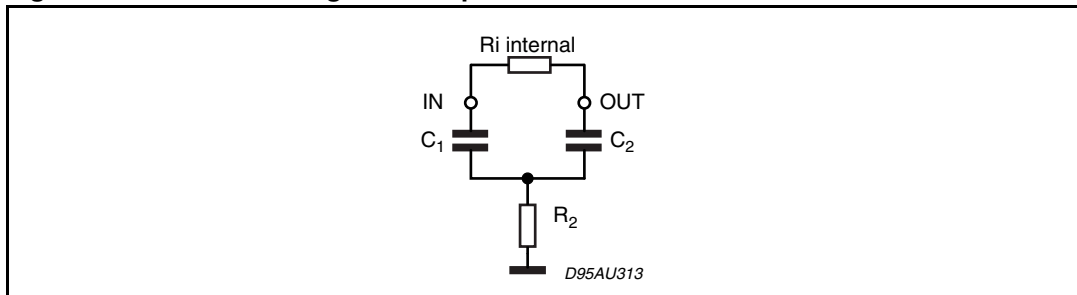
The bass and the mid-range cells have the same structure.

However, the bass cell has an internal resistor  $R_B$  of typically 44 k $\Omega$  whilst the mid-range cell has an internal resistor  $R_M$  of typically 25 k $\Omega$ .

Several filter types can be implemented by connecting external components to the bass/mid IN and OUT pins.

Typical responses are shown in [Figure 8](#), [Figure 9](#) and [Figure 11](#).

**Figure 4. Bass/mid-range filter implementation**



[Figure 4.](#) refers to the basic T-type band-pass filter. Starting from the filter component values ( $R_1$  (internal) and  $R_2$ ,  $C_1$ ,  $C_2$  (external)) then the centre frequency  $f_C$ , the gain  $A_v$  at maximum boost and the filter Q factor are computed as follows:

$$f_C = \frac{1}{2 \cdot \pi \cdot \sqrt{R_1 \cdot R_2 \cdot C_1 \cdot C_2}}$$

$$A_v = \frac{R_2 C_2 + R_2 C_1 + R_i C_1}{R_2 C_1 + R_2 C_2}$$

$$Q = \frac{\sqrt{R_1 \cdot R_2 \cdot C_1 \cdot C_2}}{R_2 C_1 + R_2 C_2}$$

Transposing and solving for the external components we get:

$$C1 = \frac{A_V - 1}{2 \cdot \pi \cdot F_c \cdot R_i \cdot Q}$$

$$C2 = \frac{Q^2 \cdot C1}{A_V - 1 - Q^2}$$

$$R2 = \frac{A_V - 1 - Q^2}{2 \cdot \pi \cdot C1 \cdot F_c \cdot (A_V - 1) \cdot Q}$$

### 3.1.2 Treble stage

The treble stage is a high-pass filter whose time constant is fixed by an internal resistor (25 kΩ typically) and an external capacitor connected between treble pins and ground.

Typical responses are shown in [Figure 10](#) and [Figure 11](#).

### 3.2 Pin CREF

The suggested value of 10 μF for the reference capacitor (C<sub>REF</sub>), connected to pin CREF, can be reduced to 4.7 μF if the application requires faster power-on.

### 3.3 Electrical characteristics

Figure 5. THD vs frequency

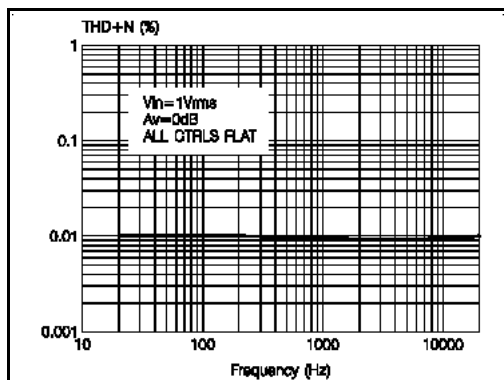
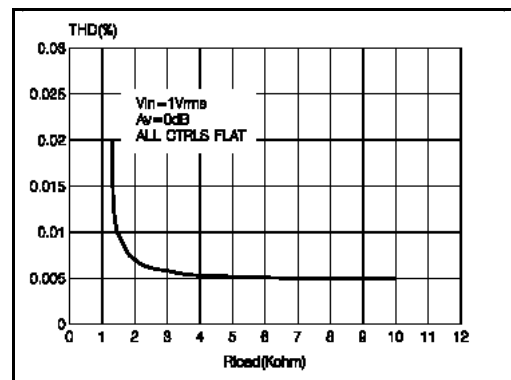


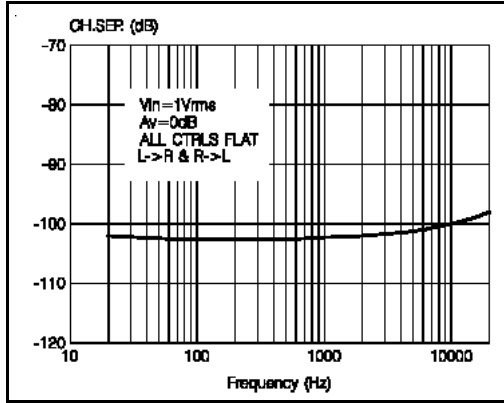
Figure 6. THD vs R<sub>LOAD</sub>



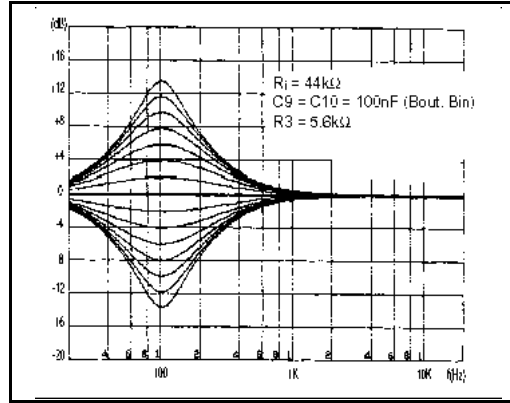
Application suggestions

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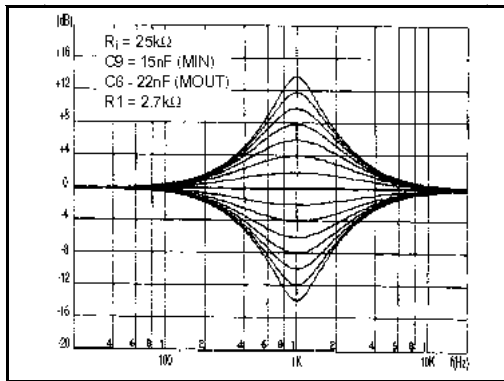
**Figure 7. Channel separation vs frequency**



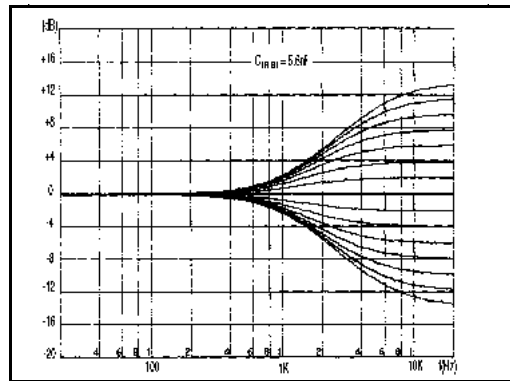
**Figure 8. Bass filter response**



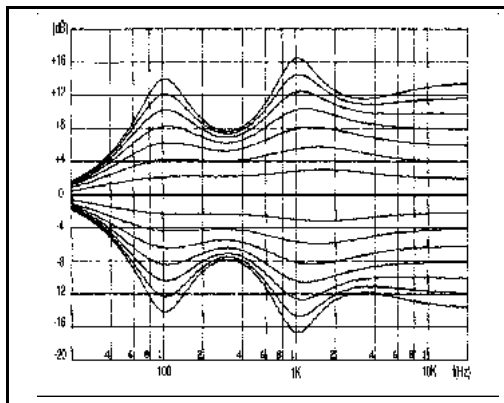
**Figure 9. Mid-range filter response**



**Figure 10. Treble filter response**



**Figure 11. Typical tone response**



## 4 I<sup>2</sup>C bus interface

Data transmission from the microprocessor to the TDA7439DS and vice versa takes place through the 2-wire I<sup>2</sup>C bus interface. This consists of the data and clock lines, SDA and SCL. Pull-up resistors to the positive supply voltage must be used (there are no internal pull-ups).

### 4.1 Data validity

The data on the SDA line must be stable during the high period of the clock as shown in [Figure 12](#). SDA is allowed to change only when SCL is low.

### 4.2 Start and stop conditions

As shown in [Figure 13](#) a start condition is a high to low transition of SDA while SCL is high. The stop condition is a low to high transition of SDA while SCL is high.

### 4.3 Byte format

Every byte transferred on the SDA line must contain 8 bits. The MSB is transferred first. There is also provision for an acknowledge bit to follow each byte to indicate that the data has been received.

### 4.4 Acknowledge

The master ( $\mu$ P) puts a resistive high level on SDA during the acknowledge clock pulse (see [Figure 14](#)). The peripheral (audio processor) that acknowledges has to pull down (low) the SDA line during this clock pulse.

The audio processor which has been addressed has to generate an acknowledge after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse time. In this case the master transmitter can generate the STOP information in order to abort the transfer.

### 4.5 Transmission without acknowledge

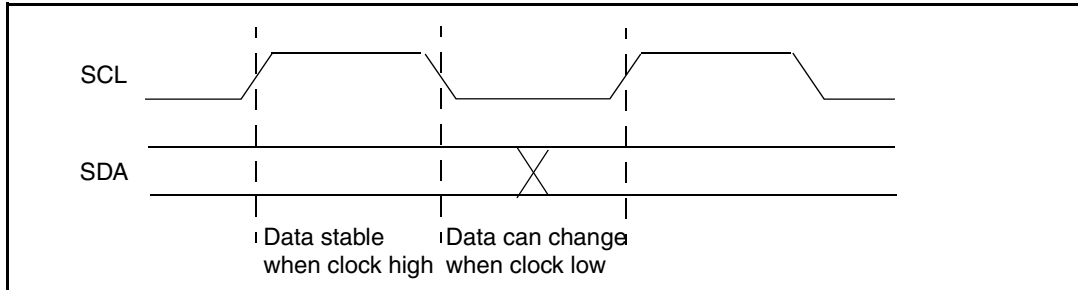
Suppressing the audio processor acknowledge detection enables the  $\mu$ P to use a simpler transmission: it simply waits for one clock, without checking the slave acknowledging, and then sends the new data.

This approach has, of course, less protection from transmission errors.

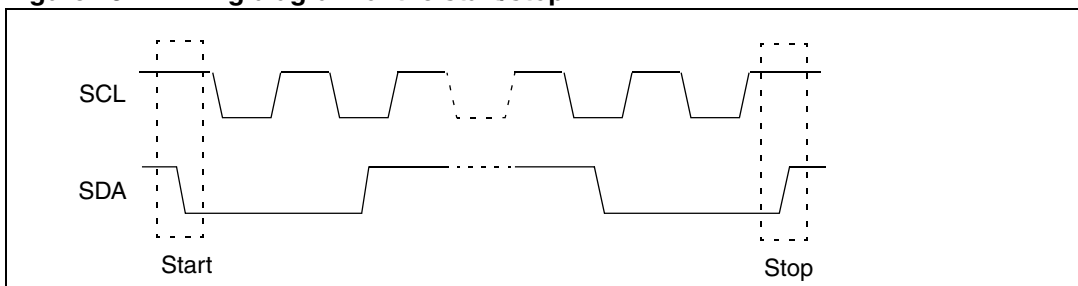
**I<sup>2</sup>C bus interface**

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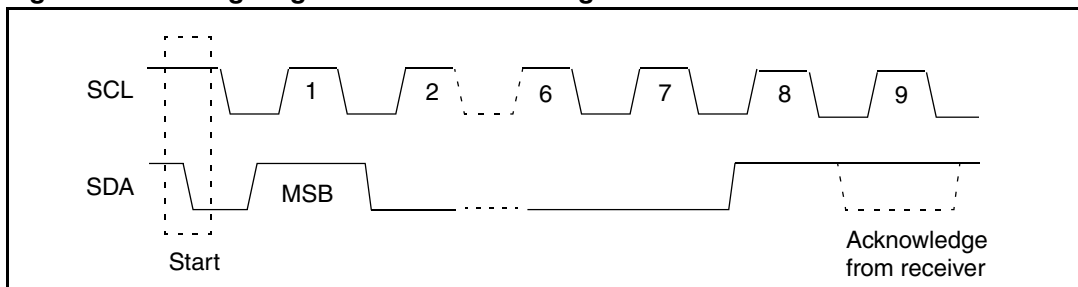
**Figure 12. Timing diagram of the data on the I<sup>2</sup>C bus**



**Figure 13. Timing diagram of the start/stop**



**Figure 14. Timing diagram of the acknowledge**

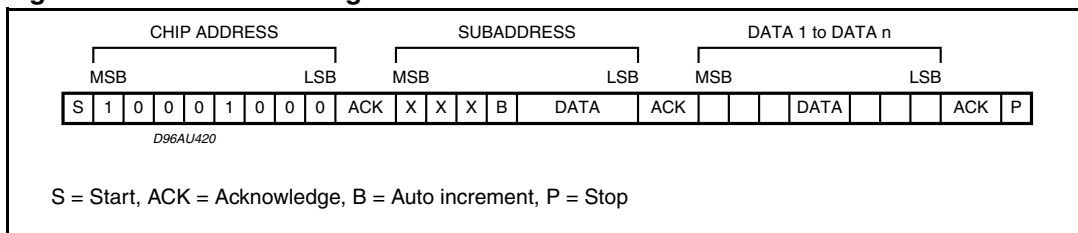


**4.6 Interface protocol**

The interface protocol comprises:

- a start condition (S)
- a chip-address byte, containing the TDA7439DS address
- a sub-address byte including an auto address-increment bit
- a sequence of data bytes (N bytes + acknowledge)
- a stop condition (P).

**Figure 15. SDA addressing and data**

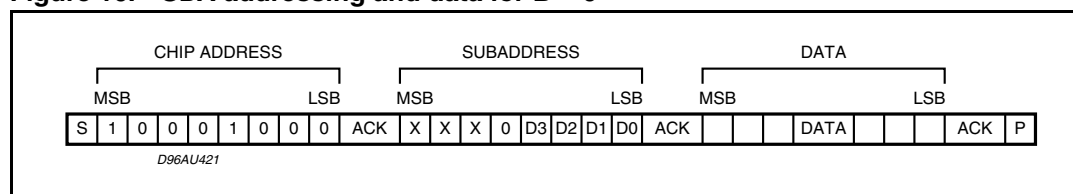


## 5 I<sup>2</sup>C bus transmission examples

### 5.1 No address incrementing

The TDA7439DS receives a start condition followed by the correct chip address, then a sub address with the bit B = 0 (for no address increment), then the data bytes to be sent to the sub address and finally a stop condition.

Figure 16. SDA addressing and data for B = 0



### 5.2 Address incrementing

The TDA7439DS receives a start condition followed by the correct chip address, then a sub address with the B = 1 for address incrementing; now it is in a loop condition with an automatic increase of the sub address up to D[3:0] = 0x7. That is, the data for sub addresses from D[3:0] = 1000 (binary) to 1111 are ignored.

In [Figure 17](#) below, DATA1 is directed to the sub address sent (that is, D[3:0]), DATA2 is directed to the sub address incremented by 1 (that is, 1 + D[3:0]) and so forth until a stop condition is received to terminate the transmission.

Figure 17. SDA addressing and data for B = 1

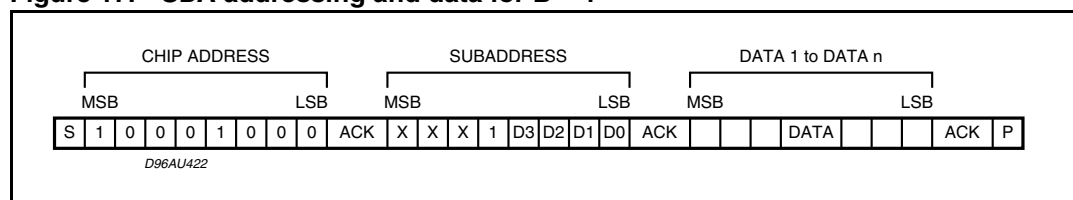


Table 6. Power-on-reset conditions

Parameter	POR value
Input selection	IN2
Input gain	28 dB
Volume	MUTE
Bass	0 dB
Mid-range	2 dB
Treble	2 dB
Speaker	MUTE

## 6 I<sup>2</sup>C bus addresses and data

### 6.1 Chip address byte

The TDA7439DS chip address is 0x88.

### 6.2 Sub-address byte

The function is selected by the 4-bit sub address as given in [Table 7](#). The three MSBs are not used and bit D4 selects address incrementing (B = 1) or single data byte (B = 0).

**Table 7. Function selection: sub-address byte**

MSB								LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0		
X	X	X	B	0	0	0	0	Input selector	
X	X	X	B	0	0	0	1	Input gain	
X	X	X	B	0	0	1	0	Volume	
X	X	X	B	0	0	1	1	Bass gain	
X	X	X	B	0	1	0	0	Mid-range gain	
X	X	X	B	0	1	0	1	Treble gain	
X	X	X	B	0	1	1	0	Speaker attenuation, R	
X	X	X	B	0	1	1	1	Speaker attenuation, L	

### 6.3 Data bytes

The function value is changed by the data byte as given in the following tables, [Table 8](#) to [Table 14](#).

In the tables of input gain, volume and attenuation, not all values are shown. A desired intermediate value is obtained by setting the three LSBs to the appropriate value.

**Table 8. Input selector value (sub address 0x0)**

MSB								LSB	Input multiplexer
D7	D6	D5	D4	D3	D2	D1	D0		
X	X	X	X	X	X	0	0	IN4	
X	X	X	X	X	X	0	1	IN3	
X	X	X	X	X	X	1	0	IN2	
X	X	X	X	X	X	1	1	IN1	

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I<sup>2</sup>C bus addresses and data

Table 9. Input gain value (sub address 0x1)

MSB							LSB	Input gain 2-dB steps
D7	D6	D5	D4	D3	D2	D1	D0	
X	X	X	X	0	0	0	0	0 dB
X	X	X	X	0	0	0	1	2 dB
X	X	X	X	0	0	1	0	4 dB
X	X	X	X	0	0	1	1	6 dB
X	X	X	X	0	1	0	0	8 dB
X	X	X	X	0	1	0	1	10 dB
X	X	X	X	0	1	1	0	12 dB
X	X	X	X	0	1	1	1	14 dB
X	X	X	X	1	0	0	0	16 dB
X	X	X	X	1	0	0	1	18 dB
X	X	X	X	1	0	1	0	20 dB
X	X	X	X	1	0	1	1	22 dB
X	X	X	X	1	1	0	0	24 dB
X	X	X	X	1	1	0	1	26 dB
X	X	X	X	1	1	1	0	28 dB
X	X	X	X	1	1	1	1	30 dB

Table 10. Volume value (sub address 0x2)

MSB							LSB	Volume 1-dB steps
D7	D6	D5	D4	D3	D2	D1	D0	
X	0	0	0	0	0	0	0	0 dB
X	0	0	0	0	0	0	1	-1 dB
X	0	0	0	0	0	1	0	-2 dB
X	0	0	0	0	0	1	1	-3 dB
X	0	0	0	0	1	0	0	-4 dB
X	0	0	0	0	1	0	1	-5 dB
X	0	0	0	0	1	1	0	-6 dB
X	0	0	0	0	1	1	1	-7 dB
X	0	0	0	1	0	0	0	-8 dB
X	0	0	1	0	0	0	0	-16 dB
X	0	0	1	1	0	0	0	-24 dB
X	0	1	0	0	0	0	0	-32 dB
X	0	1	0	1	0	0	0	-40 dB
X	X	1	1	1	X	X	X	MUTE



I<sup>2</sup>C bus addresses and data

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Table 11. Bass gain value (sub address 0x3)

MSB							LSB	Bass gain 2-dB steps
D7	D6	D5	D4	D3	D2	D1	D0	
X	X	X	X	0	0	0	0	-14 dB
X	X	X	X	0	0	0	1	-12 dB
X	X	X	X	0	0	1	0	-10 dB
X	X	X	X	0	0	1	1	-8 dB
X	X	X	X	0	1	0	0	-6 dB
X	X	X	X	0	1	0	1	-4 dB
X	X	X	X	0	1	1	0	-2 dB
X	X	X	X	X	1	1	1	0 dB
X	X	X	X	1	1	1	0	2 dB
X	X	X	X	1	1	0	1	4 dB
X	X	X	X	1	1	0	0	6 dB
X	X	X	X	1	0	1	1	8 dB
X	X	X	X	1	0	1	0	10 dB
X	X	X	X	1	0	0	1	12 dB
X	X	X	X	1	0	0	0	14 dB

Table 12. Mid-range gain value (sub address 0x4)

MSB							LSB	Mid-range gain 2-dB steps
D7	D6	D5	D4	D3	D2	D1	D0	
X	X	X	X	0	0	0	0	-14 dB
X	X	X	X	0	0	0	1	-12 dB
X	X	X	X	0	0	1	0	-10 dB
X	X	X	X	0	0	1	1	-8 dB
X	X	X	X	0	1	0	0	-6 dB
X	X	X	X	0	1	0	1	-4 dB
X	X	X	X	0	1	1	0	-2 dB
X	X	X	X	X	1	1	1	0 dB
X	X	X	X	1	1	1	0	2 dB
X	X	X	X	1	1	0	1	4 dB
X	X	X	X	1	1	0	0	6 dB
X	X	X	X	1	0	1	1	8 dB
X	X	X	X	1	0	1	0	10 dB
X	X	X	X	1	0	0	1	12 dB
X	X	X	X	1	0	0	0	14 dB

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I<sup>2</sup>C bus addresses and data

Table 13. Treble gain value (sub address 0x5)

MSB							LSB	Treble gain 2-dB steps
D7	D6	D5	D4	D3	D2	D1	D0	
X	X	X	X	0	0	0	0	-14 dB
X	X	X	X	0	0	0	1	-12 dB
X	X	X	X	0	0	1	0	-10 dB
X	X	X	X	0	0	1	1	-8 dB
X	X	X	X	0	1	0	0	-6 dB
X	X	X	X	0	1	0	1	-4 dB
X	X	X	X	0	1	1	0	-2d B
X	X	X	X	X	1	1	1	0 dB
X	X	X	X	1	1	1	0	2 dB
X	X	X	X	1	1	0	1	4 dB
X	X	X	X	1	1	0	0	6 dB
X	X	X	X	1	0	1	1	8 dB
X	X	X	X	1	0	1	0	10 dB
X	X	X	X	1	0	0	1	12 dB
X	X	X	X	1	0	0	0	14 dB

Table 14. Speaker attenuation value (sub address 0x6, 0x7)

MSB							LSB	Speaker attenuation 1-dB steps
D7	D6	D5	D4	D3	D2	D1	D0	
X	0	0	0	0	0	0	0	0 dB
X	0	0	0	0	0	0	1	1 dB
X	0	0	0	0	0	1	0	2 dB
X	0	0	0	0	0	1	1	3 dB
X	0	0	0	0	1	0	0	4 dB
X	0	0	0	0	1	0	1	5 dB
X	0	0	0	0	1	1	0	6 dB
X	0	0	0	0	1	1	1	7 dB
X	0	0	0	1	0	0	0	8 dB
X	0	0	1	0	0	0	0	16 dB
X	0	0	1	1	0	0	0	24 dB
X	0	1	0	0	0	0	0	32 dB
X	0	1	0	1	0	0	0	40 dB
X	0	1	1	0	0	0	0	48 dB
X	0	1	1	1	0	0	0	56 dB

I<sup>2</sup>C bus addresses and data

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Table 14. Speaker attenuation value (sub address 0x6, 0x7) (continued)

MSB							LSB	Speaker attenuation 1-dB steps
D7	D6	D5	D4	D3	D2	D1	D0	
X	1	0	0	0	0	0	0	64 dB
X	1	0	0	1	0	0	0	72 dB
X	1	1	1	1	X	X	X	MUTE

## 7 Chip input/output circuits

Figure 18. Pin 23

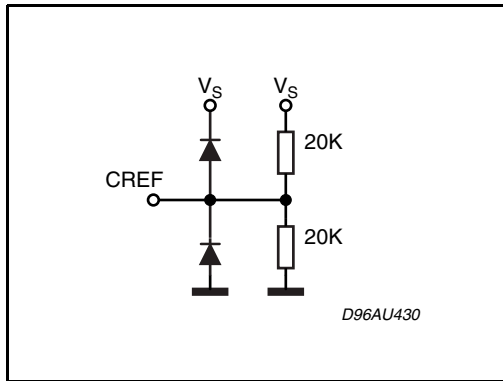


Figure 19. Pins 26, 27

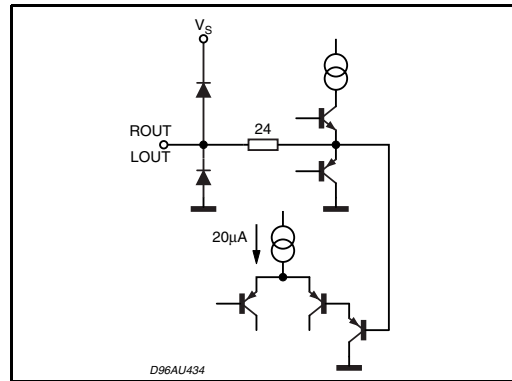


Figure 20. Pins 1, 2, 3, 4, 5, 6, 7, 28

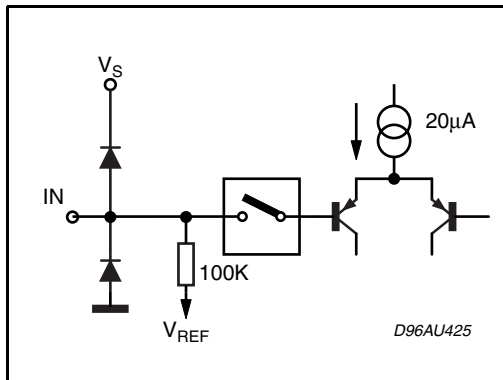


Figure 21. Pins 8, 9

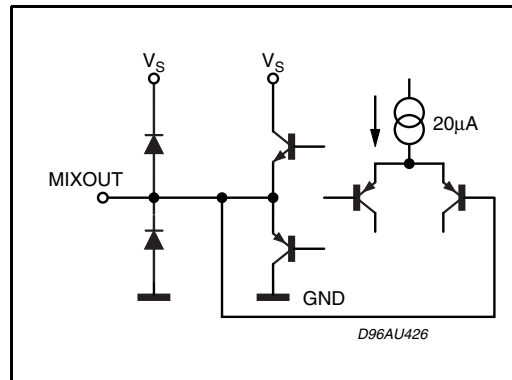


Figure 22. Pins 11, 16

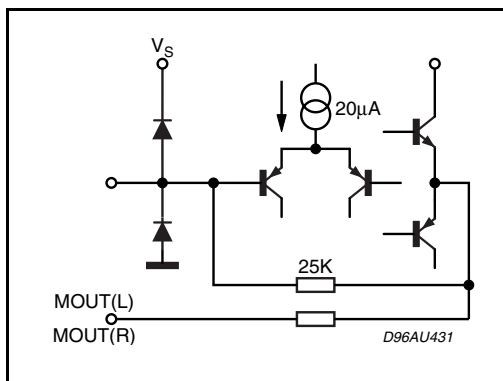
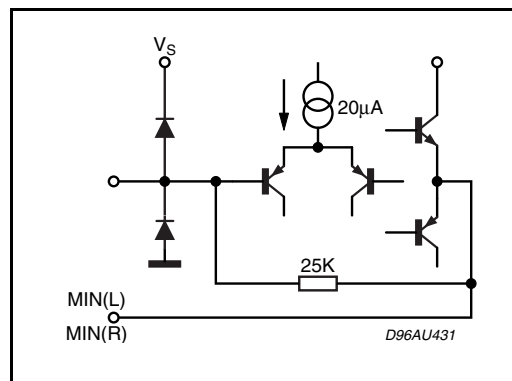


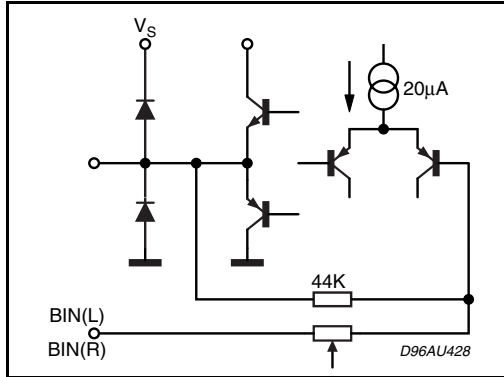
Figure 23. Pins 10, 17



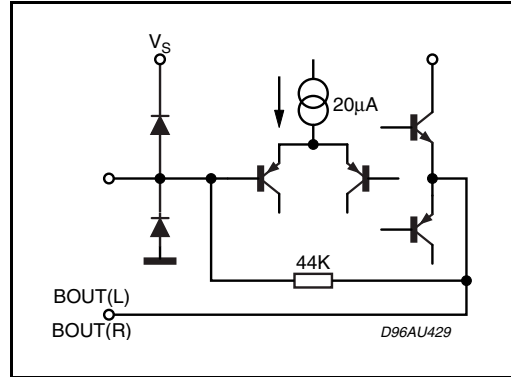
**Chip input/output circuits**

**TDA7439DS**

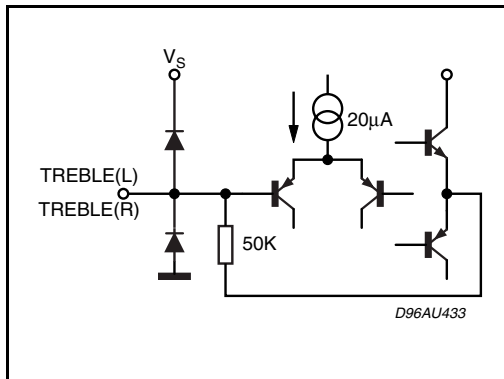
**Figure 24. Pins 12, 14**



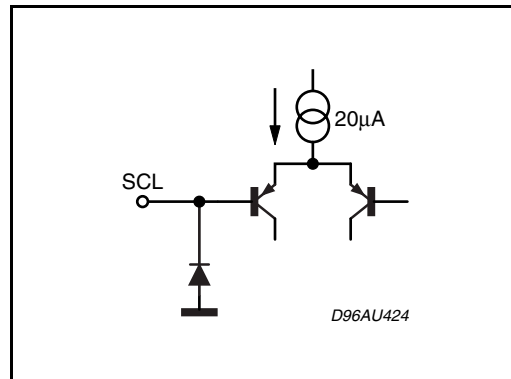
**Figure 25. Pins 13, 15**



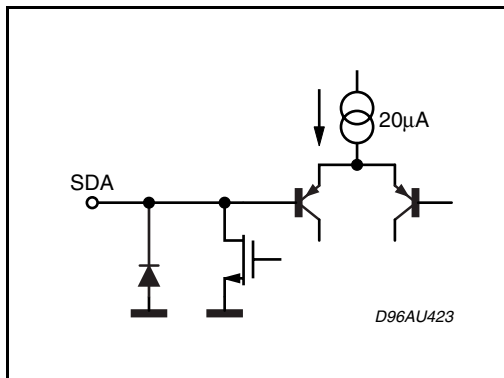
**Figure 26. Pins 18, 19**



**Figure 27. Pin 21**



**Figure 28. Pin 22**

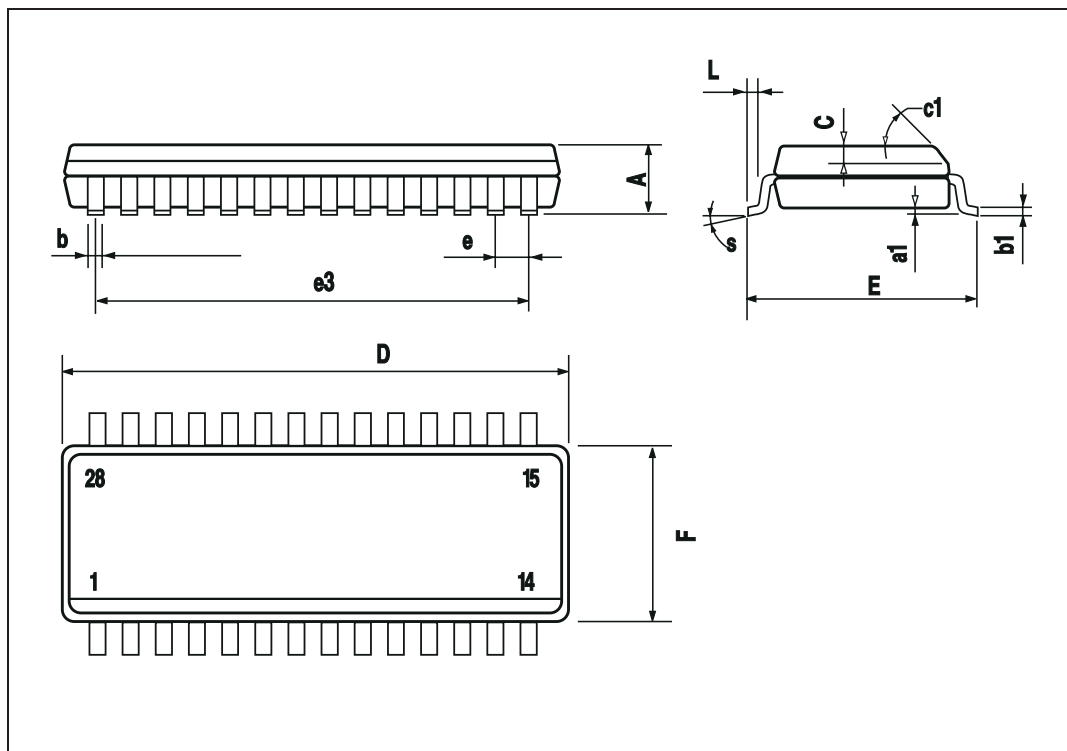
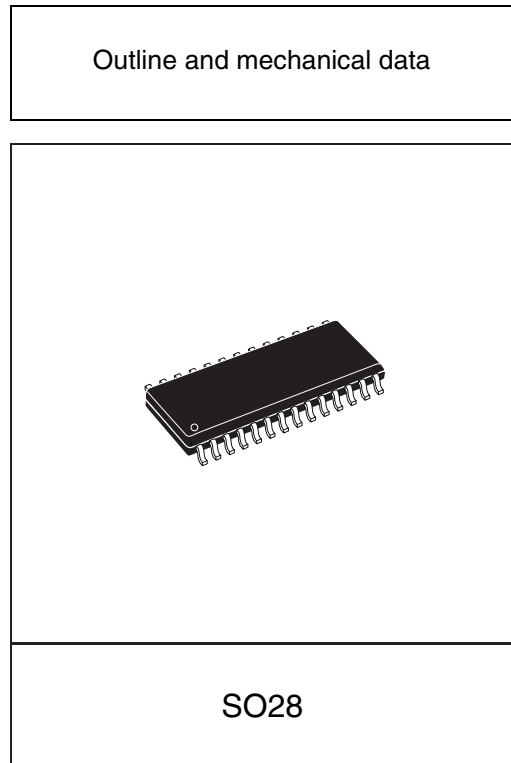


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Package information

8 Package information

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (typ.)					
D	17.7		18.1	0.697		0.713
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		16.51			0.65	
F	7.4		7.6	0.291		0.299
L	0.4		1.27	0.016		0.050
S	8° (max.)					



## 9 Revision history

Table 15. Document revision history

Date	Revision	Changes
Jan-2004	1	Initial release
Jun-2004	2	Modified presentation
14-Nov-2007	3	Updated titles to <i>Figure 9</i> and <i>Figure 10</i> Minor updates to presentation
20-Nov-2007	4	Updated <i>Figure 23</i> and <i>Figure 27</i>

## TDA7439DS

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