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FEATURES

- High-Performance Static CMOS Technology
- TMS470R1x 16/32-Bit RISC Core (ARM7TDMI™)
 - 24-MHz System Clock (48-MHz Pipeline Mode)
 - Independent 16/32-Bit Instruction Set
 - Open Architecture With Third-Party Support
 - Built-In Debug Module
 - Big-Endian Format Utilized
- Integrated Memory
 - 256K-Byte Program Flash
 - One Bank With 14 Contiguous Sectors
 - Internal State Machine for Programming and Erase
 - 12K-Byte Static RAM (SRAM)
- Operating Features
 - Core Supply Voltage (V_{CC}): 1.81 V–2.05 V
 - I/O Supply Voltage (V_{CCIO}): 3.0 V–3.6 V
 - Low-Power Modes: STANDBY and HALT
 - Extended Industrial Temperature Ranges
- 470+ System Module
 - 32-Bit Address Space Decoding
 - Bus Supervision for Memory and Peripherals
 - Analog Watchdog (AWD) Timer
 - Real-Time Interrupt (RTI)
 - System Integrity and Failure Detection
- Zero-Pin Phase-Locked Loop (ZPLL)-Based Clock Module With Prescaler
 - Multiply-by-4 or -8 Internal ZPLL Option
 - ZPLL Bypass Mode
- Six Communication Interfaces:
 - Two Serial Peripheral Interfaces (SPIs)
 - 255 Programmable Baud Rates
 - Two Serial Communications Interfaces (SCIs)
 - 2²⁴ Selectable Baud Rates
 - Asynchronous/Isosynchronous Modes
 - Standard CAN Controller (SCC)
 - 16-Mailbox Capacity
 - Fully Compliant With CAN Protocol, Version 2.0B
 - Class II Serial Interface (C2SIB)
 - Two Selectable Data Rates
 - Normal Mode 10.4 Kbps and 4X Mode 41.6 Kbps
- High-End Timer (HET)
 - 16 Programmable I/O Channels:
 - 14 High-Resolution Pins
 - 2 Standard-Resolution Pins
 - High-Resolution Share Feature (XOR)
 - High-End Timer RAM
 - 64-Instruction Capacity
- 10-Bit Multi-Buffered ADC (MibADC) 16-Channel
 - 64-Word FIFO Buffer
 - Single- or Continuous-Conversion Modes
 - 1.55 μ s Minimum Sample and Conversion Time
 - Calibration Mode and Self-Test Features
- 8 External Interrupts
- Flexible Interrupt Handling
- 11 Dedicated GIO Pins, 1 Input-Only GIO Pin, and 38 Additional Peripheral I/Os (A256)
- External Clock Prescale (ECP) Module
 - Programmable Low-Frequency External Clock (CLK)
- Compatible ROM Device
- On-Chip Scan-Base Emulation Logic, IEEE Standard 1149.1 (JTAG) Test-Access Port ⁽¹⁾
- 100-Pin Plastic Low-Profile Quad Flatpack (PZ Suffix)

(1) The test-access port is compatible with the IEEE Standard 1149.1-1990, IEEE Standard Test-Access Port and Boundary Scan Architecture. Boundary scan is not supported on this device.



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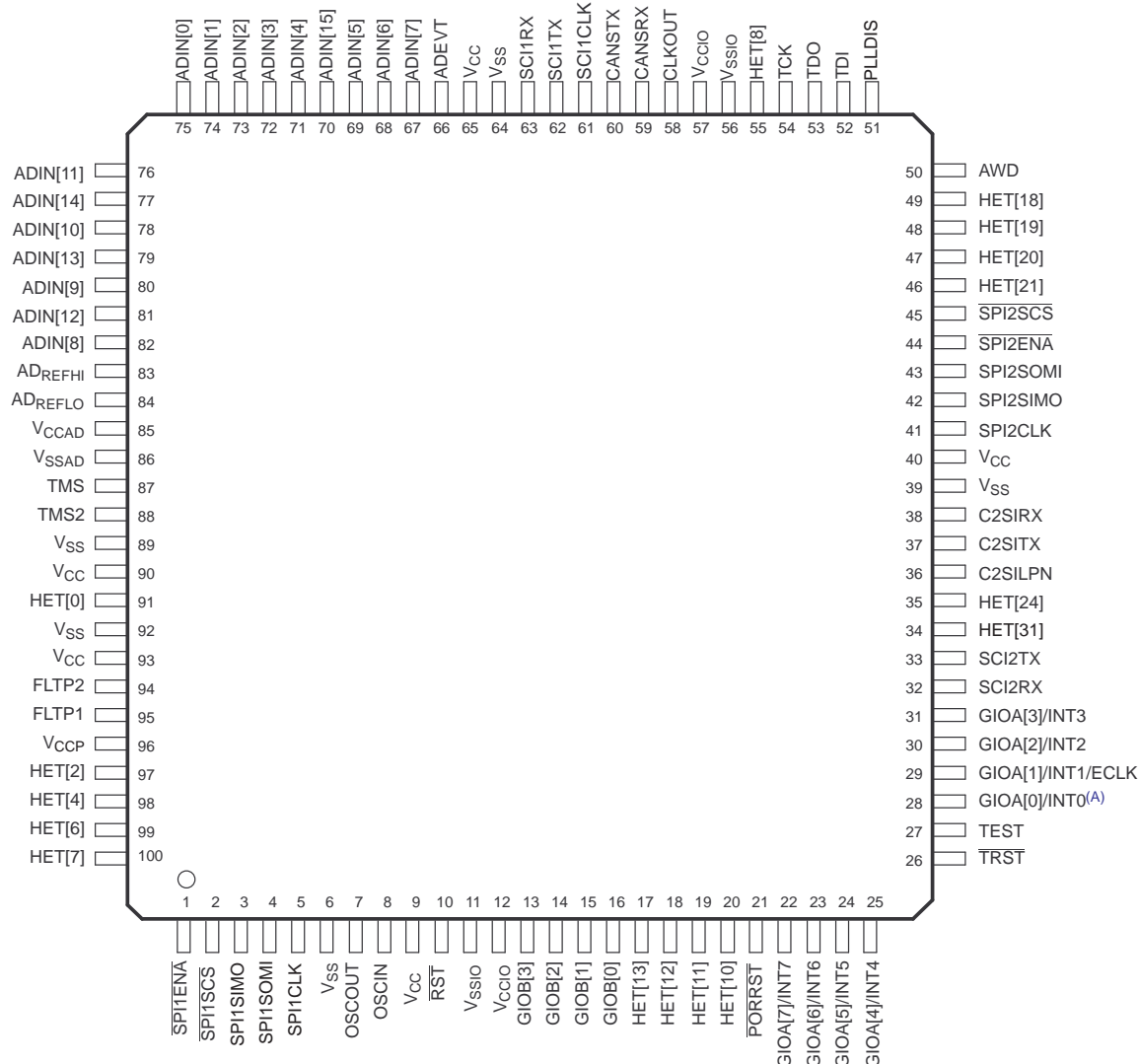
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TMS470R1A256 16/32-Bit RISC Flash Microcontroller

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TMS470R1A256 100-PIN PZ PACKAGE (TOP VIEW)



A. GIOA[0]/INT0 (pin 28) is an input-only GIO pin.

DESCRIPTION

The TMS470R1A256⁽²⁾ devices are members of the Texas Instruments TMS470R1x family of general-purpose 16/32-bit reduced instruction set computer (RISC) microcontrollers. The A256 microcontroller offers high performance utilizing the high-speed ARM7TDMI 16/32-bit RISC central processing unit (CPU), resulting in a high instruction throughput while maintaining greater code efficiency. The ARM7TDMI 16/32-bit RISC CPU views memory as a linear collection of bytes numbered upwards from 0. The TMS470R1A256 utilizes the big-endian format where the most significant byte of a word is stored at the lowest numbered byte and the least significant byte at the highest numbered byte.

High-end embedded control applications demand more performance from their controllers while maintaining low costs. The A256 RISC core architecture offers solutions to these performance and cost demands while maintaining low power consumption.

(2) Throughout the remainder of this document, the TMS470R1A256 device name will be referred to as either the full device name, TMS470R1A256, or as A256.

The A256 device contains the following:

- ARM7TDMI 16/32-Bit RISC CPU
- TMS470R1x system module (SYS) with 470+ enhancements
- 256K-byte flash
- 12K-byte SRAM
- Zero-pin phase-locked loop (ZPLL) clock module
- Analog watchdog (AWD) timer
- Real-time interrupt (RTI) module
- Two serial peripheral interface (SPI) modules
- Two serial communications interface (SCI) modules
- Standard CAN controller (SCC)
- Class II serial interface (C2S1b)
- 10-bit multi-buffered analog-to-digital converter (MibADC), 16-input channels
- High-end timer (HET) controlling 16 I/Os
- External clock prescale (ECP) module
- Up to 49 I/O pins and 1 input-only pin

The functions performed by the 470+ system module (SYS) include:

- Address decoding
- Memory protection
- Memory and peripherals bus supervision
- Reset and abort exception management
- Prioritization for all internal interrupt sources
- Device clock control
- Parallel signature analysis (PSA)
- This data sheet includes device-specific information such as memory and peripheral select assignment, interrupt priority, and a device memory map. For a more detailed functional description of the SYS module, see the *TMS470R1x System Module Reference Guide* (literature number SPNU189).

The A256 memory includes general-purpose SRAM supporting single-cycle read/write accesses in byte, half-word, and word modes.

The flash memory on this device is a nonvolatile, electrically erasable and programmable memory implemented with a 32-bit-wide data bus interface. In pipeline mode, the flash operates with a system clock frequency of up to 48 MHz. In normal mode, the flash operates with a system clock frequency of up to 24 MHz. For more detailed information on the flash, see the *F05 flash* section of this data sheet and the *TMS470R1x F05 Flash Reference Guide* (literature number SPNU213).

The A256 device has six communication interfaces: two SPIs, two SCIs, an SCC, and a C2S1b. The SPI provides a convenient method of serial interaction for high-speed communications between similar shift-register type devices. The SCI is a full-duplex, serial I/O interface intended for asynchronous communication between the CPU and other peripherals using the standard non-return-to-zero (NRZ) format. The SCC uses a serial, multimaster communication protocol that efficiently supports distributed real-time control with robust communication rates of up to 1 megabit per second (Mbps). The SCC is ideal for applications operating in noisy and harsh environments (e.g., industrial fields) that require reliable serial communication or multiplexed wiring. The C2S1b allows the A256 to transmit and receive messages on a class II network following an SAE J1850⁽³⁾ standard. For more detailed functional information on the SPI, SCI, and SCC peripherals, see the specific reference guides (literature numbers SPNU195, SPNU196, and SPNU197, respectively). For more detailed functional information on the C2S1b peripheral, see the *TMS470R1x Class II Serial Interface B (C2S1b) Reference Guide* (literature number SPNU214).

(3) SAE Standard J1850 Class B Data Communication Network Interface

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The HET is an advanced intelligent timer that provides sophisticated timing functions for real-time applications. The timer is software-controlled, using a reduced instruction set, with a specialized timer micromachine and an attached I/O port. The HET can be used for compare, capture, or general-purpose I/O. It is especially well suited for applications requiring multiple sensor information and drive actuators with complex and accurate time pulses. For more detailed functional information on the HET, see the *TMS470R1x High-End Timer (HET) Reference Guide* (literature number SPNU199).

The A256 HET peripheral contains the XOR-share feature. This feature allows two adjacent HET high-resolution channels to be XORed together, making it possible to output smaller pulses than a standard HET. For more detailed information on the HET XOR-share feature, see the *TMS470R1x High-End Timer (HET) Reference Guide* (literature number SPNU199).

The A256 device has a 10-bit-resolution sample-and-hold MibADC. The MibADC channels can be converted individually or can be grouped by software for sequential conversion sequences. There are three separate groupings, two of which are triggerable by an external event. Each sequence can be converted once when triggered or configured for continuous conversion mode. For more detailed functional information on the MibADC, see the *TMS470R1x Multi-Buffered Analog-to-Digital Converter (MibADC) Reference Guide* (literature number SPNU206).

The zero-pin phase-locked loop (ZPLL) clock module contains a phase-locked loop, a clock-monitor circuit, a clock-enable circuit, and a prescaler (with prescale values of 1–8). The function of the ZPLL is to multiply the external frequency reference to a higher frequency for internal use. The ZPLL provides ACLK to the system (SYS) module. The SYS module subsequently provides the system clock (SYSCLK), real-time interrupt clock (RTICLK), CPU clock (MCLK), and peripheral interface clock (ICLK) to all other A256 device modules. For more detailed functional information on the ZPLL, see the *TMS470R1x Zero-Pin Phase Locked Loop (ZPLL) Clock Module Reference Guide* (literature number SPNU212).

NOTE:

ACLK should not be confused with the MibADC internal clock, ADCLK. ACLK is the continuous system clock from an external resonator/crystal reference.

The A256 device also has an external clock prescaler (ECP) module that when enabled, outputs a continuous external clock (ECLK) on a specified GIO pin. The ECLK frequency is a user-programmable ratio of the peripheral interface clock (ICLK) frequency. For more detailed functional information on the ECP, see the *TMS470R1x External Clock Prescaler (ECP) Reference Guide* (literature number SPNU202).

Device Characteristics

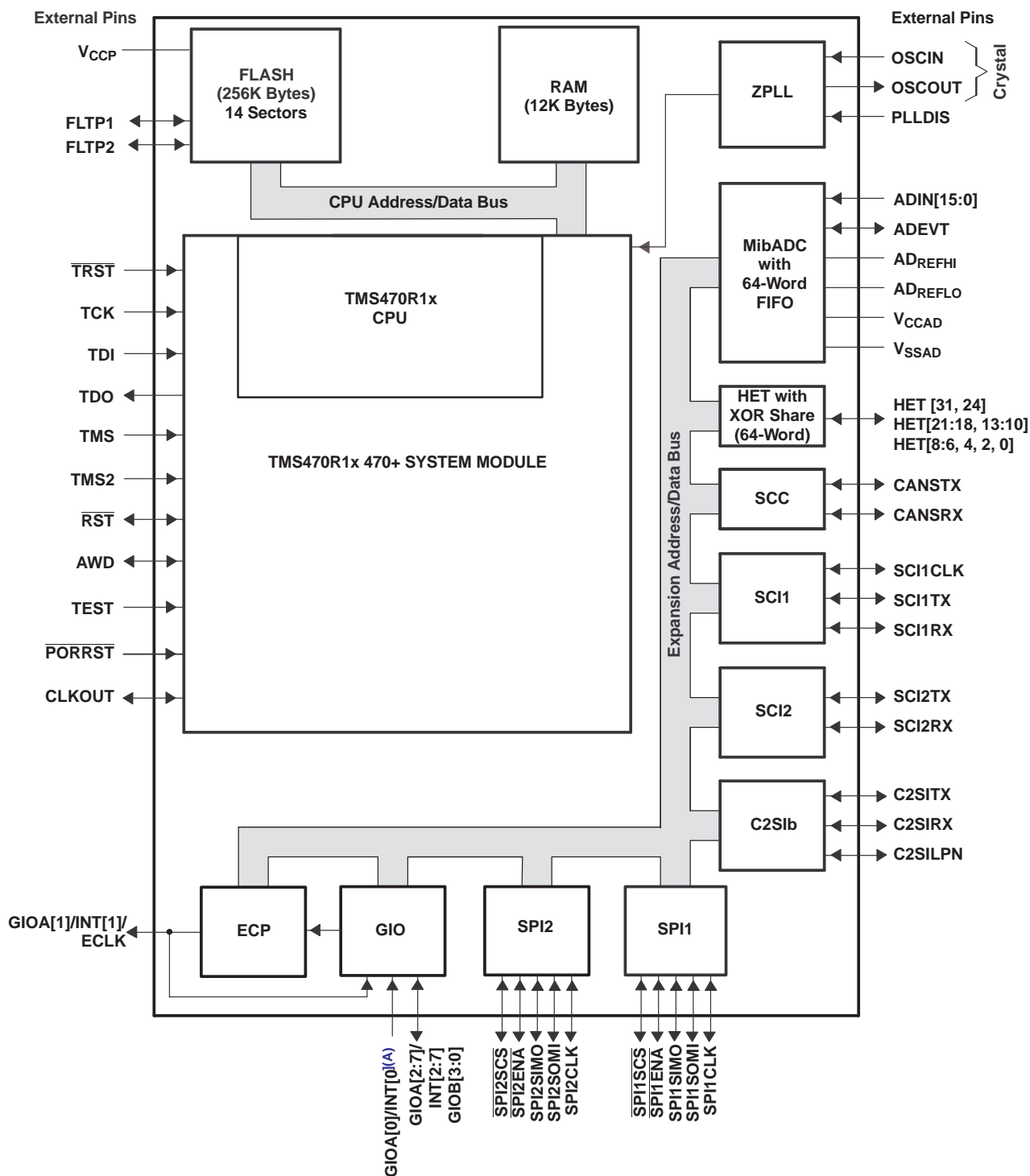
The TMS470R1A256 device is a derivative of the F05 system emulation device SE470R1VB8AD. Table 1 identifies all the characteristics of the TMS470R1A256 device except the SYSTEM and CPU, which are generic.

Table 1. Device Characteristics

| CHARACTERISTICS | DEVICE DESCRIPTION | COMMENTS |
|--|------------------------------------|--|
| MEMORY | | |
| For the number of memory selects on this device, see the "Memory Selection Assignment" table (Table 2). | | |
| INTERNAL MEMORY | 256K-Byte flash 12K-Byte SRAM | Flash is pipeline-capable. The A256 RAM is implemented in one 12K array selected by two memory-select signals (see the "Memory Selection Assignment" table, Table 2). |
| PERIPHERALS | | |
| For the device-specific interrupt priority configurations, see the "Interrupt Priority" table (Table 4). For the 1K peripheral address ranges and their peripheral selects, see the "A256 Peripherals, System Module, and Flash Base Addresses" table (Table 3). | | |
| CLOCK | ZPLL | Zero-pin PLL has no external loop filter pins. |
| GENERAL-PURPOSE I/Os | 11 I/O 1 Input only | Port A has 8 external pins and Port B has 4 external pins. |
| ECP | YES | |
| C2S1b | 1 | |
| SCI | 1 (3-pin) 1 (2-pin) | SCI2 has no external clock pin, only transmit/receive pins (SCI2TX and SCI2RX) |
| CAN (HECC and/or SCC) | 1 SCC | Standard CAN controller |
| SPI (5-pin, 4-pin or 3-pin) | 2 (5-pin) | |
| HET with XOR Share | 16 I/O | The A256 devices have both the logic and registers for a full 32-I/O HET to be implemented, even though not all 32 pins are available externally. The high-resolution (HR) SHARE feature allows even HR pins to share the next higher odd-numbered HR pin structures. This HR sharing is independent of whether or not the odd pin is available externally. If an odd pin is available externally and shared, then the odd pin can only be used as a general-purpose I/O. For more information on HR SHARE, see the <i>TMS470R1x High-End Timer (HET) Reference Guide</i> (literature number SPNU199). |
| HET RAM | 64-Instruction Capacity | |
| MibADC | 10-bit, 16-channel 64-word FIFO | Both the logic and registers for a full 16-channel MibADC are present. The MibADC is capable of being event-triggered from a user-selectable event source. |
| CORE VOLTAGE | 1.81–2.05 V | |
| I/O VOLTAGE | 3.0–3.6 V | |
| PINS | 100 | |
| PACKAGE | PZ | |

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Functional Block Diagram



A. GIOA[0]/INT[0] is an input-only GIO pin.

Table 2. Terminal Functions

| TERMINAL | | TYPE ⁽¹⁾⁽²⁾ | INTERNAL PULLUP/ PULLDOWN ⁽³⁾ | DESCRIPTION |
|-----------------------------------|---------------|------------------------|--|---|
| NAME | PIN NUMBER | | | |
| HIGH-END TIMER (HET) | | | | |
| HET[0] | 91 | 3.3-V I/O | IPD | <p>The A256 devices have both the logic and registers for a full 32-I/O HET implemented, even though not all 32 pins are available externally</p> <p>Timer input capture or output compare. The HET[31:0] applicable pins can be programmed as general-purpose input/output (GIO) pins.</p> <p>HET[21:18, 13:10, 8:6, 4, 2, 0] are high-resolution pins and HET[31, 24] are standard-resolution pins for A256.</p> <p>The high-resolution (HR) SHARE feature allows even-numbered HR pins to share the next higher odd-numbered HR pin structures. This HR sharing is independent of whether or not the odd pin is available externally. If an odd pin is available externally and shared, then the odd pin can only be used as a general-purpose I/O. For more information on HR SHARE, see the <i>TMS470R1x High-End Timer (HET) Reference Guide</i> (literature number SPNU199).</p> <p>The HET[19] or HET[18] pins can also be used as a user-selectable event source to event trigger the MibADC event group or group1 if the associated register source bits are properly configured and defined. For the internal device connections, see the MibADC section of this data sheet. For more detailed functional information on the MibADC, see the <i>TMS470R1x Multi-Buffered Analog-to-Digital Converter (MibADC) Reference Guide</i> (literature number SPNU206).</p> |
| HET[1] | - | | | |
| HET[2] | 97 | | | |
| HET[3] | - | | | |
| HET[4] | 98 | | | |
| HET[5] | - | | | |
| HET[6] | 99 | | | |
| HET[7] | 100 | | | |
| HET[8] | 55 | | | |
| HET[9] | - | | | |
| HET[10] | 20 | | | |
| HET[11] | 19 | | | |
| HET[12] | 18 | | | |
| HET[13] | 17 | | | |
| HET[14] | - | | | |
| HET[15] | - | | | |
| HET[16] | - | | | |
| HET[17] | - | | | |
| HET[18] | 49 | | | |
| HET[19] | 48 | | | |
| HET[20] | 47 | | | |
| HET[21] | 46 | | | |
| HET[22] | - | | | |
| HET[24] | 35 | | | |
| HET[28] | - | | | |
| HET[29] | - | | | |
| HET[30] | - | | | |
| HET[31] | 34 | | | |
| STANDARD CAN CONTROLLER (SCC) | | | | |
| CANSRX | 59 | 3.3-V I/O | | SCC receive pin or GIO pin |
| CANSTX | 60 | 3.3-V I/O | IPU | SCC transmit pin or GIO pin |
| CLASS II SERIAL INTERFACE (C2Sib) | | | | |
| C2SILPN | 36 | 3.3-V I/O | IPD | C2Sib module loopback enable pin or GIO pin |
| C2SIRX | 38 | 3.3-V I/O | | C2Sib module receive data input pin or GIO pin |
| C2SITX | 37 | 3.3-V I/O | IPD | C2Sib module transmit data output pin or GIO pin |

(1) I = input, O = output, PWR = power, GND = ground, REF = reference voltage, NC = no connect

(2) All I/O pins, except $\overline{\text{RST}}$, are configured as inputs while $\overline{\text{PORRST}}$ is low and immediately after $\overline{\text{PORRST}}$ goes high.

(3) IPD = internal pulldown, IPU = internal pullup (all internal pullups and pulldowns are active on input pins, independent of the $\overline{\text{PORRST}}$ state.)

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Table 2. Terminal Functions (continued)

| TERMINAL | | TYPE ⁽¹⁾⁽²⁾ | INTERNAL PULLUP/ PULLDOWN ⁽³⁾ | DESCRIPTION |
|---|---------------|------------------------|--|---|
| NAME | PIN NUMBER | | | |
| GENERAL-PURPOSE I/O (GIO) | | | | |
| GIOA[0]/INT0 | 28 | 3.3-V I | IPD | General-purpose input/output pins. GIOA[0]/INT[0] is an input-only pin. GIOA[7:0]/INT[7:0] are interrupt-capable pins. GIOA[1]/INT[1]/ECLK pin is multiplexed with the external clock-out function of the external clock prescale (ECP) module. |
| GIOA[1]/INT1/ ECLK | 29 | 3.3-V I/O | | |
| GIOA[2]/INT2 | 30 | | | |
| GIOA[3]/INT3 | 31 | | | |
| GIOA[4]/INT4 | 25 | | | |
| GIOA[5]/INT5 | 24 | | | |
| GIOA[6]/INT6 | 23 | | | |
| GIOA[7]/INT7 | 22 | | | |
| GIOB[0] | 16 | | | |
| GIOB[1] | 15 | | | |
| GIOB[2] | 14 | | | |
| GIOB[3] | 13 | | | |
| MULTI-BUFFERED ANALOG-TO-DIGITAL CONVERTER (MibADC) | | | | |
| ADEVT | 66 | 3.3-V I/O | IPD | MibADC event input. ADEVT can be programmed as a GIO pin.The ADEVT pin can also be used as a user-selectable event source to event trigger the MibADC event group or group1 if the associated register source bits are properly configured and defined. For the internal device connections, see the MibADC section of this data sheet. |
| ADIN[0] | 75 | 3.3-V I | | MibADC analog input pins |
| ADIN[1] | 74 | | | |
| ADIN[2] | 73 | | | |
| ADIN[3] | 72 | | | |
| ADIN[4] | 71 | | | |
| ADIN[5] | 69 | | | |
| ADIN[6] | 68 | | | |
| ADIN[7] | 67 | | | |
| ADIN[8] | 82 | | | |
| ADIN[9] | 80 | | | |
| ADIN[10] | 78 | | | |
| ADIN[11] | 76 | | | |
| ADIN[12] | 81 | | | |
| ADIN[13] | 79 | | | |
| ADIN[14] | 77 | | | |
| ADIN[15] | 70 | | | |
| AD _{REFHI} | 83 | 3.3-V REF I | | MibADC module high-voltage reference input |
| AD _{REFLO} | 84 | GND REF I | MibADC module low-voltage reference input | |
| V _{CCAD} | 85 | 3.3-V PWR | MibADC analog supply voltage | |
| V _{SSAD} | 86 | GND | MibADC analog ground reference. | |

Table 2. Terminal Functions (continued)

| TERMINAL | | TYPE ⁽¹⁾⁽²⁾ | INTERNAL PULLUP/ PULLDOWN ⁽³⁾ | DESCRIPTION |
|--|------------|------------------------|---|--|
| NAME | PIN NUMBER | | | |
| SERIAL PERIPHERAL INTERFACE 1 (SPI1) | | | | |
| SPI1CLK | 5 | 3.3-V I/O | IPD | SPI1 clock. SPI1CLK can be programmed as a GIO pin. |
| SPI1EN \overline{A} | 1 | | | SPI1 chip enable. $\overline{SPI1EN\overline{A}}$ can be programmed as a GIO pin. |
| SPI1SC \overline{S} | 2 | | | SPI1 slave chip select. $\overline{SPI1SC\overline{S}}$ can be programmed as a GIO pin. |
| SPI1SIMO | 3 | | | SPI1 data stream. Slave in/master out. SPI1SIMO can be programmed as a GIO pin. |
| SPI1SOMI | 4 | | | SPI1 data stream. Slave out/master in. SPI1SOMI can be programmed as a GIO pin. |
| SERIAL PERIPHERAL INTERFACE 2 (SPI2) | | | | |
| SPI2CLK | 41 | 3.3-V I/O | IPD | SPI2 clock. SPI2CLK can be programmed as a GIO pin. |
| SPI2EN \overline{A} | 44 | | | SPI2 chip enable. $\overline{SPI2EN\overline{A}}$ can be programmed as a GIO pin. |
| SPI2SC \overline{S} | 45 | | | SPI2 slave chip select. $\overline{SPI2SC\overline{S}}$ can be programmed as a GIO pin. |
| SPI2SIMO | 42 | | | SPI2 data stream. Slave in/master out. SPI2SIMO can be programmed as a GIO pin. |
| SPI2SOMI | 43 | | | SPI2 data stream. Slave out/master in. SPI2SOMI can be programmed as a GIO pin. |
| ZERO-PIN PHASE-LOCKED LOOP (ZPLL) | | | | |
| OSCIN | 8 | 1.8-V I | | Crystal connection pin or external clock input |
| OSCO \overline{U} T | 7 | 1.8-V O | | External crystal connection pin |
| PLLDIS | 51 | 3.3-V I | IPD | Enable/disable the ZPLL. The ZPLL can be bypassed and the oscillator becomes the system clock. If not in bypass mode, TI recommends that PLLDIS be connected to ground or pulled down to ground by an external resistor. |
| SERIAL COMMUNICATIONS INTERFACE 1 (SCI1) | | | | |
| SCI1CLK | 61 | 3.3-V I/O | IPD | SCI1 clock. SCI1CLK can be programmed as a GIO pin. |
| SCI1RX | 63 | 3.3-V I/O | IPU | SCI1 data receive. SCI1RX can be programmed as a GIO pin. |
| SCI1TX | 62 | 3.3-V I/O | IPU | SCI1 data transmit. SCI1TX can be programmed as a GIO pin. |
| SERIAL COMMUNICATIONS INTERFACE 2 (SCI2) | | | | |
| SCI2RX | 32 | 3.3-V I/O | IPU | SCI2 data receive. SCI2RX can be programmed as a GIO pin. |
| SCI2TX | 33 | 3.3-V I/O | IPU | SCI2 data transmit. SCI2TX can be programmed as a GIO pin. |
| SYSTEM MODULE (SYS) | | | | |
| CLKOUT | 58 | 3.3-V I/O | IPD | Bidirectional pin. CLKOUT can be programmed as a GIO pin or the output of SYSCLK, ICLK, or MCLK. |
| PORRST | 21 | 3.3-V I | IPD | Input master chip power-up reset. External V _{CC} monitor circuitry must assert a power-on reset. |
| \overline{RST} | 10 | 3.3-V I/O | IPU | Bidirectional reset. The internal circuitry can assert a reset, and an external system reset can assert a device reset. On \overline{RST} , the output buffer is implemented as an open drain (drives low only). To ensure an external reset is not arbitrarily generated, TI recommends that an external pullup resistor be connected to \overline{RST} . |
| WATCHDOG/REAL-TIME INTERRUPT (WD/RTI) | | | | |
| AWD | 50 | 3.3-V I/O | IPD | Analog watchdog reset. The AWD pin provides a system reset if the WD KEY is not written in time by the system, providing an external RC network circuit is connected. If the user is not using AWD, TI recommends that AWD be connected to ground or pulled down to ground by an external resistor. For more details on the external RC network circuit, see the <i>TMS470R1x System Module Reference Guide</i> (literature number SPNU189) and the application note <i>Analog Watchdog Resistor, Capacitor and Discharge Interval Selection Constraints</i> (literature number SPNA005). |

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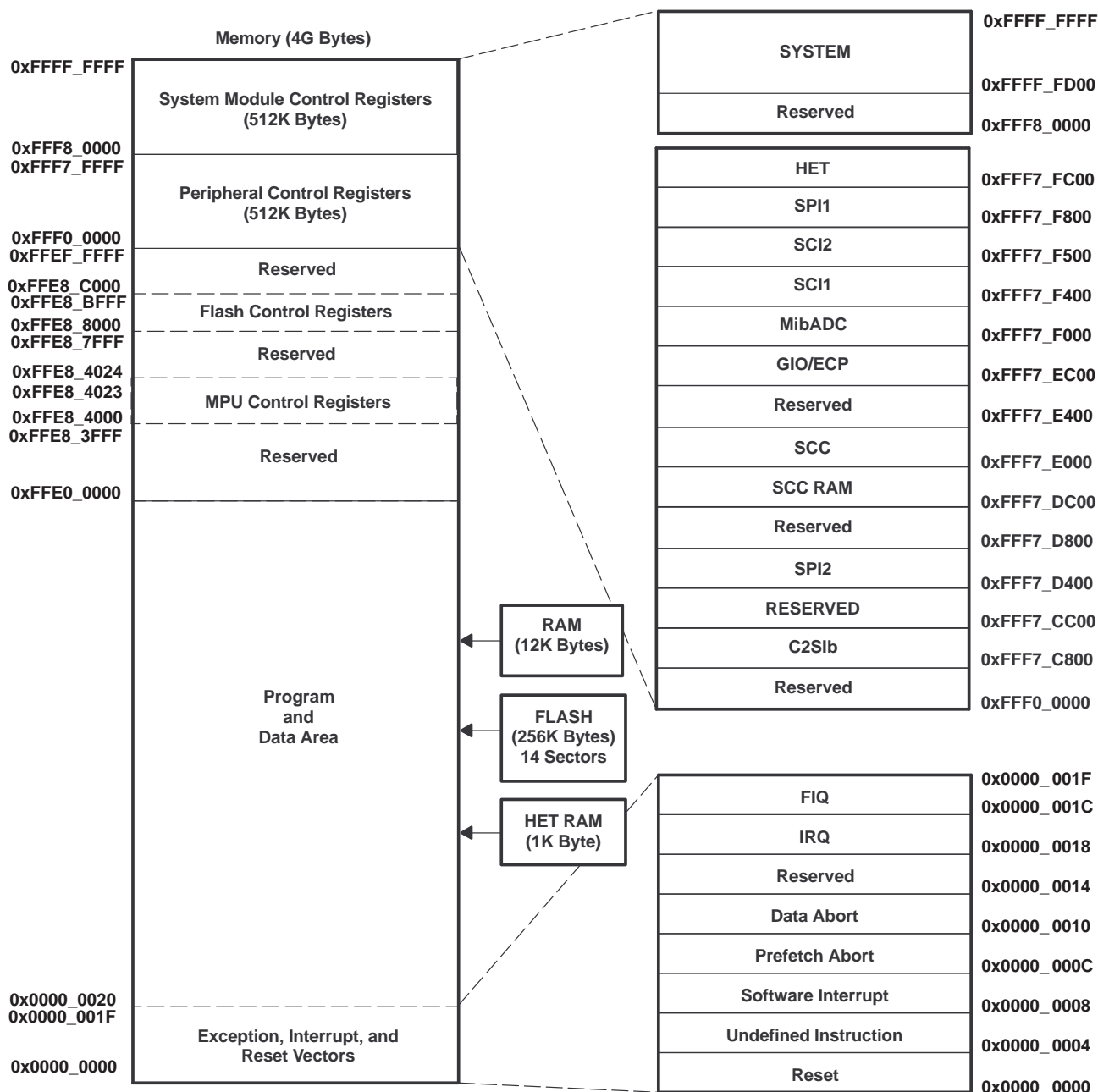
Table 2. Terminal Functions (continued)

| TERMINAL | | TYPE ⁽¹⁾⁽²⁾ | INTERNAL PULLUP/ PULLDOWN ⁽³⁾ | DESCRIPTION |
|------------------------------------|---------------|------------------------|--|--|
| NAME | PIN NUMBER | | | |
| TEST/DEBUG (T/D) | | | | |
| TCK | 54 | 3.3-V I | IPD | Test clock. TCK controls the test hardware (JTAG) |
| TDI | 52 | 3.3-V I | IPU | Test data in. TDI inputs serial data to the test instruction register, test data register, and programmable test address (JTAG). |
| TDO | 53 | 3.3-V O | IPD | Test data out. TDO outputs serial data from the test instruction register, test data register, identification register, and programmable test address (JTAG). |
| TEST | 27 | 3.3-V I | IPD | Test enable. Reserved for internal use only. TI recommends that TEST be connected to ground or pulled down to ground by an external resistor. |
| TMS | 87 | 3.3-V I | IPU | Serial input for controlling the state of the CPU test access port (TAP) controller (JTAG) |
| TMS2 | 88 | 3.3-V I | IPU | Serial input for controlling the second TAP. TI recommends that TMS2 be connected to VCCIO or pulled up to VCCIO by an external resistor. |
| TRST | 26 | 3.3-V I | IPD | Test hardware reset to TAP1 and TAP2. IEEE Standard 1149-1 (JTAG) Boundary-Scan Logic. TI recommends that TRST be pulled down to ground by an external resistor. |
| FLASH | | | | |
| FLTP1 | 95 | NC | | Flash test pads 1 and 2. For proper operation, these pins must not be connected (no connect [NC]). |
| FLTP2 | 94 | | | |
| V _{CCP} | 96 | 3.3-V PWR | | Flash external pump voltage (3.3 V) |
| SUPPLY VOLTAGE CORE (1.8 V) | | | | |
| V _{CC} | 9 | 1.8-V PWR | | Core logic supply voltage |
| | 40 | | | |
| | 65 | | | |
| | 90 | | | |
| | 93 | | | |
| SUPPLY VOLTAGE DIGITAL I/O (3.3 V) | | | | |
| V _{CCIO} | 12 | 3.3-V PWR | | Digital I/O supply voltage |
| | 57 | | | |
| SUPPLY GROUND CORE | | | | |
| V _{SS} | 6 | GND | | Core supply ground reference |
| | 39 | | | |
| | 64 | | | |
| | 89 | | | |
| | 92 | | | |
| SUPPLY GROUND DIGITAL I/O | | | | |
| V _{SSIO} | 11 | GND | | Digital I/O supply ground reference |
| | 56 | | | |

A256 DEVICE-SPECIFIC INFORMATION

Memory

Figure 1 shows the memory map of the A256 device.



- Memory addresses are configurable by the system (SYS) module within the range of 0x0000_0000 to 0xFFE0_0000.
- The CPU registers are not part of the memory map.

Figure 1. Memory Map

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Memory Selects

Memory selects allow the user to address memory arrays (i.e., flash, RAM, and HET RAM) at user-defined addresses. Each memory select has its own set (low and high) of memory base address registers (MFBHRx and MFBALRx) that together define the array's starting (base) address, block size, and protection.

The base address of each memory select is configurable to any memory address boundary that is a multiple of the decoded block size. For more information on how to control and configure these memory select registers, see the bus structure and memory sections of the *TMS470R1x System Module Reference Guide* (literature number SPNU189).

For the memory selection assignments and the memory selected, see [Table 3](#).

Table 3. Memory Selection Assignment

| MEMORY SELECT | MEMORY SELECTED (ALL INTERNAL) | MEMORY SIZE | MPU | MEMORY BASE ADDRESS REGISTER | STATIC MEM CTL REGISTER |
|---------------|--------------------------------|--------------------|-----|------------------------------|-------------------------|
| 0 (fine) | FLASH | 256K | NO | MFBHR0 and MFBALR0 | |
| 1 (fine) | FLASH | | NO | MFBHR1 and MFBALR1 | |
| 2 (fine) | RAM | 12K ⁽¹⁾ | YES | MFBHR2 and MFBALR2 | |
| 3 (fine) | RAM | | YES | MFBHR3 and MFBALR3 | |
| 4 (fine) | HET RAM | 1K | | MFBHR4 and MFBALR4 | SMCR1 |

(1) The starting addresses for both RAM memory-select signals cannot be offset from each other by a multiple of the user-defined block size in the memory-base address register.

RAM

The A256 device contains 12K bytes of internal static RAM configurable by the SYS module to be addressed within the range of 0x0000_0000 to 0xFFE0_0000. This RAM is implemented in one 12K-byte array selected by two memory-select signals. This configuration imposes an additional constraint on the memory map for RAM; the starting addresses for both RAM memory selects cannot be offset from each other by the multiples of the size of the physical RAM (i.e., 12K bytes for the A256 device). The RAM is addressed through memory selects 2 and 3.

The RAM can be protected by the memory protection unit (MPU) portion of the SYS module, allowing the user finer blocks of memory protection than is allowed by the memory selects. The MPU is ideal for protecting an operating system while allowing access to the current task. For more detailed information on the MPU portion of the SYS module and memory protection, see the memory section of the *TMS470R1x System Module Reference Guide* (literature number SPNU189).

F05 flash

The F05 flash memory is a nonvolatile electrically erasable, and programmable memory implemented with a 32-bit-wide data bus interface. The F05 flash has an external state machine for programming and erase functions. See the flash read and flash program and erase sections of this document.

flash protection keys

The A256 device provides flash protection keys. These four 32-bit protection keys prevent program/erase/compaction operations from occurring until after the four protection keys have been matched by the CPU loading the correct user keys into the FMPKEY control register. The protection keys on the A256 are located in the last 4 words of the first 8K sector. For more detailed information on the flash protection keys and the FMPKEY control register, see the protection keys portions of the *TMS470R1x F05 Flash Reference Guide* (literature number SPNU213).

flash read

The A256 flash memory is configurable by the SYS module to be addressed within the range of 0x0000_0000 to 0xFFE0_0000. The flash is addressed through memory selects 0 and 1.

NOTE:

The flash external pump voltage (V_{CCP}) is required for all operations (program, erase, and read).

flash pipeline mode

When in pipeline mode, the flash operates with a system clock frequency of up to 48 MHz. In normal mode, it operates with a system clock frequency of up to 24 MHz. Flash in pipeline mode is capable of accessing 64-bit words and provides two 32-bit pipelined words to the CPU. Also in pipeline mode, the flash can be read with no wait states when memory addresses are contiguous (after the initial 1-or 2-wait-state reads).

NOTE:

After a system reset, pipeline mode is disabled (ENPIPE bit FMREGOPT[0] = 0). In other words, the A256 device powers up and comes out of reset in non-pipeline mode. Furthermore, setting the flash configuration mode bit (GLBCTRL[4]) will override pipeline mode.

flash program and erase

The A256 device flash has one 256K-byte bank that consists of 14 sectors. These 14 sectors are sized as follows:

| SECTOR NO. | SEGMENT | LOW ADDRESS | HIGH ADDRESS |
|------------|-----------|-------------|--------------|
| 0 | 8K Bytes | 0x00000000 | 0x00001FFF |
| 1 | 8K Bytes | 0x00002000 | 0x00003FFF |
| 2 | 8K Bytes | 0x00004000 | 0x00005FFF |
| 3 | 8K Bytes | 0x00006000 | 0x00007FFF |
| 4 | 32K Bytes | 0x00008000 | 0x0000FFFF |
| 5 | 32K Bytes | 0x00010000 | 0x00017FFF |
| 6 | 32K Bytes | 0x00018000 | 0x0001FFFF |
| 7 | 32K Bytes | 0x00020000 | 0x00027FFF |
| 8 | 32K Bytes | 0x00028000 | 0x0002FFFF |
| 9 | 32K Bytes | 0x00030000 | 0x00037FFF |
| 10 | 8K Bytes | 0x00038000 | 0x00039FFF |
| 11 | 8K Bytes | 0x0003A000 | 0x0003BFFF |
| 12 | 8K Bytes | 0x0003C000 | 0x0003DFFF |
| 13 | 8K Bytes | 0x0003E000 | 0x0003FFFF |

The minimum size for an erase operation is one sector. The maximum size for a program operation is one 16-bit word.

NOTE:

The flash external pump voltage (V_{CCP}) is required for all operations (program, erase, and read).

For more detailed information on flash program and erase operations, see the *TMS470R1x F05 Flash Reference Guide* (literature number SPNU213).

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HET RAM

The A256 device contains HET RAM. The HET RAM has a 64-instruction capability. The HET RAM is configurable by the SYS module to be addressed within the range of 0x0000_0000 to 0xFFE0_0000. The HET RAM is addressed through memory select 4.

Peripheral Selects and Base Addresses

The A256 device uses 10 of the 16 peripheral selects to decode the base addresses of the peripherals. These peripheral selects are fixed and transparent to the user since they are part of the decoding scheme used by the SYS module.

Control registers for the peripherals, SYS module, and flash begin at the base addresses shown in [Table 4](#).

Table 4. A256 Peripherals, System Module, and Flash Base Addresses

| CONNECTING MODULE | ADDRESS RANGE | | PERIPHERAL SELECTS |
|-------------------------|---------------|----------------|--------------------|
| | BASE ADDRESS | ENDING ADDRESS | |
| SYSTEM | 0xFFFF_FD00 | 0xFFFF_FFFF | N/A |
| RESERVED | 0xFFFF8_0000 | 0xFFFF_FCFE | N/A |
| HET | 0xFFFF7_FC00 | 0xFFFF7_FFFF | PS[0] |
| SPI1 | 0xFFFF7_F800 | 0xFFFF7_FBFF | PS[1] |
| SCI2 | 0xFFFF7_F500 | 0xFFFF7_F7FF | PS[2] |
| SCI1 | 0xFFFF7_F400 | 0xFFFF7_F4FF | |
| ADC | 0xFFFF7_F000 | 0xFFFF7_F3FF | PS[3] |
| GIO/ECP | 0xFFFF7_EC00 | 0xFFFF7_EFFF | PS[4] |
| RESERVED | 0xFFFF7_E400 | 0xFFFF7_EBFF | PS[5] – PS[6] |
| SCC | 0xFFFF7_E000 | 0xFFFF7_E3FF | PS[7] |
| SCC RAM | 0xFFFF7_DC00 | 0xFFFF7_DFFF | PS[8] |
| RESERVED | 0xFFFF7_D800 | 0xFFFF7_DBFF | PS[9] |
| SPI2 | 0xFFFF7_D400 | 0xFFFF7_D7FF | PS[10] |
| RESERVED | 0xFFFF7_CC00 | 0xFFFF7_D3FF | PS[11] – PS[12] |
| C2Sib | 0xFFFF7_C800 | 0xFFFF7_CBFF | PS[13] |
| RESERVED | 0xFFFF7_C000 | 0xFFFF7_C7FF | PS[14] – PS[15] |
| RESERVED | 0xFFFF0_0000 | 0xFFFF7_BFFF | N/A |
| FLASH CONTROL REGISTERS | 0xFFE8_8000 | 0xFFE8_BFFF | N/A |
| MPU CONTROL REGISTERS | 0xFFE8_4000 | 0xFFE8_4023 | N/A |

Interrupt Priority

The central interrupt manager (CIM) portion of the SYS module manages the interrupt requests from the device modules (i.e., SPI1 or SPI2, SCI1 or SCI2, and RTI, etc.).

Although the CIM can accept up to 32 interrupt request signals, the A256 device only uses 21 of those interrupt request signals. The request channels are maskable so that individual channels can be selectively disabled. All interrupt requests can be programmed in the CIM to be of either type:

- Fast interrupt request (FIQ)
- Normal interrupt request (IRQ)

The precedences of request channels decrease with ascending channel order in the CIM (0 [highest] and 31 [lowest] priority). For these channel priorities and the associated modules, see [Table 5](#).

Table 5. Interrupt Priority

| MODULES | INTERRUPT SOURCES | INTERRUPT LEVEL/CHANNEL |
|-----------|---------------------------|-------------------------|
| SPI1 | SPI1 end-transfer/overrun | 0 |
| RTI | COMP2 interrupt | 1 |
| RTI | COMP1 interrupt | 2 |
| RTI | TAP interrupt | 3 |
| SPI2 | SPI2 end-transfer/overrun | 4 |
| GIO | Interrupt A | 5 |
| RESERVED | | 6 |
| HET | Interrupt 1 | 7 |
| RESERVED | | 8 |
| SCI1/SCI2 | SCI1/SCI2 error interrupt | 9 |
| SCI1 | SCI1 receive interrupt | 10 |
| C2S1b | C2S1b interrupt | 11 |
| RESERVED | | 12 |
| RESERVED | | 13 |
| SCC | Interrupt A | 14 |
| RESERVED | | 15 |
| MibADC | End event conversion | 16 |
| SCI2 | SCI2 receive interrupt | 17 |
| RESERVED | | 18 |
| RESERVED | | 19 |
| SCI1 | SCI1 transmit interrupt | 20 |
| System | SW interrupt (SSI) | 21 |
| RESERVED | | 22 |
| HET | Interrupt 2 | 23 |
| RESERVED | | 24 |
| SCC | Interrupt B | 25 |
| SCI2 | SCI2 transmit interrupt | 26 |
| MibADC | End Group 1 conversion | 27 |
| RESERVED | | 28 |
| GIO | Interrupt B | 29 |
| MibADC | End Group 2 conversion | 30 |
| RESERVED | | 31 |

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MibADC

The multi-buffered analog-to-digital converter (MibADC) accepts an analog signal and converts the signal to a 10-bit digital value.

The A256 MibADC module can function in two modes: compatibility mode, where its programmer's model is compatible with the TMS470R1x ADC module and its digital results are stored in digital result registers; or in buffered mode, where the digital result registers are replaced with three FIFO buffers, one for each conversion group (event, group1 [G1], and group2 [G2]). In buffered mode, the MibADC buffers can be serviced by interrupts.

MibADC event trigger enhancements

The MibADC includes two major enhancements over the event-triggering capability of the TMS470R1x ADC.

- Both group1 and the event group can be configured for event-triggered operation, providing up to two event-triggered groups.
- The trigger source and polarity can be selected individually for both group 1 and the event group from the three options identified in [Table 6](#).

Table 6. MibADC Event Hookup Configuration

| EVENT # | SOURCE SELECT BITS for G1 or EVENT (G1SRC[1:0] or EVSRC[1:0]) | SIGNAL PIN NAME |
|---------|--|-----------------|
| EVENT1 | 00 | ADEVT |
| EVENT2 | 01 | HET18 |
| EVENT3 | 10 | HET19 |
| EVENT4 | 11 | RESERVED |

For group 1, these event-triggered selections are configured through the group 1 source select bits (G1SRC[1:0]) in the AD event source register (ADEVTSRC[5:4]). For the event group, these event-triggered selections are configured through the event group source select bits (EVSRC[1:0]) in the AD event source register (ADEVTSRC[1:0]).

For more detailed functional information on the MibADC, see the *TMS470R1x Multi-Buffered Analog-to-Digital Converter (MibADC) Reference Guide* (literature number SPNU206).

Documentation Support

Extensive documentation supports all of the TMS470 microcontroller family generation of devices. The types of documentation available include: data sheets with design specifications; complete user's guides; and errata sheets. Useful reference documentation includes:

- Bulletin
 - *TMS470 Microcontroller Family Product Bulletin* (literature number SPNB086)
- User's Guides
 - *TMS470R1x System Module Reference Guide* (literature number SPNU189)
 - *TMS470R1x General Purpose Input/Output (GPIO) Reference Guide* (literature number SPNU192)
 - *TMS470R1x Direct Memory Access (DMA) Controller Reference Guide* (literature number SPNU194)
 - *TMS470R1x Serial Peripheral Interface (SPI) Reference Guide* (literature number SPNU195)
 - *TMS470R1x Serial Communication Interface (SCI) Reference Guide* (literature number SPNU196)
 - *TMS470R1x Controller Area Network (CAN) Reference Guide* (literature number SPNU197)
 - *TMS470R1x High End Timer (HET) Reference Guide* (literature number SPNU199)
 - *TMS470R1x External Clock Prescale (ECP) Reference Guide* (literature number SPNU202)
 - *TMS470R1x MultiBuffered Analog to Digital (MibADC) Reference Guide* (literature number SPNU206)
 - *TMS470R1x ZeroPin Phase Locked Loop (ZPLL) Clock Module Reference Guide* (literature number SPNU212)
 - *TMS470R1x F05 Flash Reference Guide* (literature number SPNU213)
 - *TMS470R1x Class II Serial Interface B (C2S1b) Reference Guide* (literature number SPNU214)
 - *TMS470R1x Class II Serial Interface A (C2S1a) Reference Guide* (literature number SPNU218)
 - *TMS470R1x Inter-Integrated Circuit (I2C) Reference Guide* (literature number SPNU223)
 - *TMS470 Peripherals Overview Reference Guide* (literature number SPNU248)
- Errata Sheet:
 - *TMS470R1A256 TMS470 Microcontrollers Silicon Errata* (literature number SPNZ133)

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Device and Development-Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all DSP devices and support tools. Each DSP commercial family member has one of three prefixes: TMX, TMP, or TMS (e.g., **TMS470R1A256**). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX/TMDX) through fully qualified production devices/tools (TMS/TMDS).

Device development evolutionary flow:

- TMX** Experimental device that is not necessarily representative of the final device's electrical specifications
- TMP** Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification
- TMS** Fully qualified production device

Support tool development evolutionary flow:

- TMDX** Development-support product that has not yet completed Texas Instruments internal qualification testing.
- TMDS** Fully qualified development-support product

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

TMS devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

[Figure 2](#) illustrates the numbering and symbol nomenclature for the TMS470R1x family.

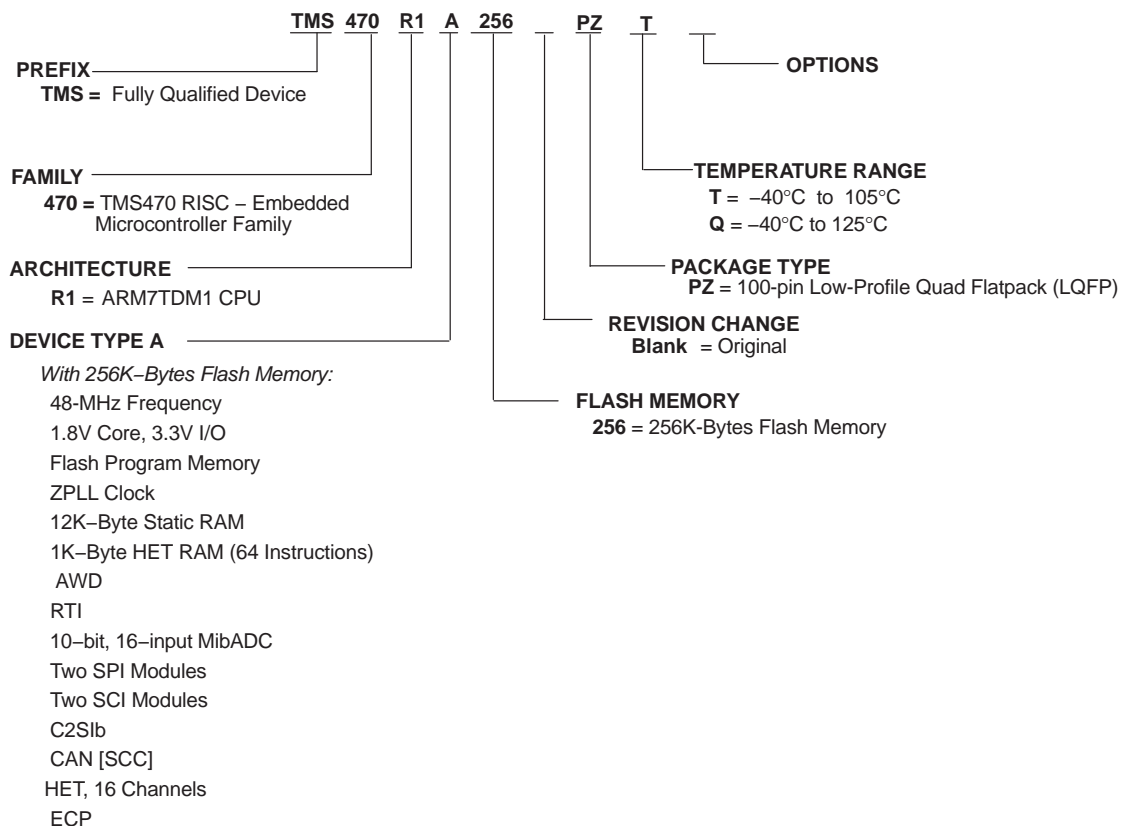


Figure 2. TMS470R1x Family Nomenclature

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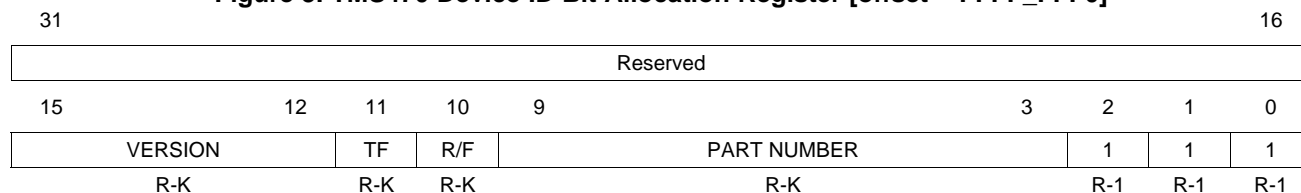
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Device Identification Code Register

The device identification code register identifies the silicon version, the technology family (TF), a ROM or flash device, and an assigned device-specific part number (see Figure 3). The A256 device identification code register value is 0x0857.

Figure 3. TMS470 Device ID Bit Allocation Register [offset = FFFF_FFF0]



LEGEND: R = Read only; -K = value constant after RESET; -n = value after RESET

TMS470 Device ID Bit Allocation Register Description

| BIT | NAME | Value | DESCRIPTION |
|-------|-------------|--------|--|
| 31-16 | Reserved | | Reads are undefined and writes have no effect. |
| 15-12 | VERSION | | Silicon version (revision) bits These bits identify what version of silicon the device is. Initial device version numbers start at 0000. |
| 11 | TF | 0 1 | Technology Family (TF) This bit distinguishes the technology family core power supply. 3.3 V for F10/C10 devices 1.8 V for F05/C05 devices |
| 10 | R/F | 0 1 | ROM/flash This bit distinguishes between ROM and flash devices: Flash device ROM device |
| 9-3 | PART NUMBER | | Device-specific part number These bits identify the assigned device-specific part number. The assigned device-specific part number for the A256 device is 0001010. |
| 2-0 | 1 | | Mandatory High Bits 2, 1, and 0 are tied high by default. |

DEVICE ELECTRICAL SPECIFICATIONS AND TIMING PARAMETERS

Absolute Maximum Ratings

over operating free-air temperature range, T version (unless otherwise noted)⁽¹⁾

| | | |
|--|--|---------------------|
| Supply voltage ranges: | V_{CC}, V_{CCF} ⁽²⁾ | -0.3 V to 2.5 |
| Supply voltage ranges: | $V_{CCIO}, V_{CCAD}, V_{CCP}$ (flash pump) ⁽²⁾ | -0.3 V to 4.1V |
| Input voltage range: | All input pins | -0.3 V to 4.1 |
| Input clamp current: | $I_{IK} (V_I < 0 \text{ or } V_I > V_{CCIO})$ All pins except ADIN[0:15], \overline{PORRST} , \overline{TRST} , TEST and TCK | $\pm 20 \text{ mA}$ |
| | $I_{IK} (V_I < 0 \text{ or } V_I > V_{CCAD})$ ADIN[0:11] | $\pm 10 \text{ mA}$ |
| Operating free-air temperature ranges, T_A : | T version | -40°C to 105°C |
| | Q version | -40°C to 125°C |
| Operating junction temperature range, T_J | | -40°C to 150°C |
| Storage temperature range, T_{stg} | | -65°C to 150°C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to their associated grounds.

Device Recommended Operating Conditions⁽¹⁾

| | | | MIN | NOM | MAX | UNIT |
|-------------------|---|-----------|------|-----|------|------|
| V _{CC} | Digital logic and flash supply voltage (Core) | | 1.81 | | 2.06 | V |
| V _{CCIO} | Digital logic supply voltage (I/O) | | 3 | 3.3 | 3.6 | V |
| V _{CCAD} | ADC supply voltage | | 3 | 3.3 | 3.6 | V |
| V _{CCP} | Flash pump supply voltage | | 3 | 3.3 | 3.6 | V |
| V _{SS} | Digital logic supply ground | | 0 | | | V |
| V _{SSAD} | ADC supply ground | | -0.1 | | 0.1 | V |
| T _A | Operating free-air temperature | T version | -40 | | 105 | °C |
| | | Q version | -40 | | 125 | |
| T _J | Operating junction temperature | | -40 | | 150 | °C |

(1) All voltages are with respect to VSS, except VCCAD, which is with respect to VSSAD.

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Electrical Characteristics over Recommended Operating Free-Air Temperature Range⁽¹⁾

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------|--|---|--|-------------------------|-----|-------------------------|------|
| V _{hys} | Input hysteresis | | | 0.15 | | | V |
| V _{IL} | Low-level input voltage | All inputs ⁽²⁾ except OSCIN | | -0.3 | | 0.8 | V |
| | | OSCIN only | | -0.3 | | 0.35 V _{CC} | |
| V _{IH} | High-level input voltage | All inputs except OSCIN | | 2 | | V _{CCIO} + 0.3 | V |
| | | OSCIN only | | 0.65 V _{CC} | | V _{CC} + 0.3 | |
| V _{th} | Input threshold voltage | AWD only | | 1.35 | | 1.8 | V |
| RDS _{ON} | Drain to source on resistance | AWD only ⁽³⁾ | VOL = 0.35 V @ I _{OL} = 8mA | | | 45 | Ω |
| V _{OL} | Low-level output voltage ⁽⁴⁾ | | I _{OL} = I _{OL} MAX | | | 0.2 V _{CCIO} | V |
| | | | I _{OL} = 50 μA | | | 0.2 | |
| V _{OH} | High-level output voltage ⁽⁴⁾ | | I _{OH} = I _{OH} MIN | 0.8 V _{CCIO} | | | V |
| | | | I _{OH} = 50 μA | V _{CCIO} - 0.2 | | | |
| I _{IC} | Input clamp current (I/O pins) ⁽⁵⁾ | | V _I < V _{SSIO} - 0.3 or V _I > V _{CCIO} + 0.3 | -2 | | 2 | mA |
| I _I | Input current (I/O pins) | I _{IL} Pulldown | V _I = V _{SS} | -1 | | 1 | μA |
| | | I _{IH} Pulldown | V _I = V _{CCIO} | 5 | | 40 | |
| | | I _{IL} Pullup | V _I = V _{SS} | -40 | | -5 | |
| | | I _{IH} Pullup | V _I = V _{CCIO} | -1 | | 1 | |
| | | All other pins | No pullup or pulldown | -1 | | 1 | |
| I _{OL} | Low-level output current | CLKOUT, AWD, TDO | V _{OL} = V _{OL} MAX | | | 8 | mA |
| | | RST, SPI1CLK, SPI1SIMO, SPI1SOMI, SPI2CLK, SPI2SIMO, SPI2SOMI | V _{OL} = V _{OL} MAX | | | 4 | |
| | | All other output pins ⁽⁶⁾ | V _{OL} = V _{OL} MAX | | | 2 | |
| I _{OH} | High-level output current | CLKOUT, TDO | V _{OH} = V _{OH} MIN | -8 | | | mA |
| | | SPI1CLK, SPI1SIMO, SPI1SOMI, SPI2CLK, SPI2SIMO, SPI2SOMI | V _{OH} = V _{OH} MIN | -4 | | | |
| | | All other output pins ⁽⁶⁾ | V _{OH} = V _{OH} MIN | -2 | | | |
| I _{CC} | V _{CC} digital supply current (operating mode) | | SYSCLK = 48 MHz, ICLK = 24 MHz, V _{CC} = 2.06 V | | | 70 | mA |
| | | | SYSCLK = 24 MHz, ICLK = 12 MHz, V _{CC} = 2.06 V | | | 50 | mA |
| | V _{CC} digital supply current (standby mode) ⁽⁷⁾ | | OSCIN = 6 MHz, V _{CC} = 2.06 V | | | 3.0 | mA |
| | V _{CC} digital supply current (halt mode) ⁽⁷⁾ | | All frequencies, V _{CC} = 2.06 V | | | 1.0 | mA |

(1) Source currents (out of the device) are negative while sink currents (into the device) are positive.

(2) This does not apply to the PORRST pin. For PORRST exceptions, see the RST and PORRST timings section.

(3) These values help to determine the external RC network circuit. For more details, see the TMS470R1x System Module Reference Guide (literature number SPNU189).

(4) V_{OL} and V_{OH} are linear with respect to the amount of load current (I_{OL}/I_{OH}) applied.

(5) Parameter does not apply to input-only or output-only pins.

(6) The 2 mA buffers on this device are called zero-dominant buffers. If two of these buffers are shorted together and one is outputting a low level and the other is outputting a high level, the resulting value will always be low.

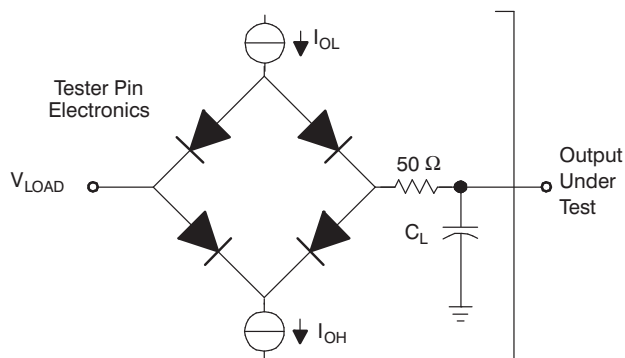
(7) For flash pumps/banks in sleep mode.

Electrical Characteristics over Recommended Operating Free-Air Temperature Range (continued)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------|--|--|-----|-----|-----|---------------|
| I_{CCIO} | V_{CCIO} digital supply current (operating mode) | No DC load, $V_{CCIO} = 3.6\text{ V}^{(8)}$ | | | 10 | mA |
| | V_{CCIO} digital supply current (standby mode) | No DC load, $V_{CCIO} = 3.6\text{ V}^{(8)}$ | | | 300 | μA |
| | V_{CCIO} digital supply current (halt mode) | No DC load, $V_{CCIO} = 3.6\text{ V}^{(8)}$ | | | 300 | μA |
| I_{CCAD} | V_{CCAD} supply current (operating mode) | All frequencies, $V_{CCAD} = 3.6\text{ V}$ | | | 15 | mA |
| | V_{CCAD} supply current (standby mode) | All frequencies, $V_{CCAD} = 3.6\text{ V}$ | | | 20 | μA |
| | V_{CCAD} supply current (halt mode) | All frequencies, $V_{CCAD} = 3.6\text{ V}$ | | | 20 | μA |
| I_{CCP} | V_{CCP} pump supply current | $V_{CCP} = 3.6\text{ V}$ read operation | | | 45 | mA |
| | | $V_{CCP} = 3.6\text{ V}$ program and erase | | | 70 | mA |
| | | $V_{CCP} = 3.6\text{ V}$ standby mode operation ⁽⁷⁾ | | | 20 | μA |
| | | $V_{CCP} = 3.6\text{ V}$ halt mode operation ⁽⁷⁾ | | | 20 | μA |
| C_I | Input capacitance | | | 2 | | pF |
| C_O | Output capacitance | | | 3 | | pF |

(8) I/O pins configured as inputs or outputs with no load. All pulldown inputs $\geq 0.2\text{ V}$. All pullup inputs $\geq V_{CCIO} - 0.2\text{ V}$.

Parameter Measurement Information



Where: I_{OL} = $I_{OL\text{ MAX}}$ for the respective pin^(A)
 I_{OH} = $I_{OH\text{ MIN}}$ for the respective pin^(A)
 V_{LOAD} = 1.5 V
 C_L = 150-pF typical load-circuit capacitance^(B)

- For these values, see the "Electrical Characteristics over Recommended Operating Free-Air Temperature Range" table.
- All timing parameters measured using an external load capacitance of 150 pF unless otherwise noted.

Figure 4. Test Load Circuit

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Timing Parameter Symbolology

Timing parameter symbols have been created in accordance with JEDEC Standard 100. To shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

| | | | |
|-----------|------------------------|------|--------------------------------|
| CM | Compaction, CMPCT | RD | Read |
| CO | CLKOUT | RST | Reset, $\overline{\text{RST}}$ |
| ER | Erase | RX | SCInRX |
| ICLK | Interface clock | S | Slave mode |
| M | Master mode | SCC | SCInCLK |
| OSC, OSCI | OSCIN | SIMO | SPInSIMO |
| OSCO | OSCO | SOMI | SPInSOMI |
| P | Program, PROG | SPC | SPInCLK |
| R | Ready | SYS | System clock |
| R0 | Read margin 0, RDMRGN0 | TX | SCInTX |
| R1 | Read margin 1, RDMRGN1 | | |

Lowercase subscripts and their meanings are:

| | | | |
|---|---------------------|----|------------------------|
| a | access time | r | rise time |
| c | cycle time (period) | su | setup time |
| d | delay time | t | transition time |
| f | fall time | v | valid time |
| h | hold time | w | pulse duration (width) |

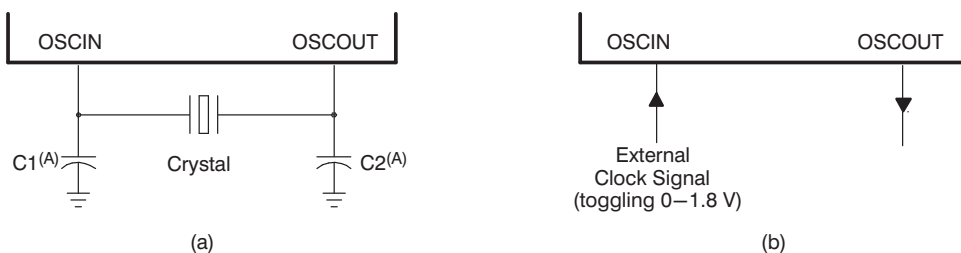
The following additional letters are used with these meanings:

| | | | |
|---|-------|---|--|
| H | High | X | Unknown, changing, or don't care level |
| L | Low | Z | High impedance |
| V | Valid | | |

External Reference Resonator/Crystal Oscillator Clock Option

The oscillator is enabled by connecting the appropriate fundamental 4–20 MHz resonator/crystal and load capacitors across the external OSCIN and OSCOUT pins as shown in Figure 5a. The oscillator is a single-stage inverter held in bias by an integrated bias resistor. This resistor is disabled during leakage test measurement and HALT mode. **TI strongly encourages each customer to submit samples of the device to the resonator/crystal vendors for validation.** The vendors are equipped to determine what load capacitors will best tune their resonator/crystal to the microcontroller device for optimum start-up and operation over temperature/voltage extremes.

An external oscillator source can be used by connecting a 1.8-V clock signal to the OSCIN pin and leaving the OSCOUT pin unconnected (open) as shown in Figure 5b.



- A. The values of C1 and C2 should be provided by the resonator/crystal vendor.

Figure 5. Crystal/Clock Connection

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ZPLL AND CLOCK SPECIFICATIONS

Timing Requirements for ZPLL Circuits Enabled or Disabled

| | | MIN | MAX | UNIT |
|----------------|-----------------------------------|-----|-----|------|
| $f_{(OSC)}$ | Input clock frequency | 4 | 20 | MHz |
| $t_{c(OSC)}$ | Cycle time, OSCIN | 50 | | ns |
| $t_{w(OSCIL)}$ | Pulse duration, OSCIN low | 15 | | ns |
| $t_{w(OSCIH)}$ | Pulse duration, OSCIN high | 15 | | ns |
| $f_{(OSCRST)}$ | OSC FAIL frequency ⁽¹⁾ | | 53 | kHz |

- (1) Causes a device reset (specifically a clock reset) by setting the RST OSC FAIL (GLBCTRL.15) and the OSC FAIL flag (GLBSTAT.1) bits equal to 1. For more detailed information on these bits and device resets, see the *TMS470R1x System Module Reference Guide* (literature number SPNU189).

Switching Characteristics over Recommended Operating Conditions for Clocks⁽¹⁾⁽²⁾

| PARAMETER | | TEST CONDITION ⁽³⁾ | MIN | MAX | UNIT |
|-----------------|--|-------------------------------|------|-----|------|
| $f_{(SYS)}$ | System clock frequency ⁽⁴⁾ | Pipeline mode enabled | | 48 | MHz |
| | | Pipeline mode disabled | | 24 | |
| $f_{(CONFIG)}$ | System clock frequency - flash config mode | | | 24 | MHz |
| $f_{(ICLK)}$ | Interface clock frequency | Pipeline mode enabled | | 25 | MHz |
| | | Pipeline mode disabled | | 24 | |
| $f_{(ECLK)}$ | External clock output frequency for ECP Module | Pipeline mode enabled | | 25 | MHz |
| | | Pipeline mode disabled | | 24 | |
| $t_{c(SYS)}$ | Cycle time, system clock | Pipeline mode enabled | 20.8 | | ns |
| | | Pipeline mode disabled | 41.6 | | |
| $t_{c(CONFIG)}$ | Cycle time, system clock - flash config mode | | 41.6 | | ns |
| $t_{c(ICLK)}$ | Cycle time, interface clock | Pipeline mode enabled | 40 | | ns |
| | | Pipeline mode disabled | 41.6 | | |
| $t_{c(ECLK)}$ | Cycle time, ECP module external clock output | Pipeline mode enabled | 40 | | ns |
| | | Pipeline mode disabled | 41.6 | | |

- (1) $f_{(SYS)} = M \times f_{(OSC)} / R$, where $M = \{4 \text{ or } 8\}$, $R = \{1, 2, 3, 4, 5, 6, 7, 8\}$ when $PLLDIS = 0$. R is the system-clock divider determined by the CLKDIVPRE [2:0] bits in the global control register (GLBCTRL[2:0]) and M is the PLL multiplier determined by the MULT4 bit, also in the GLBCTRL register (GLBCTRL.3).
 $f_{(SYS)} = f_{(OSC)} / R$, where $R = \{1, 2, 3, 4, 5, 6, 7, 8\}$ when $PLLDIS = 1$.
 $f_{(ICLK)} = f_{(SYS)} / X$, where $X = \{1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16\}$. X is the interface clock divider ratio determined by the PCR0[4:1] bits in the SYS module.
 (2) $f_{(ECLK)} = f_{(ICLK)} / N$, where $N = \{1 \text{ to } 256\}$. N is the ECP prescale value defined by the ECPCTRL[7:0] register bits in the ECP module.
 (3) Pipeline mode enabled or disabled is determined by the ENPIPE bit (FMREGOPT.0).
 (4) Flash Vread must be set to 5 V to achieve maximum system clock frequency.

Switching Characteristics over Recommended Operating Conditions for External Clocks⁽¹⁾⁽²⁾⁽³⁾

(see Figure 6 and Figure 7)

| PARAMETER | TEST CONDITION | MIN | MAX | UNIT |
|--------------|---|--|-----|------|
| $t_{w(COL)}$ | SYSCLK or MCLK ⁽⁴⁾ | $0.5t_{c(SYS)} - t_f$ | | ns |
| | ICLK, X is even or 1 ⁽⁵⁾ | $0.5t_{c(ICLK)} - t_f$ | | |
| | ICLK, X is odd and not 1 ⁽⁵⁾ | $0.5t_{c(ICLK)} + 0.5t_{c(SYS)} - t_f$ | | |
| $t_{w(COH)}$ | SYSCLK or MCLK ⁽⁴⁾ | $0.5t_{c(SYS)} - t_r$ | | ns |
| | ICLK, X is even or 1 ⁽⁵⁾ | $0.5t_{c(ICLK)} - t_r$ | | |
| | ICLK, X is odd and not 1 ⁽⁵⁾ | $0.5t_{c(ICLK)} - 0.5t_{c(SYS)} - t_r$ | | |
| $t_{w(EOL)}$ | N is even and X is even or odd | $0.5t_{c(ECLK)} - t_f$ | | ns |
| | N is odd and X is even | $0.5t_{c(ECLK)} - t_f$ | | |
| | N is odd and X is odd and not 1 | $0.5t_{c(ECLK)} + 0.5t_{c(SYS)} - t_f$ | | |
| $t_{w(EOH)}$ | N is even and X is even or odd | $0.5t_{c(ECLK)} - t_r$ | | ns |
| | N is odd and X is even | $0.5t_{c(ECLK)} - t_r$ | | |
| | N is odd and X is odd and not 1 | $0.5t_{c(ECLK)} - 0.5t_{c(SYS)} - t_r$ | | |

(1) $X = \{1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16\}$. X is the interface clock divider ratio determined by the PCR0[4:1] bits in the SYS module.

(2) $N = \{1 \text{ to } 256\}$. N is the ECP prescale value defined by the ECPCTRL[7:0] register bits in the ECP module.

(3) CLKOUT/ECLK pulse durations (low/high) are a function of the OSCIN pulse durations when PLLDIS is active.

(4) Clock source bits selected as either SYSCLK (CLKCNTL[6:5] = 11 binary) or MCLK (CLKCNTL[6:5] = 10 binary).

(5) Clock source bits selected as ICLK (CLKCNTL[6:5] = 01 binary).

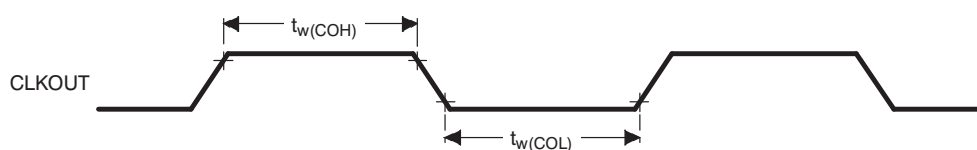


Figure 6. CLKOUT Timing Diagram

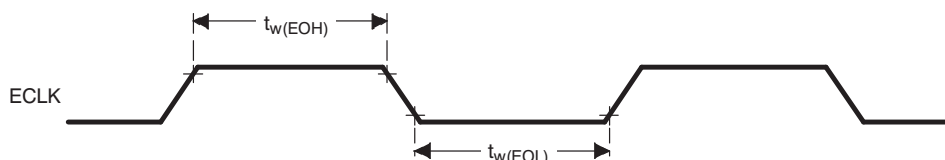


Figure 7. ECLK Timing Diagram

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RST AND PORRST TIMINGS

Timing Requirements for PORRST

(see Figure 8)

| | | MIN | MAX | UNIT |
|---------------------|--|------|----------------|------|
| V_{CCPORL} | V_{CC} low supply level when \overline{PORRST} must be active during power up | | 0.6 | V |
| V_{CCPORH} | V_{CC} high supply level when \overline{PORRST} must remain active during power up and become active during power down | 1.5 | | V |
| $V_{CCIOPORL}$ | V_{CCIO} low supply level when \overline{PORRST} must be active during power up | | 1.1 | V |
| $V_{CCIOPORH}$ | V_{CCIO} high supply level when \overline{PORRST} must remain active during power up and become active during power down | 2.75 | | V |
| V_{IL} | Low-level input voltage after $V_{CCIO} > V_{CCIOPORH}$ | | $0.2 V_{CCIO}$ | V |
| $V_{IL(PORRST)}$ | Low-level input voltage of \overline{PORRST} before $V_{CCIO} > V_{CCIOPORL}$ | | 0.5 | V |
| $t_{su(PORRST)r}$ | Setup time, \overline{PORRST} active before $V_{CCIO} > V_{CCIOPORL}$ during power up | 0 | | ms |
| $t_{su(VCCIO)r}$ | Setup time, $V_{CCIO} > V_{CCIOPORL}$ before $V_{CC} > V_{CCPORL}$ | 0 | | ms |
| $t_h(PORRST)r$ | Hold time, \overline{PORRST} active after $V_{CC} > V_{CCPORH}$ | 1 | | ms |
| $t_{su(PORRST)f}$ | Setup time, \overline{PORRST} active before $V_{CC} \leq V_{CCPORH}$ during power down | 8 | | ms |
| $t_h(PORRST)rio$ | Hold time, \overline{PORRST} active after $V_{CC} > V_{CCIOPORH}$ | 1 | | ms |
| $t_h(PORRST)d$ | Hold time, \overline{PORRST} active after $V_{CC} < V_{CCPORL}$ | 0 | | ms |
| $t_{su(PORRST)fio}$ | Setup time, \overline{PORRST} active before $V_{CC} \leq V_{CCIOPORH}$ during power down | 0 | | ms |
| $t_{su(VCCIO)f}$ | Setup time, $V_{CC} < V_{CCPORL}$ before $V_{CCIO} < V_{CCIOPORL}$ | 0 | | ms |

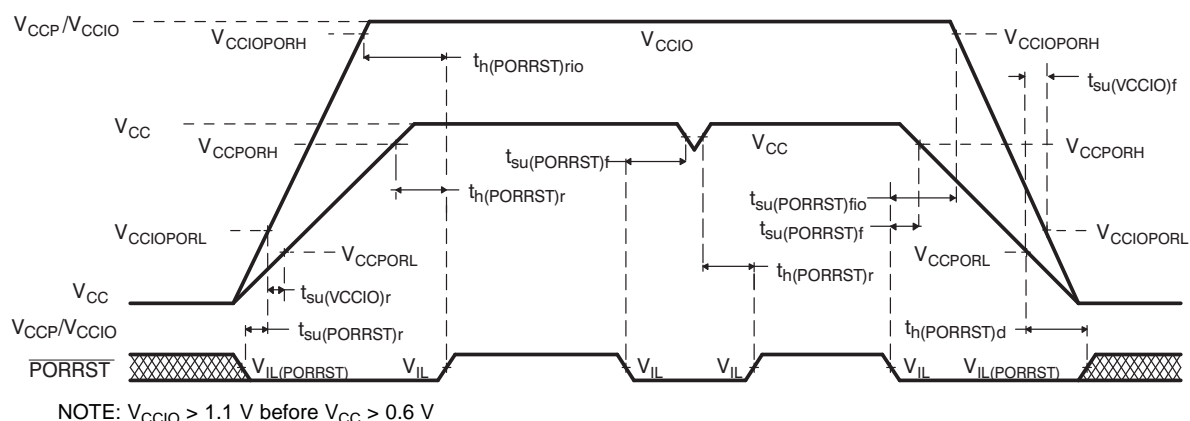


Figure 8. \overline{PORRST} Timing Diagram

Switching Characteristics over Recommended Operating Conditions for $\overline{RST}^{(1)}$

| | PARAMETER | MIN | MAX | UNIT |
|------------|--|------------------|-----|------|
| $t_v(RST)$ | Valid time, \overline{RST} active after PORRST inactive | $4112t_{c(OSC)}$ | | ns |
| | Valid time, \overline{RST} active (all others) | $8t_{c(SYS)}$ | | |
| T_{fsu} | Flash start-up time, from \overline{RST} inactive to fetch of first instruction from flash (flash pump stabilization time) | $456t_{c(OSC)}$ | | ns |

(1) Specified values do NOT include rise/fall times. For rise and fall timings, see the "Switching Characteristics for Output Timings versus Load Capacitance" table.

JTAG SCAN INTERFACE TIMING

(JTAG clock specification 10-MHz and 50-pF load on TDO output) (see [Figure 9](#))

| | | MIN | MAX | UNIT |
|--------------------------|---|-----|-----|------|
| $t_{c(JTAG)}$ | Cycle time, JTAG low and high period | 50 | | ns |
| $t_{su(TDI/TMS - TCKr)}$ | Setup time, TDI, TMS before TCK rise (TCKr) | 15 | | ns |
| $t_{h(TCKr - TDI/TMS)}$ | Hold time, TDI, TMS after TCKr | 15 | | ns |
| $t_{h(TCKf - TDO)}$ | Hold time, TDO after TCKf | 10 | | ns |
| $t_{d(TCKf - TDO)}$ | Delay time, TDO valid after TCK fall (TCKf) | | 45 | ns |

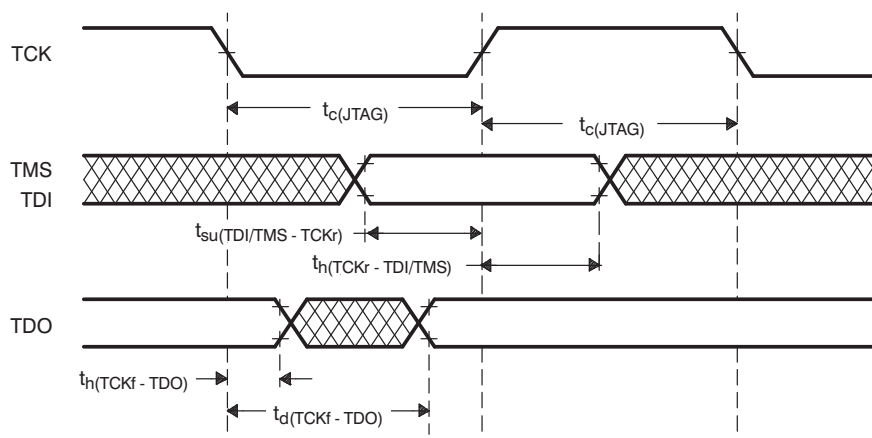


Figure 9. JTAG Scan Timings

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OUTPUT TIMINGS

Switching Characteristics for Output Timings versus Load Capacitance (C_L)

(see Figure 10)

| PARAMETER | | | MIN | MAX | UNIT |
|-----------|---|-----------------------|-----|------|------|
| t_r | Rise time, CLKOUT, AWD, TDO | $C_L = 15\text{ pF}$ | 0.5 | 2.50 | ns |
| | | $C_L = 50\text{ pF}$ | 1.5 | 5 | |
| | | $C_L = 100\text{ pF}$ | 3 | 9 | |
| | | $C_L = 150\text{ pF}$ | 4.5 | 12.5 | |
| t_f | Fall time, CLKOUT, AWD, TDO | $C_L = 15\text{ pF}$ | 0.5 | 2.5 | ns |
| | | $C_L = 50\text{ pF}$ | 1.5 | 5 | |
| | | $C_L = 100\text{ pF}$ | 3 | 9 | |
| | | $C_L = 150\text{ pF}$ | 4.5 | 12.5 | |
| t_r | Rise time, SPInCLK, SPInSOMI, SPInSIMO ⁽¹⁾ | $C_L = 15\text{ pF}$ | 2.5 | 8 | ns |
| | | $C_L = 50\text{ pF}$ | 5 | 14 | |
| | | $C_L = 100\text{ pF}$ | 9 | 23 | |
| | | $C_L = 150\text{ pF}$ | 13 | 32 | |
| t_f | Fall time, $\overline{\text{RST}}$, SPInCLK, SPInSOMI, SPInSIMO ⁽¹⁾ | $C_L = 15\text{ pF}$ | 2.5 | 8 | ns |
| | | $C_L = 50\text{ pF}$ | 5 | 14 | |
| | | $C_L = 100\text{ pF}$ | 9 | 23 | |
| | | $C_L = 150\text{ pF}$ | 13 | 32 | |
| t_r | Rise time, all other output pins | $C_L = 15\text{ pF}$ | 2.5 | 10 | ns |
| | | $C_L = 50\text{ pF}$ | 6.0 | 25 | |
| | | $C_L = 100\text{ pF}$ | 12 | 45 | |
| | | $C_L = 150\text{ pF}$ | 18 | 65 | |
| t_f | Fall time, all other output pins | $C_L = 15\text{ pF}$ | 3 | 10 | ns |
| | | $C_L = 50\text{ pF}$ | 8.5 | 25 | |
| | | $C_L = 100\text{ pF}$ | 16 | 45 | |
| | | $C_L = 150\text{ pF}$ | 23 | 65 | |

(1) Where n = 1 and 2

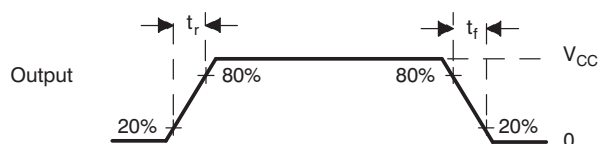


Figure 10. CMOS-Level Outputs

INPUT TIMINGS

Timing Requirements for Input Timings⁽¹⁾

(see Figure 11)

| | | MIN | MAX | UNIT |
|----------|---------------------------|--------------------|-----|------|
| t_{pw} | Input minimum pulse width | $t_{c(ICLK)} + 10$ | | ns |

(1) $t_{c(ICLK)}$ = interface clock cycle time = $1 / f_{(ICLK)}$

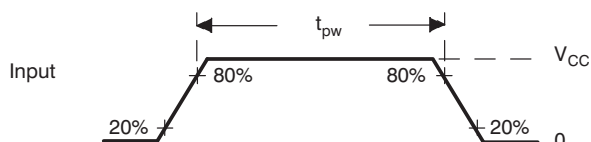


Figure 11. CMOS-Level Inputs

FLASH TIMINGS

Timing Requirements for Program Flash⁽¹⁾

| | | MIN | TYP | MAX | UNIT |
|---------------------|--|-------|-----------------|-----|---------|
| $t_{prog(16-bit)}$ | Half word (16-bit) programming time | 4 | 16 | 200 | μ s |
| $t_{prog(Total)}$ | 256K-byte programming time ⁽²⁾ | | 2 | 8 | s |
| $t_{erase(sector)}$ | Sector erase time | | 1.7 | | s |
| t_{wec} | Write/erase cycles at $T_A = -40^{\circ}\text{C}$ to 125°C | 50000 | | | cycles |
| $t_{fp(RST)}$ | Flash pump settling time from RST to SLEEP | | $167t_{c(SYS)}$ | | ns |
| $t_{fp(SLEEP)}$ | Initial flash pump settling time from SLEEP to STANDBY | | $167t_{c(SYS)}$ | | ns |
| $t_{fp(STANDBY)}$ | Initial flash pump settling time from STANDBY to ACTIVE | | $84t_{c(SYS)}$ | | ns |

(1) For more detailed information on the flash core sectors, see the flash program and erase section of this data sheet.

(2) The 256K-byte programming times include overhead of state machine.

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SPI MASTER MODE TIMING PARAMETERS

SPI Master Mode External Timing Parameters

(CLOCK PHASE = 0, SPInCLK = output, SPInSIMO = output, and SPInSOMI = input)⁽¹⁾⁽²⁾⁽³⁾ (see Figure 12)

| NO. | | | MIN | MAX | UNIT |
|------------------|----------------------|---|-------------------------|----------------------|------|
| 1 | $t_{c(SPC)M}$ | Cycle time, SPInCLK ⁽⁴⁾ | 100 | $256t_{c(ICLK)}$ | ns |
| 2 ⁽⁵⁾ | $t_{w(SPCH)M}$ | Pulse duration, SPInCLK high (clock polarity = 0) | $0.5t_{c(SPC)M} - t_r$ | $0.5t_{c(SPC)M} + 5$ | ns |
| | $t_{w(SPCL)M}$ | Pulse duration, SPInCLK low (clock polarity = 1) | $0.5t_{c(SPC)M} - t_f$ | $0.5t_{c(SPC)M} + 5$ | |
| 3 ⁽⁵⁾ | $t_{w(SPCL)M}$ | Pulse duration, SPInCLK low (clock polarity = 0) | $0.5t_{c(SPC)M} - t_f$ | $0.5t_{c(SPC)M} + 5$ | ns |
| | $t_{w(SPCH)M}$ | Pulse duration, SPInCLK high (clock polarity = 1) | $0.5t_{c(SPC)M} - t_r$ | $0.5t_{c(SPC)M} + 5$ | |
| 4 ⁽⁵⁾ | $t_{d(SPCH-SIMO)M}$ | Delay time, SPInCLK high to SPInSIMO valid (clock polarity = 0) | | 10 | ns |
| | $t_{d(SPCL-SIMO)M}$ | Delay time, SPInCLK low to SPInSIMO valid (clock polarity = 1) | | 10 | |
| 5 ⁽⁵⁾ | $t_{v(SPCL-SIMO)M}$ | Valid time, SPInSIMO data valid after SPInCLK low (clock polarity = 0) | $t_{c(SPC)M} - 5 - t_f$ | | ns |
| | $t_{v(SPCH-SIMO)M}$ | Valid time, SPInSIMO data valid after SPInCLK high (clock polarity = 1) | $t_{c(SPC)M} - 5 - t_r$ | | |
| 6 ⁽⁵⁾ | $t_{su(SOMI-SPCL)M}$ | Setup time, SPInSOMI before SPInCLK low (clock polarity = 0) | 6 | | ns |
| | $t_{su(SOMI-SPCH)M}$ | Setup time, SPInSOMI before SPInCLK high (clock polarity = 1) | 6 | | |
| 7 ⁽⁵⁾ | $t_{v(SPCL-SOMI)M}$ | Valid time, SPInSOMI data valid after SPInCLK low (clock polarity = 0) | 4 | | ns |
| | $t_{v(SPCH-SOMI)M}$ | Valid time, SPInSOMI data valid after SPInCLK high (clock polarity = 1) | 4 | | |

(1) The MASTER bit (SPInCTRL2.3) is set and the CLOCK PHASE bit (SPInCTRL2[1]) is cleared.

(2) $t_{c(ICLK)}$ = interface clock cycle time = $1 / f_{i(ICLK)}$

(3) For rise and fall timings, see the "Switching Characteristics for Output Timings versus Load Capacitance" table.

(4) When the SPI is in master mode, the following must be true:

For PS values from 1 to 255: $t_{c(SPC)M} \geq (PS + 1)t_{c(ICLK)} \geq 100$ ns, where PS is the prescale value set in the SPInCTL1[12:5] register bits.

For PS values of 0: $t_{c(SPC)M} = 2t_{c(ICLK)} \geq 100$ ns.

(5) The active edge of the SPInCLK signal referenced is controlled by the CLOCK POLARITY bit (SPInCTRL2[1]).

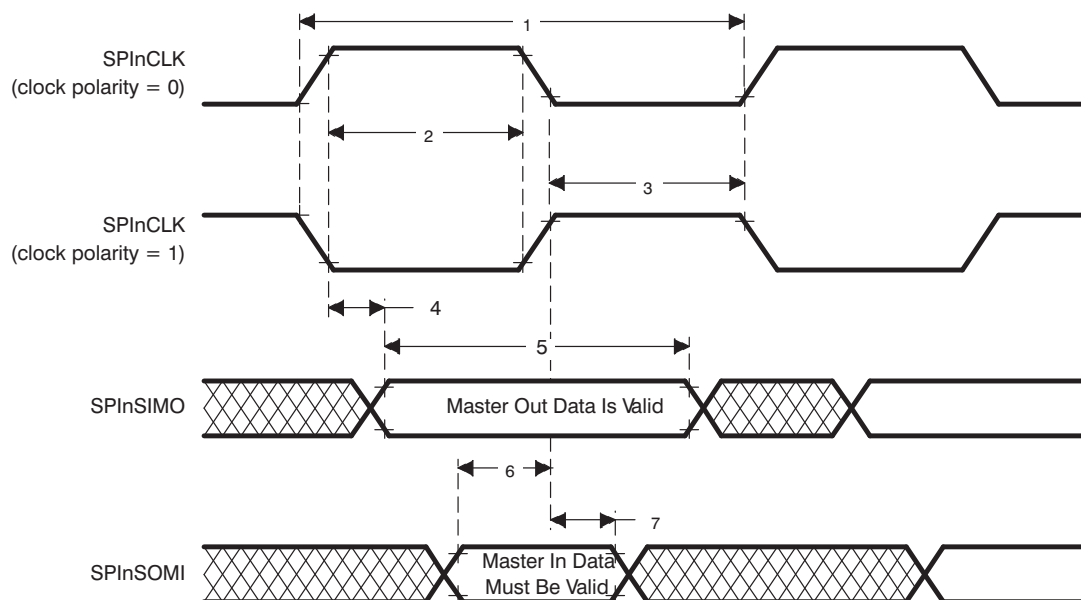


Figure 12. SPI Master Mode External Timing (CLOCK PHASE = 0)

SPI Master Mode External Timing Parameters

(CLOCK PHASE = 1, SPInCLK = output, SPInSIMO = output, and SPInSOMI = input)⁽¹⁾⁽²⁾⁽³⁾ (see Figure 13)

| NO. | | | MIN | MAX | UNIT |
|------------------|----------------------|---|-------------------------|----------------------|------|
| 1 | $t_{c(SPC)M}$ | Cycle time, SPInCLK ⁽⁴⁾ | 100 | $256t_{c(ICK)}K$ | ns |
| 2 ⁽⁵⁾ | $t_{w(SPCH)M}$ | Pulse duration, SPInCLK high (clock polarity = 0) | $0.5t_{c(SPC)M} - t_f$ | $0.5t_{c(SPC)M} + 5$ | ns |
| | $t_{w(SPCL)M}$ | Pulse duration, SPInCLK low (clock polarity = 1) | $0.5t_{c(SPC)M} - t_f$ | $0.5t_{c(SPC)M} + 5$ | |
| 3 ⁽⁵⁾ | $t_{w(SPCL)M}$ | Pulse duration, SPInCLK low (clock polarity = 0) | $0.5t_{c(SPC)M} - t_f$ | $0.5t_{c(SPC)M} + 5$ | ns |
| | $t_{w(SPCH)M}$ | Pulse duration, SPInCLK high (clock polarity = 1) | $0.5t_{c(SPC)M} - t_f$ | $0.5t_{c(SPC)M} + 5$ | |
| 4 ⁽⁵⁾ | $t_{v(SIMO-SPCH)M}$ | Valid time, SPInCLK high after SPInSIMO data valid (clock polarity = 0) | $0.5t_{c(SPC)M} - 10$ | | ns |
| | $t_{v(SIMO-SPCL)M}$ | Valid time, SPInCLK low after SPInSIMO data valid (clock polarity = 1) | $0.5t_{c(SPC)M} - 10$ | | |
| 5 ⁽⁶⁾ | $t_{v(SPCH-SIMO)M}$ | Valid time, SPInSIMO data valid after SPInCLK high (clock polarity = 0) | $t_{c(SPC)M} - 5 - t_f$ | | ns |
| | $t_{v(SPCL-SIMO)M}$ | Valid time, SPInSIMO data valid after SPInCLK low (clock polarity = 1) | $t_{c(SPC)M} - 5 - t_f$ | | |
| 6 ⁽⁶⁾ | $t_{su(SOMI-SPCH)M}$ | Setup time, SPInSOMI before SPInCLK high (clock polarity = 0) | 6 | | ns |
| | $t_{su(SOMI-SPCL)M}$ | Setup time, SPInSOMI before SPInCLK low (clock polarity = 1) | 6 | | |
| 7 ⁽⁵⁾ | $t_{v(SPCH-SOMI)M}$ | Valid time, SPInSOMI data valid after SPInCLK high (clock polarity = 0) | 4 | | ns |
| | $t_{v(SPCL-SOMI)M}$ | Valid time, SPInSOMI data valid after SPInCLK low (clock polarity = 1) | 4 | | |

(1) The MASTER bit (SPInCTRL2.3) is set and the CLOCK PHASE bit (SPInCTRL2[1]) is set.

(2) $t_{c(ICK)} = \text{interface clock cycle time} = 1 / f_{(ICK)}$

(3) For rise and fall timings, see the "Switching Characteristics for Output Timings versus Load Capacitance" table.

(4) When the SPI is in master mode, the following must be true:

For PS values from 1 to 255: $t_{c(SPC)M} \geq (PS + 1)t_{c(ICK)} \geq 100 \text{ ns}$, where PS is the prescale value set in the SPInCTL1[12:5] register bits.

For PS values of 0: $t_{c(SPC)M} = 2t_{c(ICK)} \geq 100 \text{ ns}$.

(5) The active edge of the SPInCLK signal referenced is controlled by the CLOCK POLARITY bit (SPInCTRL2[1]).

(6) The active edge of the SPInCLK signal referenced is controlled by the CLOCK POLARITY bit (SPInCTRL2[1]).

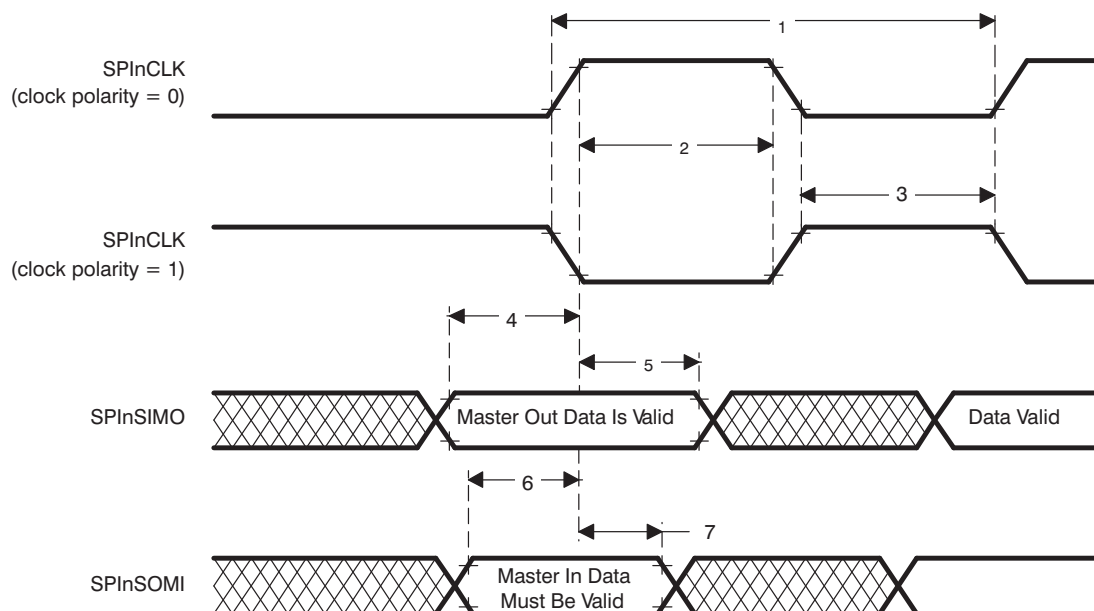


Figure 13. SPI Master Mode External Timing (CLOCK PHASE = 1)

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SPI Slave Mode Timing Parameters

SPI Slave Mode External Timing Parameters

(CLOCK PHASE = 0, SPInCLK = input, SPInSIMO = input, and SPInSOMI = output)⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾ (see Figure 14)

| NO. | | | MIN | MAX | UNIT |
|------------------|----------------------|---|------------------------------------|------------------------------------|------|
| 1 | $t_{c(SPC)}S$ | Cycle time, SPInCLK ⁽⁵⁾ | 100 | $256t_{c(ICK)}S$ | ns |
| 2 ⁽⁶⁾ | $t_{w(SPCH)}S$ | Pulse duration, SPInCLK high (clock polarity = 0) | $0.5t_{c(SPC)}S - 0.25t_{c(ICK)}S$ | $0.5t_{c(SPC)}S + 0.25t_{c(ICK)}S$ | ns |
| | $t_{w(SPCL)}S$ | Pulse duration, SPInCLK low (clock polarity = 1) | $0.5t_{c(SPC)}S - 0.25t_{c(ICK)}S$ | $0.5t_{c(SPC)}S + 0.25t_{c(ICK)}S$ | |
| 3 ⁽⁶⁾ | $t_{w(SPCL)}S$ | Pulse duration, SPInCLK low (clock polarity = 0) | $0.5t_{c(SPC)}S - 0.25t_{c(ICK)}S$ | $0.5t_{c(SPC)}S + 0.25t_{c(ICK)}S$ | ns |
| | $t_{w(SPCH)}S$ | Pulse duration, SPInCLK high (clock polarity = 1) | $0.5t_{c(SPC)}S - 0.25t_{c(ICK)}S$ | $0.5t_{c(SPC)}S + 0.25t_{c(ICK)}S$ | |
| 4 ⁽⁶⁾ | $t_{d(SPCH-SOMI)}S$ | Delay time, SPInCLK high to SPInSOMI valid (clock polarity = 0) | | $6 + t_r$ | ns |
| | $t_{d(SPCL-SOMI)}S$ | Delay time, SPInCLK low to SPInSOMI valid (clock polarity = 1) | | $6 + t_f$ | |
| 5 ⁽⁶⁾ | $t_{v(SPCH-SOMI)}S$ | Valid time, SPInSOMI data valid after SPInCLK high (clock polarity = 0) | $t_{c(SPC)}S - 6 - t_r$ | | ns |
| | $t_{v(SPCL-SOMI)}S$ | Valid time, SPInSOMI data valid after SPInCLK low (clock polarity = 1) | $t_{c(SPC)}S - 6 - t_f$ | | |
| 6 ⁽⁶⁾ | $t_{su(SIMO-SPCL)}S$ | Setup time, SPInSIMO before SPInCLK low (clock polarity = 0) | 6 | | ns |
| | $t_{su(SIMO-SPCH)}S$ | Setup time, SPInSIMO before SPInCLK high (clock polarity = 1) | 6 | | |
| 7 ⁽⁶⁾ | $t_{v(SPCL-SIMO)}S$ | Valid time, SPInSIMO data valid after SPInCLK low (clock polarity = 0) | 6 | | ns |
| | $t_{v(SPCH-SIMO)}S$ | Valid time, SPInSIMO data valid after SPInCLK high (clock polarity = 1) | 6 | | |

(1) The MASTER bit (SPInCTRL2.3) is cleared and the CLOCK PHASE bit (SPInCTRL2[1]) is cleared.

(2) If the SPI is in slave mode, the following must be true: $t_{c(SPC)}S \geq (PS + 1)t_{c(ICK)}S$, where PS = prescale value set in SPInCTL1[12:5].

(3) For rise and fall timings, see the "Switching Characteristics for Output Timings versus Load Capacitance" table.

(4) $t_{c(ICK)}S$ = interface clock cycle time = $1/f_{(ICK)}$

(5) When the SPIn is in slave mode, the following must be true:

For PS values from 1 to 255: $t_{c(SPC)}S \geq (PS + 1)t_{c(ICK)}S \geq 100$ ns, where PS is the prescale value set in the SPInCTL1[12:5] register bits.

For PS values of 0: $t_{c(SPC)}S = 2t_{c(ICK)}S \geq 100$ ns.

(6) The active edge of the SPInCLK signal referenced is controlled by the CLOCK POLARITY bit (SPInCTRL2[1]).

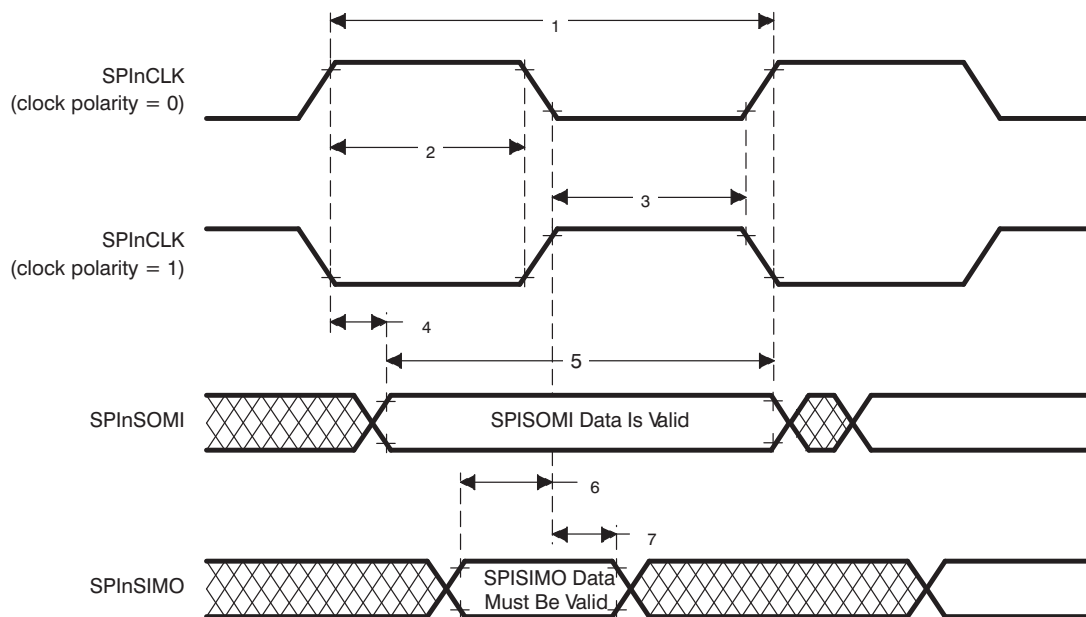


Figure 14. SPIn Slave Mode External Timing (CLOCK PHASE = 0)

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SPI Slave Mode External Timing Parameters

(CLOCK PHASE = 1, SPInCLK = input, SPInSIMO = input, and SPInSOMI = output) ⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾ (see Figure 15)

| NO. | | | MIN | MAX | UNIT |
|------------------|----------------------|---|------------------------------------|------------------------------------|------|
| 1 | $t_{c(SPC)}S$ | Cycle time, SPInCLK ⁽⁵⁾ | 100 | $256t_{c(ICLK)}$ | ns |
| 2 ⁽⁶⁾ | $t_{w(SPCH)}S$ | Pulse duration, SPInCLK high (clock polarity = 0) | $0.5t_{c(SPC)}S - 0.25t_{c(ICLK)}$ | $0.5t_{c(SPC)}S + 0.25t_{c(ICLK)}$ | ns |
| | $t_{w(SPCL)}S$ | Pulse duration, SPInCLK low (clock polarity = 1) | $0.5t_{c(SPC)}S - 0.25t_{c(ICLK)}$ | $0.5t_{c(SPC)}S + 0.25t_{c(ICLK)}$ | |
| 3 ⁽⁶⁾ | $t_{w(SPCL)}S$ | Pulse duration, SPInCLK low (clock polarity = 0) | $0.5t_{c(SPC)}S - 0.25t_{c(ICLK)}$ | $0.5t_{c(SPC)}S + 0.25t_{c(ICLK)}$ | ns |
| | $t_{w(SPCH)}S$ | Pulse duration, SPInCLK high (clock polarity = 1) | $0.5t_{c(SPC)}S - 0.25t_{c(ICLK)}$ | $0.5t_{c(SPC)}S + 0.25t_{c(ICLK)}$ | |
| 4 ⁽⁶⁾ | $t_{v(SOMI-SPCH)}S$ | Valid time, SPInCLK high after SPInSOMI data valid (clock polarity = 0) | $0.5t_{c(SPC)}S - 6 - t_r$ | | ns |
| | $t_{v(SOMI-SPCL)}S$ | Valid time, SPInCLK low after SPInSOMI data valid (clock polarity = 1) | $0.5t_{c(SPC)}S - 6 - t_f$ | | |
| 5 ⁽⁶⁾ | $t_{v(SPCH-SOMI)}S$ | Valid time, SPInSOMI data valid after SPInCLK high (clock polarity = 0) | $0.5t_{c(SPC)}S - 6 - t_r$ | | ns |
| | $t_{v(SPCL-SOMI)}S$ | Valid time, SPInSOMI data valid after SPInCLK low (clock polarity = 1) | $0.5t_{c(SPC)}S - 6 - t_f$ | | |
| 6 ⁽⁶⁾ | $t_{su(SIMO-SPCH)}S$ | Setup time, SPInSIMO before SPInCLK high (clock polarity = 0) | 6 | | ns |
| | $t_{su(SIMO-SPCL)}S$ | Setup time, SPInSIMO before SPInCLK low (clock polarity = 1) | 6 | | |
| 7 ⁽⁶⁾ | $t_{v(SPCH-SIMO)}S$ | Valid time, SPInSIMO data valid after SPInCLK high (clock polarity = 0) | 6 | | ns |
| | $t_{v(SPCL-SIMO)}S$ | Valid time, SPInSIMO data valid after SPInCLK low (clock polarity = 1) | 6 | | |

(1) The MASTER bit (SPInCTRL2.3) is cleared and the CLOCK PHASE bit (SPInCTRL2[1]) is set.

(2) If the SPI is in slave mode, the following must be true: $t_{c(SPC)}S \geq (PS + 1)t_{c(ICLK)}$, where PS = prescale value set in SPInCTL1[12:5].

(3) For rise and fall timings, see the "Switching Characteristics for Output Timings versus Load Capacitance" table.

(4) $t_{c(ICLK)}$ = interface clock cycle time = $1/f_{ICLK}$

(5) When the SPIn is in slave mode, the following must be true:

For PS values from 1 to 255: $t_{c(SPC)}S \geq (PS + 1)t_{c(ICLK)} \geq 100$ ns, where PS is the prescale value set in the SPInCTL1[12:5] register bits.

For PS values of 0: $t_{c(SPC)}S = 2t_{c(ICLK)} \geq 100$ ns.

(6) The active edge of the SPInCLK signal referenced is controlled by the CLOCK POLARITY bit (SPInCTRL2[1]).

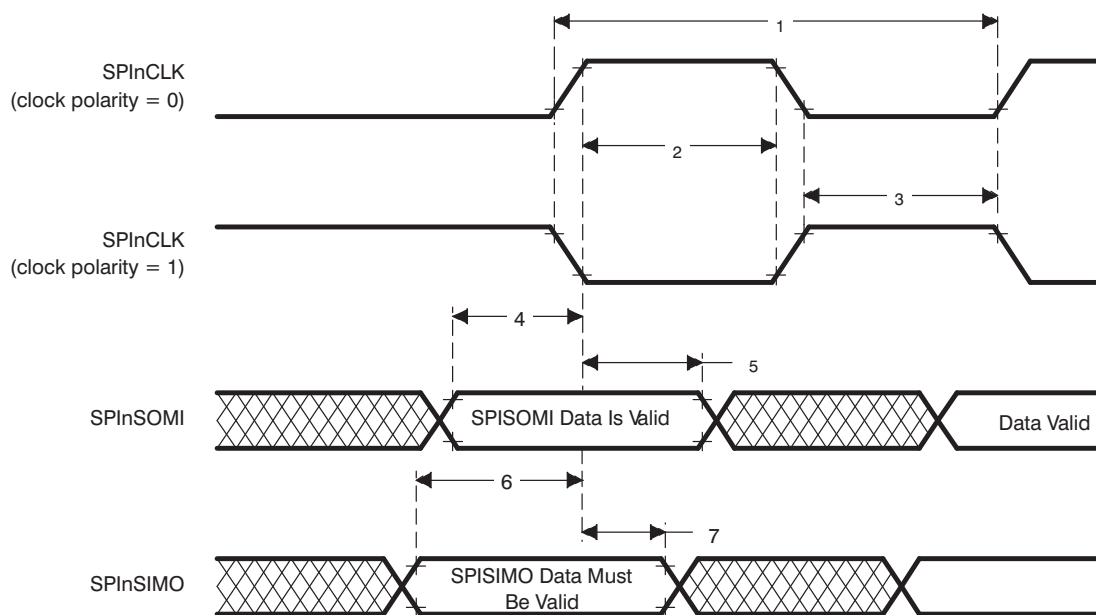


Figure 15. SPIn Slave Mode External Timing (CLOCK PHASE = 1)

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SCIn ISOSYNCHRONOUS MODE TIMINGS INTERNAL CLOCK

Timing Requirements for Internal Clock SCIn Isosynchronous Mode⁽¹⁾⁽²⁾⁽³⁾

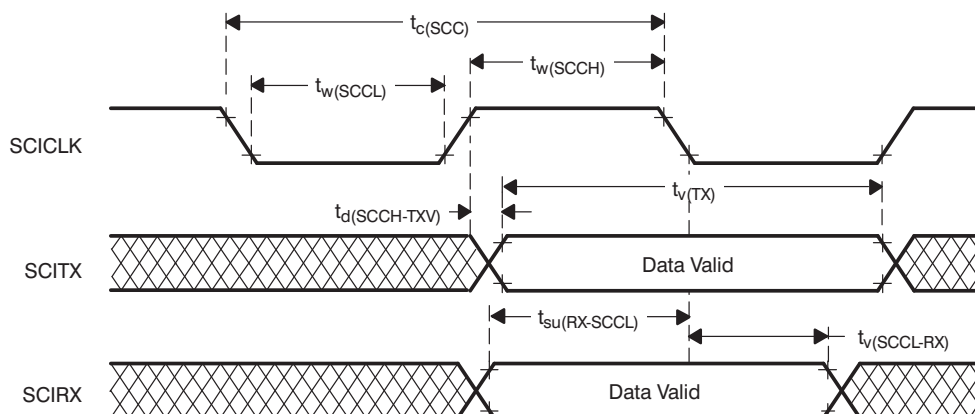
(see Figure 16)

| | | (BAUD + 1) IS EVEN OR BAUD = 0 | | (BAUD + 1) IS ODD AND BAUD ≠ 0 | | UNIT |
|-------------------|---|-----------------------------------|----------------------|---|-----------------------------------|------|
| | | MIN | MAX | MIN | MAX | |
| $t_{c(SCC)}$ | Cycle time, SCInCLK | $2t_{c(ICKLK)}$ | $2^{24}t_{c(ICKLK)}$ | $3t_{c(ICKLK)}$ | $(2^{24} - 1)t_{c(ICKLK)}$ | ns |
| $t_{w(SCCL)}$ | Pulse duration, SCInCLK low | $0.5t_{c(SCC)} - t_f$ | $0.5t_{c(SCC)} + 5$ | $0.5t_{c(SCC)} + 0.5t_{c(ICKLK)} - t_f$ | $0.5t_{c(SCC)} + 0.5t_{c(ICKLK)}$ | ns |
| $t_{w(SCCH)}$ | Pulse duration, SCInCLK high | $0.5t_{c(SCC)} - t_r$ | $0.5t_{c(SCC)} + 5$ | $0.5t_{c(SCC)} - 0.5t_{c(ICKLK)} - t_r$ | $0.5t_{c(SCC)} - 0.5t_{c(ICKLK)}$ | ns |
| $t_{d(SCCH-TXV)}$ | Delay time, SCInCLK high to SCInTX valid | | 10 | | 10 | ns |
| $t_{v(TX)}$ | Valid time, SCInTX data after SCInCLK low | $t_{c(SCC)} - 10$ | | $t_{c(SCC)} - 10$ | | ns |
| $t_{su(RX-SCCL)}$ | Setup time, SCInRX before SCInCLK low | $t_{c(ICKLK)} + t_f + 20$ | | $t_{c(ICKLK)} + t_f + 20$ | | ns |
| $t_{v(SCCL-RX)}$ | Valid time, SCInRX data after SCInCLK low | $-t_{c(ICKLK)} + t_f + 20$ | | $-t_{c(ICKLK)} + t_f + 20$ | | ns |

(1) BAUD = 24-bit concatenated value formed by the SCI[H,M,L]BAUD registers.

(2) $t_{c(ICKLK)}$ = interface clock cycle time = $1 / f_{(ICKLK)}$

(3) For rise and fall timings, see the "Switching Characteristics for Output Timings versus Load Capacitance" table.



- A. Data transmission/reception characteristics for isosynchronous mode with internal clocking are similar to the asynchronous mode. Data transmission occurs on the SCICLK rising edge, and data reception occurs on the SCICLK falling edge.

Figure 16. SCIn Isosynchronous Mode Timing Diagram for Internal Clock

SCIn ISOSYNCHRONOUS MODE TIMINGS EXTERNAL CLOCK

Timing Requirements for External Clock SCIn Isosynchronous Mode⁽¹⁾⁽²⁾

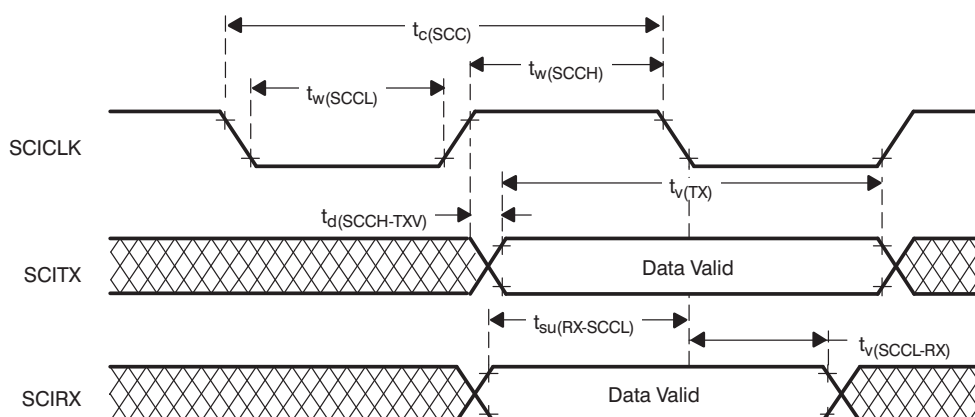
(see Figure 17)

| | | MIN | MAX | UNIT |
|-------------------|---|-----------------------------------|-----------------------------------|------|
| $t_{c(SCC)}$ | Cycle time, SCInCLK ⁽³⁾ | $8t_{c(ICKL)}$ | | ns |
| $t_{w(SCCH)}$ | Pulse duration, SCInCLK high | $0.5t_{c(SCC)} - 0.25t_{c(ICKL)}$ | $0.5t_{c(SCC)} + 0.25t_{c(ICKL)}$ | ns |
| $t_{w(SCCL)}$ | Pulse duration, SCInCLK low | $0.5t_{c(SCC)} - 0.25t_{c(ICKL)}$ | $0.5t_{c(SCC)} + 0.25t_{c(ICKL)}$ | ns |
| $t_{d(SCCH-TXV)}$ | Delay time, SCInCLK high to SCInTX valid | | $2t_{c(ICKL)} + 12 + t_r$ | ns |
| $t_{v(TX)}$ | Valid time, SCInTX data after SCInCLK low | $2t_{c(SCC)} - 10$ | | ns |
| $t_{su(RX-SCCL)}$ | Setup time, SCInRX before SCInCLK low | 0 | | ns |
| $t_{v(SCCL-RX)}$ | Valid time, SCInRX data after SCInCLK low | $2t_{c(ICKL)} + 10$ | | ns |

(1) $t_{c(ICKL)}$ = interface clock cycle time = $1 / f_{(ICKL)}$

(2) For rise and fall timings, see the "Switching Characteristics for Output Timings versus Load Capacitance" table.

(3) When driving an external SCInCLK, the following must be true: $t_{c(SCC)} \geq 8t_{c(ICKL)}$



- A. Data transmission / reception characteristics for isosynchronous mode with external clocking are similar to the asynchronous mode. Data transmission occurs on the SCInCLK rising edge, and data reception occurs on the SCInCLK falling edge.

Figure 17. SCIn Isosynchronous Mode Timing Diagram for External Clock

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HIGH-END TIMER (HET) TIMINGS

Minimum PWM Output Pulse Width:

This is equal to one high resolution clock period (HRP). The HRP is defined by the 6-bit high resolution prescale factor (hr), which is user defined, giving prescale factors of 1 to 64, with a linear increment of codes.

Therefore, the minimum PWM output pulse width = $HRP(\min) = hr(\min)/SYSCLK = 1/SYSCLK$

For example, for a SYSCLK of 30 MHz, the minimum PWM output pulse width = $1/30 = 33.33\text{ns}$

Minimum Input Pulses that Can Be Captured:

The input pulse width must be greater or equal to the low resolution clock period (LRP), i.e., the HET loop (the HET program must fit within the LRP). The LRP is defined by the 3-bit loop-resolution prescale factor (lr), which is user defined, with a power of 2 increment of codes. That is, the value of lr can be 1, 2, 4, 8, 16, or 32.

Therefore, the minimum input pulse width = $LRP(\min) = hr(\min) * lr(\min)/SYSCLK = 1 * 1/SYSCLK$

For example, with a SYSCLK of 30 MHz, the minimum input pulse width = $1 * 1/30 = 33.33\text{ ns}$

NOTE:

Once the input pulse width is greater than LRP, the resolution of the measurement is still HRP. (That is, the captured value gives the number of HRP clocks inside the pulse.)

Abbreviations:

hr = HET high resolution divide rate = 1, 2, 3,...63, 64

lr = HET low resolution divide rate = 1, 2, 4, 8, 16, 32

High resolution clock period = $HRP = hr/SYSCLK$

Loop resolution clock period = $LRP = hr*lr/SYSCLK$

STANDARD CAN CONTROLLER (SCC) MODE TIMINGS

Dynamic Characteristics for the CANSTX and CANSRX Pins

| PARAMETER | | MIN | MAX | UNIT |
|----------------------|--|-----|-----|------|
| $t_d(\text{CANSTX})$ | Delay time, transmit shift register to CANSTX pin ⁽¹⁾ | | 15 | ns |
| $t_d(\text{CANSRX})$ | Delay time, CANSRX pin to receive shift register | | 5 | ns |

(1) These values do not include the rise/fall times of the output buffer.

MULTI-BUFFERED A-TO-D CONVERTER (MibADC)

The multi-buffered A-to-D converter (MibADC) has a separate power bus for its analog circuitry. This power bus enhances the A-to-D performance by preventing digital switching noise on the logic circuitry which could be present on VSS and VCC from coupling into the A-to-D analog stage. All A-to-D specifications are given with respect to ADREFLO unless otherwise noted.

| | |
|------------------------|---|
| Resolution | 10 bits (1024 values) |
| Monotonic | Assured |
| Output conversion code | 00h to 3FFh [00 for $V_{AI} \leq AD_{REFLO}$; 3FF for $V_{AI} \geq AD_{REFHI}$] |

Table 17. MibADC Recommended Operating Conditions⁽¹⁾

| | | MIN | MAX | UNIT |
|---------------------|---|-------------------------|-------------------------|------|
| AD _{REFHI} | A-to-D high-voltage reference source | V _{SSAD} | V _{CCAD} | V |
| AD _{REFLO} | A-to-D low-voltage reference source | V _{SSAD} | V _{CCAD} | V |
| V _{AI} | Analog input voltage | V _{SSAD} - 0.3 | V _{CCAD} + 0.3 | V |
| I _{AIC} | Analog input clamp current ⁽²⁾ (V _{AI} < V _{SSAD} - 0.3 or V _{AI} > V _{CCAD} + 0.3) | -2 | 2 | mA |

- (1) For V_{CCAD} and V_{SSAD} recommended operating conditions, see the "Device Recommended Operating Conditions" table.
(2) Input currents into any ADC input channel outside the specified limits could affect conversion results of other channels.

Table 18. Operating Characteristics over Full Ranges of Recommended Operating Conditions⁽¹⁾⁽²⁾

| PARAMETER | | DESCRIPTION/CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------|--|---|-----|-----|-----|------|
| R _i | Analog input resistance | See Figure 18. | | 250 | 500 | Ω |
| C _i | Analog input capacitance | See Figure 18. | | | 10 | pF |
| | | Conversion | | | 30 | pF |
| I _{AIL} | Analog input leakage current | See Figure 18. | -1 | | 1 | μA |
| I _{ADREFHI} | AD _{REFHI} input current | AD _{REFHI} = 3.6 V, AD _{REFLO} = V _{SSAD} | | | 5 | mA |
| CR | Conversion range over which specified accuracy is maintained | AD _{REFHI} - AD _{REFLO} | 3 | | 3.6 | V |
| E _{DNL} | Differential nonlinearity error | Difference between the actual step width and the ideal value after offset correction. See Figure 19. | | | ±2 | LSB |
| E _{INL} | Integral nonlinearity error | Maximum deviation from the best straight line through the MibADC. MibADC transfer characteristics, excluding the quantization error after offset correction. See Figure 20. | | | ±2 | LSB |
| E _{TOT} | Total error/Absolute accuracy | Maximum value of the difference between an analog value and the ideal midstep value. See Figure 21. | | | ±2 | LSB |

- (1) V_{CCIO} = V_{CCAD} = AD_{REFHI}
(2) 1 LSB = (AD_{REFHI} - AD_{REFLO})/2¹⁰ for the MibADC

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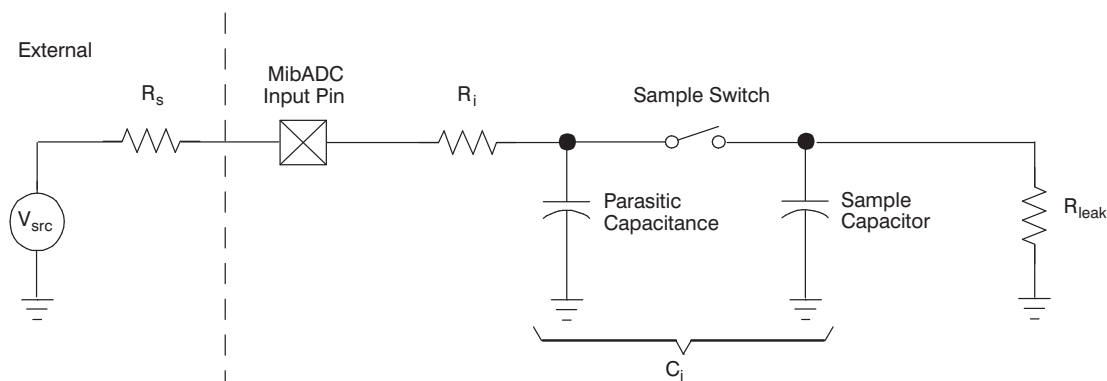


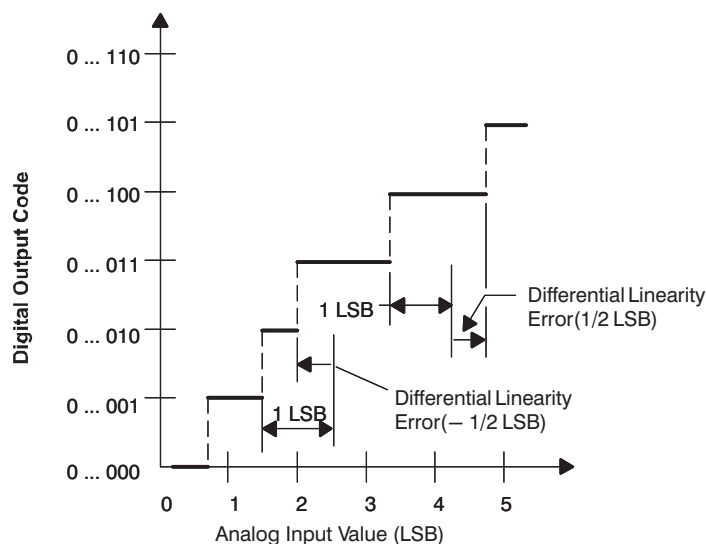
Figure 18. MibADC Input Equivalent Circuit

Table 19. Multi-Buffer ADC Timing Requirements

| | | MIN | MAX | UNIT |
|--------------------|---|------|-----|---------|
| $t_{c(ADCLK)}$ | Cycle time, MibADC clock | 0.05 | | μs |
| $t_{d(SH)}$ | Delay time, sample and hold time | 1 | | μs |
| $t_{d(C)}$ | Delay time, conversion time | 0.55 | | μs |
| $t_{d(SHC)}^{(1)}$ | Delay time, total sample/hold and conversion time | 1.55 | | μs |

(1) This is the minimum sample/hold and conversion time that can be achieved. These parameters are dependent on many factors for more detail; see the *TMS470R1x Multi-Buffered Analog-to-Digital Converter (MibADC) Reference Guide* (literature number SPNU206).

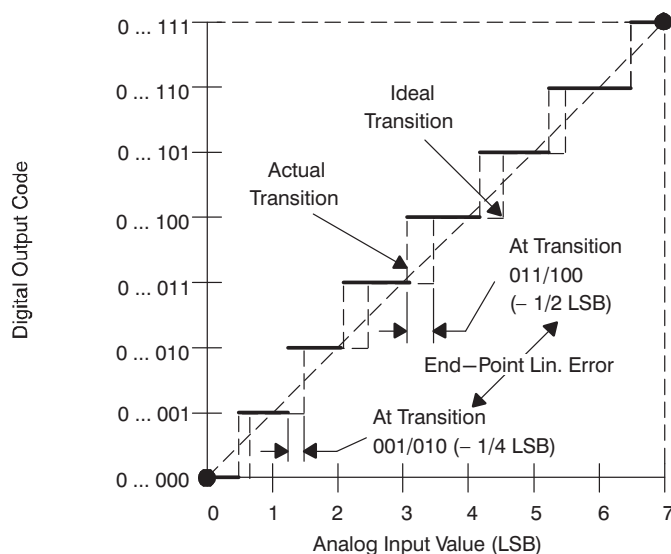
The differential nonlinearity error shown in Figure 19 (sometimes referred to as differential linearity) is the difference between an actual step width and the ideal value of 1 LSB.



A. $1 \text{ LSB} = (AD_{REFHI} - AD_{REFLO})/2^{10}$

Figure 19. Differential Nonlinearity (DNL)

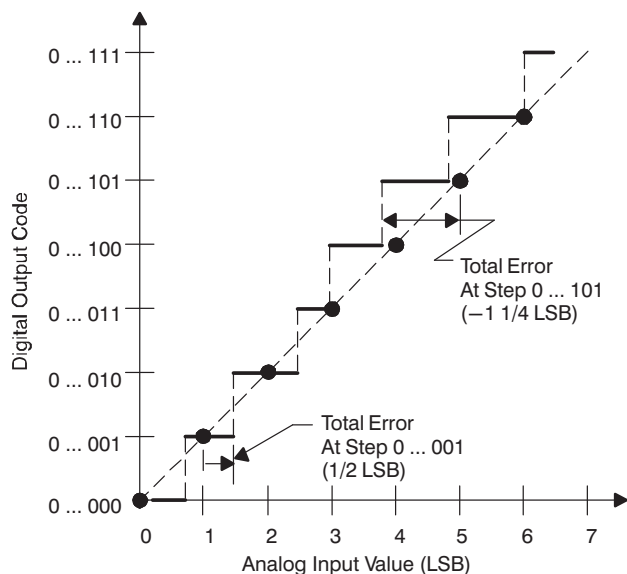
The integral nonlinearity error shown in Figure 20 (sometimes referred to as linearity error) is the deviation of the values on the actual transfer function from a straight line.



A. $1 \text{ LSB} = (AD_{\text{REFHI}} - AD_{\text{REFLO}})/2^{10}$

Figure 20. Integral Nonlinearity (INL) Error

The absolute accuracy or total error of an MibADC as shown in Figure 21 is the maximum value of the difference between an analog value and the ideal midstep value.



A. $1 \text{ LSB} = (AD_{\text{REFHI}} - AD_{\text{REFLO}})/2^{10}$

Figure 21. Absolute Accuracy (Total) Error

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THERMAL CHARACTERISTICS

| PARAMETER | °C/W |
|-----------------|------|
| $R_{\theta JA}$ | 51 |
| $R_{\theta JC}$ | 5 |

REVISION HISTORY

This revision history highlights the changes made to the device-specific datasheet SPNS100.

Table 7. Revision History

| |
|---|
| SPNS100A to SPNS100B |
| Revised the Family Nomenclature drawing, Figure 2 , to add Q version of the temperature range. |
| Revised "Absolute Maximum Ratings" table to add Q version of the temperature range. |
| Revised "Device Recommended Operating Conditions" table to add Q version of the temperature range. |
| Added note to $\overline{\text{PORRST}}$ Timing Diagram. |
| Changed T_A range to -40°C to 125°C on t_{wec} in "Timing Requirements for Program Flash" table. |
| Added t_{wec} MIN value of 50000 and deleted MAX value in "Timing Requirements for Program Flash" table. |
| Changed $t_{\text{erase(sector)}}$ TYP value to 1.7 and removed MAX value in "Timing Requirements for Program Flash" table. |
| SPNS100 to SPNS100A |
| Changed Figure 2 , the Family Nomenclature drawing, to reflect T version of the temperature range. |
| Revised "Absolute Maximum Ratings over Operating Free-Air Temperature Range" table to show T version of the temperature range. |
| Revised "Device Recommended Operating Conditions" table to show T version of the temperature range. |
| Added "Device and Development-Support Tool Nomenclature" information. |
| Changed VCC to 2.06 V in the ICC in the "Electrical Characteristics over Recommended Operating Free-Air Temperature Range" table. |
| Changed the max for the I_{CC} Digital supply current (operating mode) at $\text{SYSCLK} = 48 \text{ MHz}$ from 75 to 70 mA. |
| Corrected V_{CCPORE} to V_{CCPORL} in "Timing Requirements for $\overline{\text{PORRST}}$ " table. |
| Moved 2.75 from Max to Min column for V_{CCIOPORH} in "Timing Requirements for $\overline{\text{PORRST}}$ " table. |
| Added row for T_{fsu} to "Switching Characteristics over Recommended Operating Conditions for $\overline{\text{RST}}$ " table. |
| Added rows for $T_{\text{fp(RST)}}$, $T_{\text{fp(SLEEP)}}$, and $T_{\text{fp(STANDBY)}}$ to "Flash Timings" table. |

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| TMS470R1A256PZ-T | NRND | LQFP | PZ | 100 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

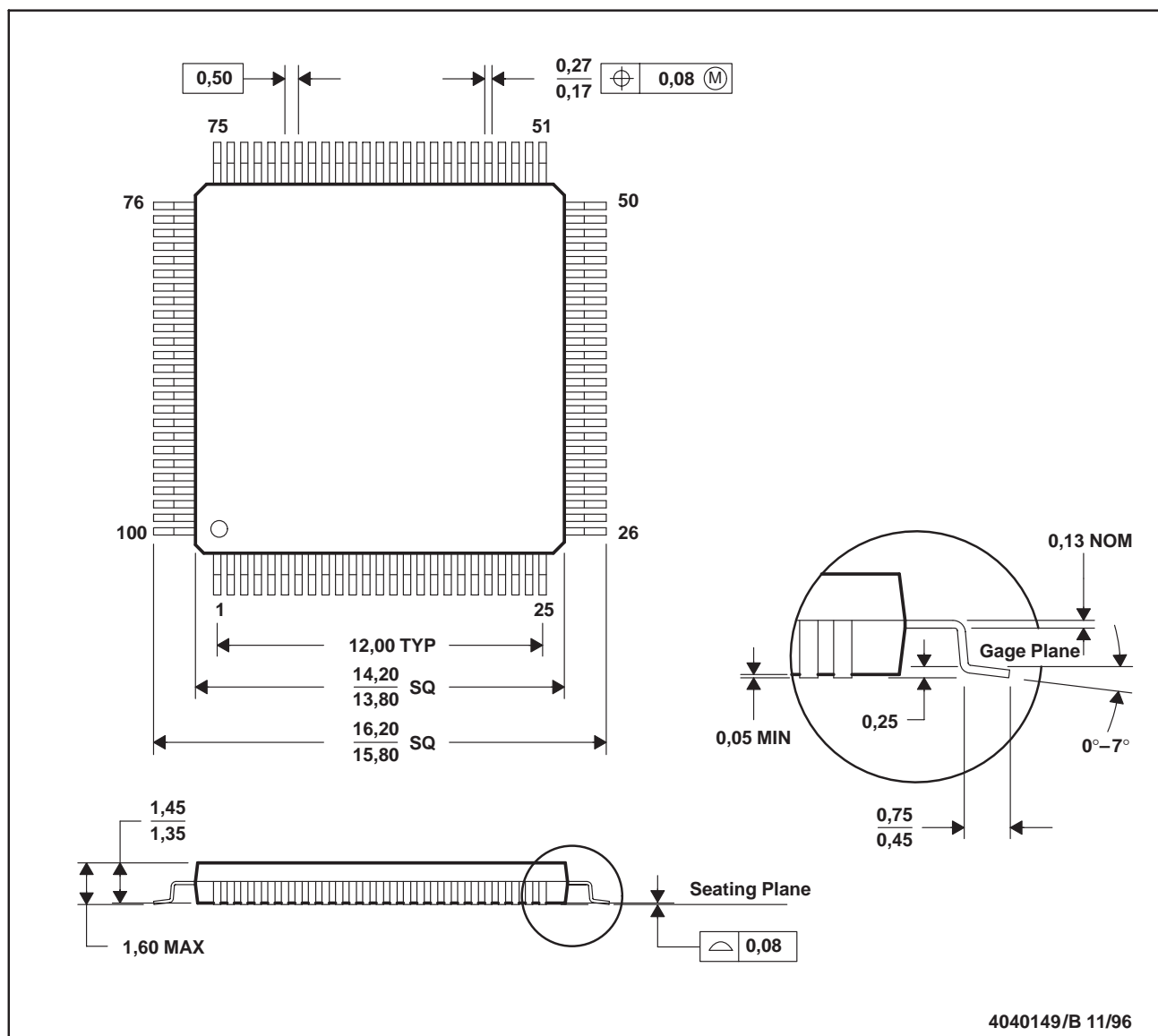
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MTQF013A – OCTOBER 1994 – REVISED DECEMBER 1996

PZ (S-PQFP-G100)

PLASTIC QUAD FLATPACK



- NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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