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# STS12NH3LL

N-channel 30 V - 0.008 Ω - 12 A - SO-8  
 ultra low gate charge STripFET™ Power MOSFET

## Features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STS12NH3LL	30 V	<0.0105 Ω	12 A

- Optimal R<sub>DS(on)</sub> x Qg trade-off @ 4.5 V
- Switching losses reduced
- Low input capacitance
- Low threshold device

## Application

- Switching applications

## Description

This series is based on the latest generation of ST's proprietary "STripFET™" technology. An innovative layout enables the device to also exhibit extremely low gate charge for the most demanding requirements as high-side switch in high-frequency DC-DC converters. It's therefore ideal for high-density converters in telecom and computer applications.

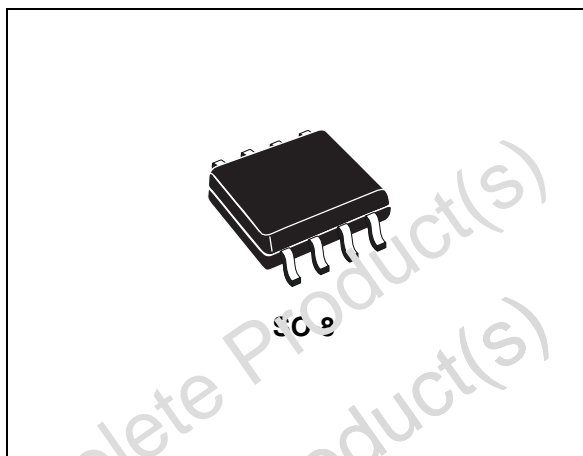


Figure 1. Internal schematic diagram

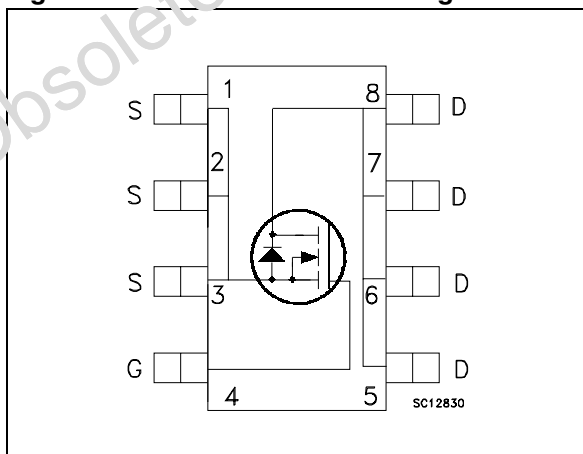


Table 1. Device summary

Order code	Marking	Packag	Packaging
STS12NH3LL	12H3LL	SO-8	Tape & reel

## Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	30	V
$V_{GS}^{(1)}$	Gate-source voltage	$\pm 16$	V
$V_{GS}^{(2)}$	Gate-source voltage	$\pm 18$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	12	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	7.5	A
$I_{DM}^{(3)}$	Drain current (pulsed)	48	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	2.7	W
$T_J$ $T_{stg}$	Operating junction temperature Storage temperature	-55 to 150	$^\circ\text{C}$

1. Continuous mode
2. Guaranteed for test time  $\leq 15\text{ ms}$
3. Pulse width limited by safe operating area

**Table 3. Thermal resistance**

Symbol	Parameter	Value	Unit
$R_{thj-amb}^{(1)}$	Thermal resistance junction-ambient	47	$^\circ\text{C/W}$

1. When mounted on FR-4 board of 1inch<sup>2</sup>, 2oz Cu,  $t < 10\text{ sec}$

Electrical characteristics

STS12NH3LL

## 2 Electrical characteristics

(T<sub>CASE</sub>=25°C unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0	30			V
I <sub>DSS</sub>	Zero gate voltage drain current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max rating, V <sub>DS</sub> = Max rating @ 125 °C			1 10	μA μA
I <sub>GSS</sub>	Gate body leakage current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ±16 V			100	nA
V <sub>GS(th)</sub>	Gate threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1			V
R <sub>DS(on)</sub>	Static drain-source on resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 6 A V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 6 A		0.008 0.010	0.0105 0.013	Ω Ω

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub>	Forward transconductance	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 12 A		38		S
C <sub>iss</sub>	Input capacitance	V <sub>DS</sub> = 25 V, f = 1 MHz, V <sub>GS</sub> = 0		965		pF
C <sub>oss</sub>	Output capacitance			285		pF
C <sub>rss</sub>	Reverse transfer capacitance			38		pF
Q <sub>g</sub>	Total gate charge	V <sub>DD</sub> = 15 V, I <sub>D</sub> = 12 A		9	12	nC
Q <sub>gs</sub>	Gate-source charge	V <sub>GS</sub> = 4.5 V		3.7		nC
Q <sub>gd</sub>	Gate-drain charge	(see Figure 20)		3		nC
Q <sub>gs1</sub>	Pre V <sub>th</sub> gate-to-source charge	V <sub>DD</sub> = 15 V, I <sub>D</sub> = 12 A V <sub>GS</sub> = 4.5 V		2.5		nC
Q <sub>gs2</sub>	Post V <sub>th</sub> gate-to-source charge	(see Figure 20)		1.2		nC
R <sub>G</sub>	Gate Input Resistance	f = 1 MHz Gate DC Bias = 0 Test signal level = 20 mV open drain	0.5	1.5	2.5	Ω

**STS12NH3LL**
**Electrical characteristics**
**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD}=15\text{ V}$ , $I_D=6\text{ A}$ , $R_G=4.7\ \Omega$ , $V_{GS}=4.5\text{ V}$ <i>(see Figure 14)</i>		15		ns
$t_r$	Rise time			32		ns
$t_{d(off)}$	Turn-off delay time			18		ns
$t_f$	Fall time			8.5		ns

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$I_{SD}$	Source-drain current				2	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				48	A
$V_{SD}^{(2)}$	Forward on Voltage	$I_{SD}=12\text{ A}$ , $V_{GS}=0$			1.3	V
$t_{rr}$	Reverse recovery time	$I_{SD}=12\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD}=20\text{ V}$ , $T_J=150\text{ }^\circ\text{C}$ <i>(see Figure 16)</i>		24		ns
$Q_{rr}$	Reverse recovery charge			17.4		nC
$I_{RRM}$	Reverse recovery current			1.45		A

1. Pulse width limited by safe operating area

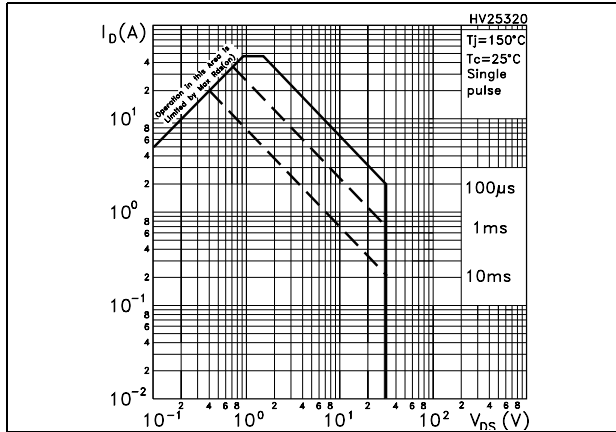
 2. Pulsed: pulse duration=300  $\mu\text{s}$ , duty cycle 1.5%

**Electrical characteristics**

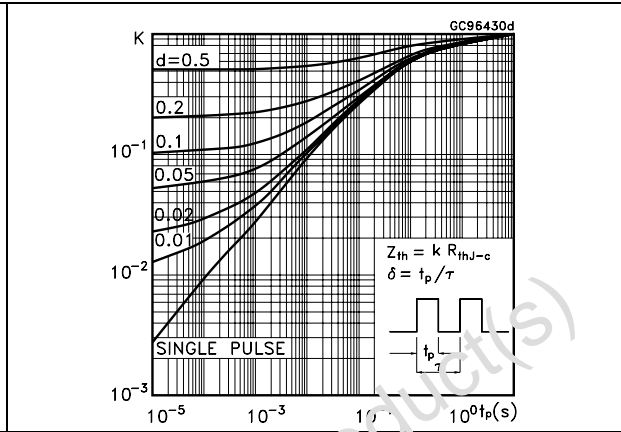
**STS12NH3LL**

**2.1 Electrical characteristics (curves)**

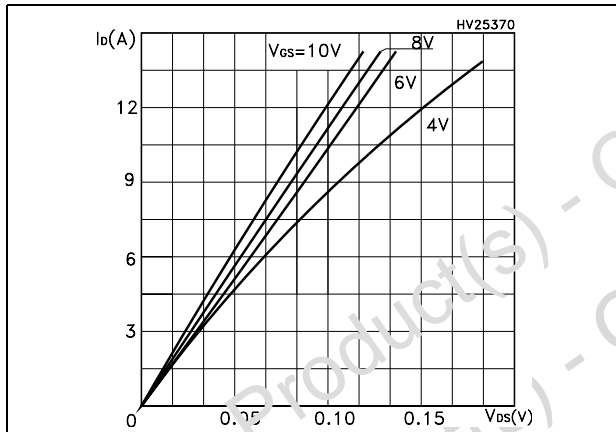
**Figure 2. Safe operating area**



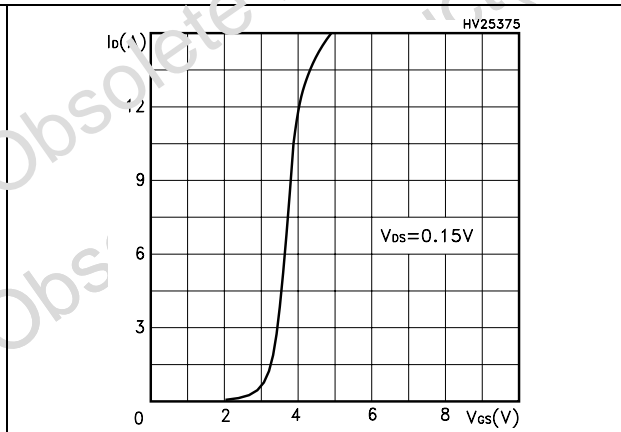
**Figure 3. Thermal impedance**



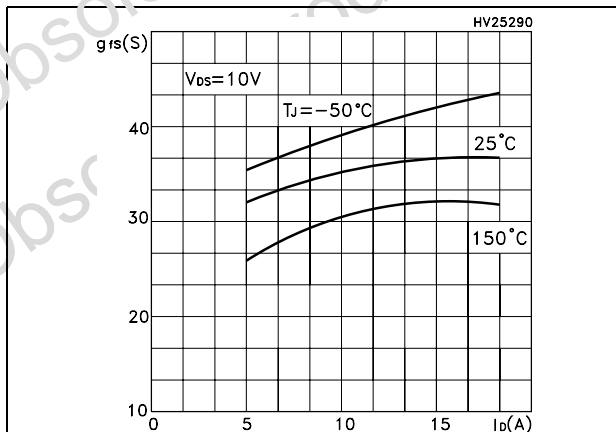
**Figure 4. Output characteristics**



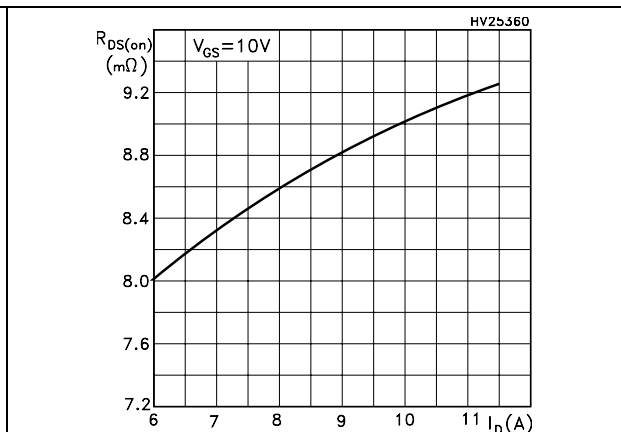
**Figure 5. Transfer characteristics**



**Figure 6. Transconductance**



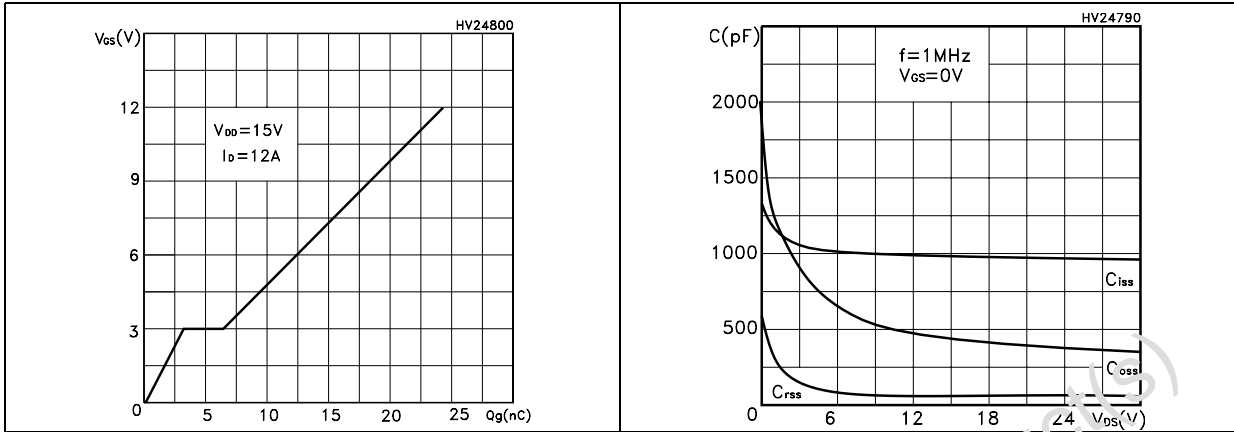
**Figure 7. Static drain-source on resistance**



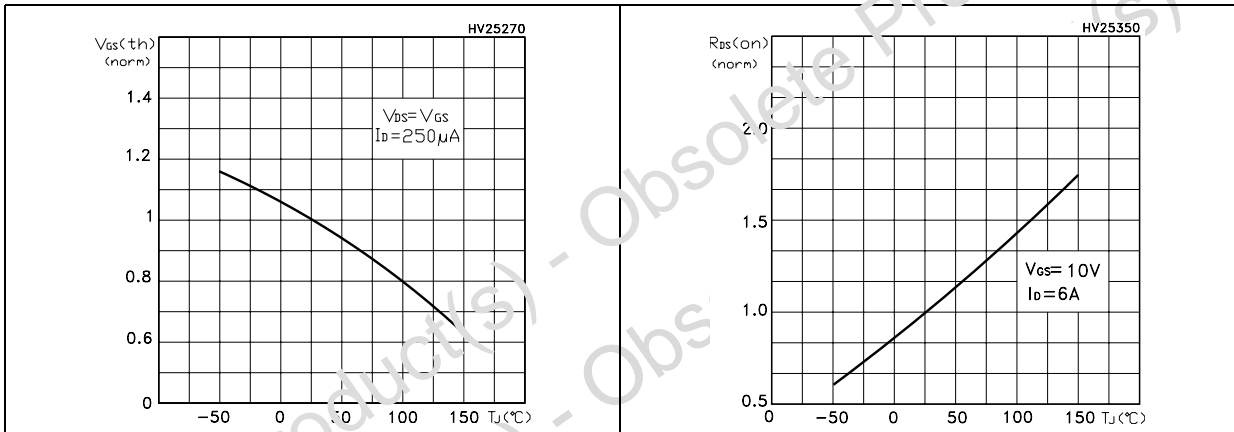
**STS12NH3LL**

**Electrical characteristics**

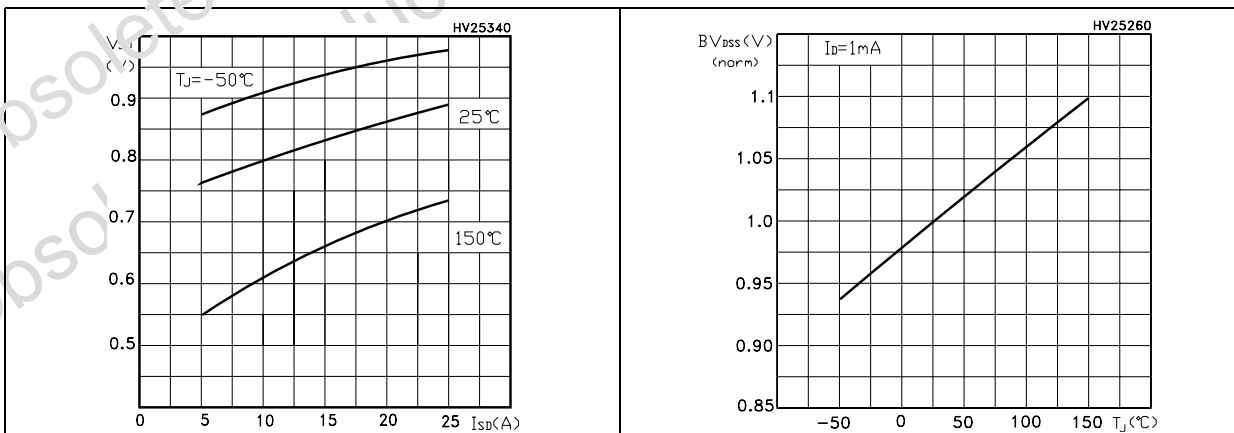
**Figure 8. Gate charge vs gate-source voltage** **Figure 9. Capacitance variations**



**Figure 10. Normalized gate threshold voltage vs temperature** **Figure 11. Normalized on resistance vs temperature**



**Figure 12. Source-drain diode forward characteristics** **Figure 13. Normalized  $B_{V_{DS}}$  vs temperature**



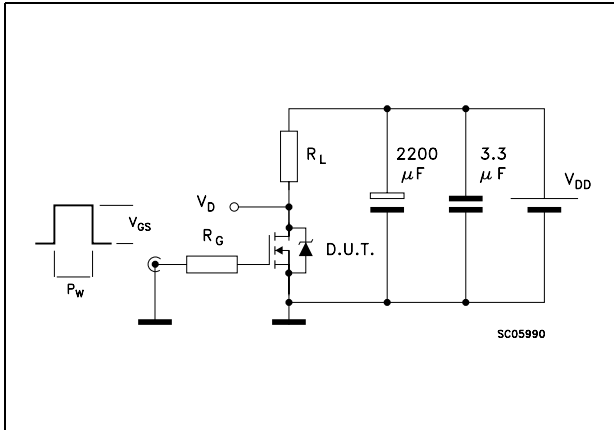


**Test circuit**

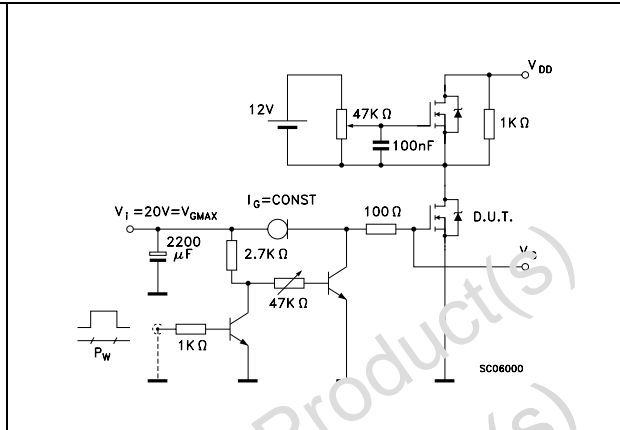
**STS12NH3LL**

**3 Test circuit**

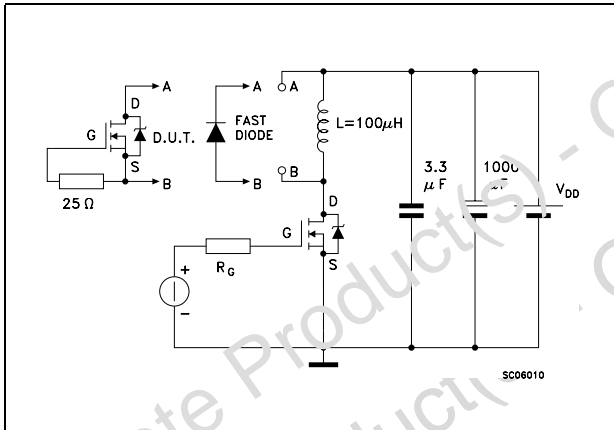
**Figure 14. Switching times test circuit for resistive load**



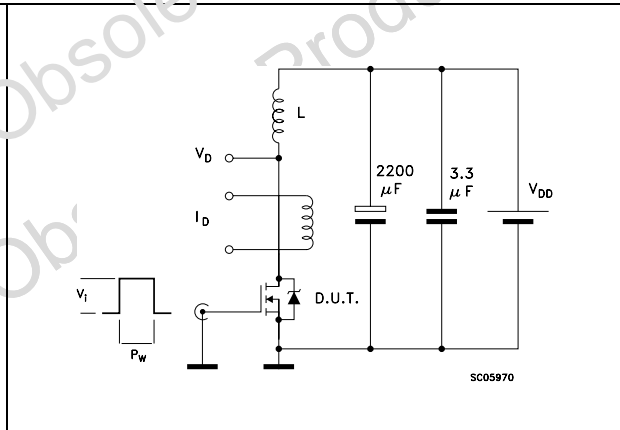
**Figure 15. Gate charge test circuit**



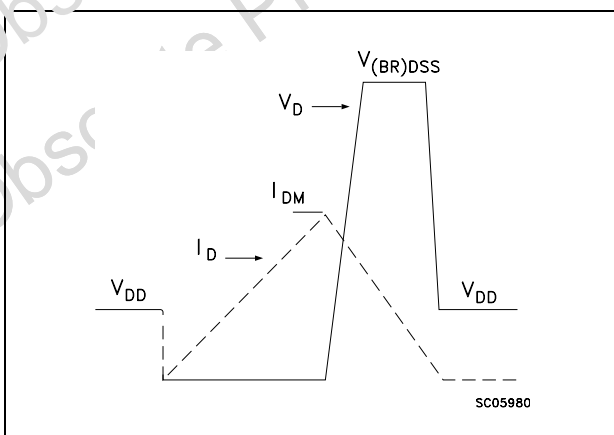
**Figure 16. Test circuit for inductive load switching and diode recovery times**



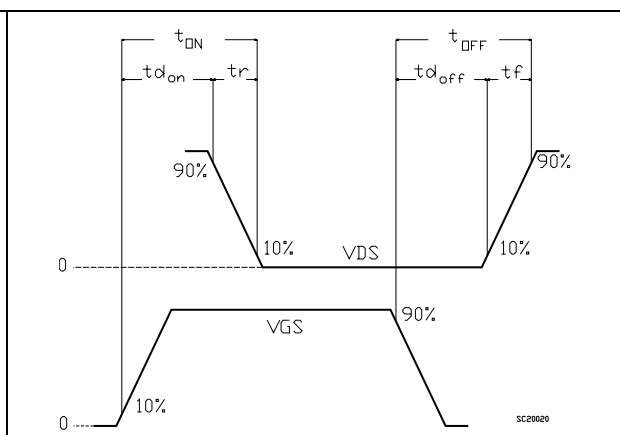
**Figure 17. Unclamped inductive load test circuit**



**Figure 18. Unclamped inductive waveform**



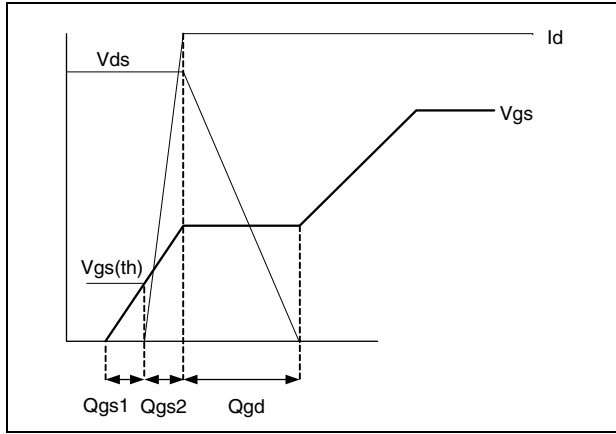
**Figure 19. Switching time waveform**



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**Test circuit**

**Figure 20. Gate charge waveform**



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## 4 Package mechanical data

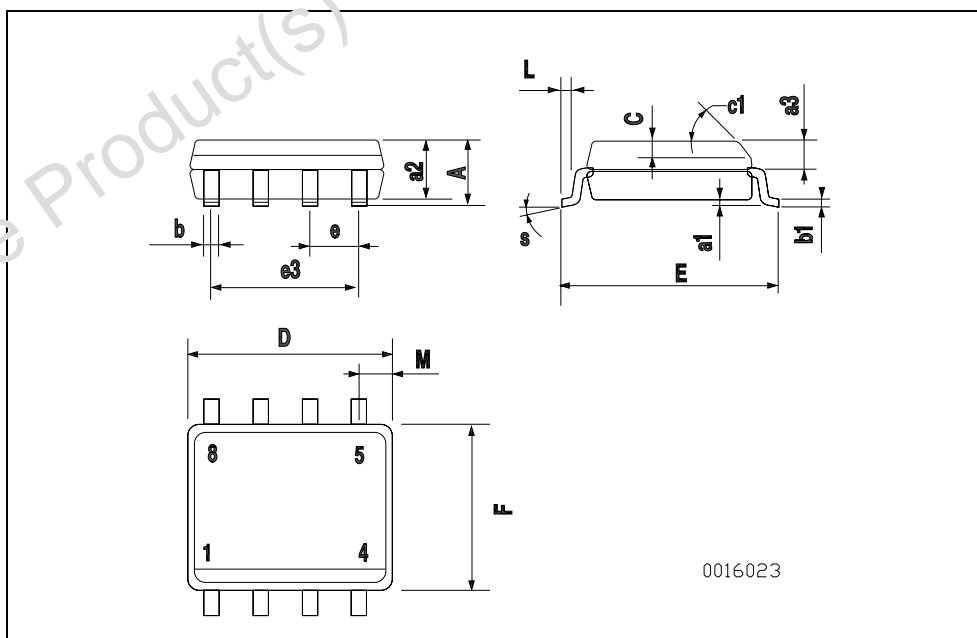
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Package mechanical data

SO-8 MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



## 5 Revision history

**Table 8. Document revision history**

Date	Revision	Changes
22-Jun2004	1	First release
03-Aug-2004	2	Some value change in <a href="#">Table 2</a>
08-Mar-2005	3	Complete version
17-Mar-2005	4	Ron value change (see <a href="#">Table 4</a> )
23-Jun-2005	5	New Rg value on <a href="#">Table 5</a>
30-Mar-2006	6	The document has been reformatted
17-Apr-2007	7	New parameters on <a href="#">Table 5</a> and new <a href="#">Figure 20</a>
23-Apr-2007	8	Modified value on <a href="#">Table 2</a>
26-Nov-2007	9	Modified marking on <a href="#">Table 1</a>

## STS12NH3LL

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