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**SN74AVCH4T245**

SCES577E –JUNE 2004–REVISED NOVEMBER 2015

## SN74AVCH4T245 4-Bit Dual-Supply Bus Transceiver With Configurable Level-Shifting, Voltage Translation, and 3-State Outputs

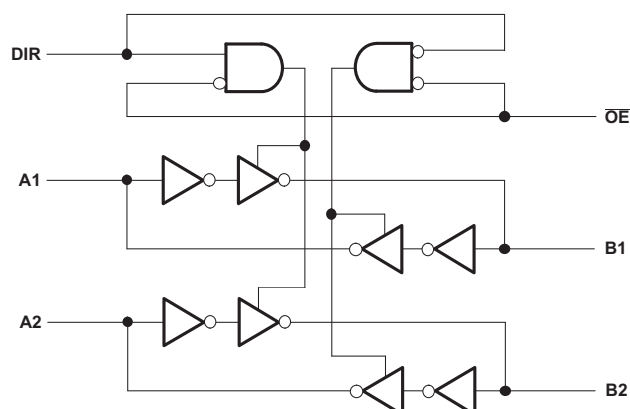
### 1 Features

- Control Inputs  $V_{IH}/V_{IL}$  Levels are Referenced to  $V_{CCA}$  Voltage
- Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.2V to 3.6V Power-Supply Range
- I/Os Are 4.6V Tolerant
- $I_{off}$  Supports Partial Power-Down-Mode Operation
- Bus Hold on Data Inputs Eliminates the Need for External pull-up/pull-down Resistors
- Max Data Rates
  - 380 Mbps (1.8 V to 3.3 V Translation)
  - 200 Mbps (<1.8 V to 3.3 V Translation)
  - 200 Mbps (Translate to 2.5 V or 1.8 V)
  - 150 Mbps (Translate to 1.5 V)
  - 100 Mbps (Translate to 1.2 V)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 8000 V Human Body Model (A114-A)
  - 200 V Machine Model (A115-A)
  - 1000 V Charged-Device Model (C101)

### 2 Applications

- Personal Electronics
- Industrial
- Enterprise
- Telecom

**Logic Diagram (Positive Logic) for 1/2 of AVCH4T245**



### 3 Description

This 4-bit noninverting bus transceiver uses two separate configurable power-supply rails. The A port is designed to track  $V_{CCA}$ .  $V_{CCA}$  accepts any supply voltage from 1.2 V to 3.6 V. The B port is designed to track  $V_{CCB}$ .  $V_{CCB}$  accepts any supply voltage from 1.2 V to 3.6 V. The SN74AVCH4T245 is optimized to operate with  $V_{CCA}/V_{CCB}$  set at 1.4 V to 3.6 V. It is operational with  $V_{CCA}/V_{CCB}$  as low as 1.2 V. This allows for universal low voltage bidirectional translation between any of the 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V voltage nodes.

The SN74AVCH4T245 is designed for asynchronous communication between two data buses. The logic levels of the direction-control (DIR) input and the output-enable (OE) input activate either the B-port outputs or the A-port outputs or place both output ports into the high-impedance mode. The device transmits data from the A bus to the B bus when the B-port outputs are activated, and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports is always active and must have a logic HIGH or LOW level applied to prevent excess  $I_{CC}$  and  $I_{CCZ}$ .

The SN74AVCH4T245 device control pins (1DIR, 2DIR, 1OE, and 2OE) are supplied by  $V_{CCA}$ .

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

**Device Information<sup>(1)</sup>**

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74AVCH4T245	UQFN (16)	1.80 mm × 2.60 mm
	VQFN (16)	3.50 mm × 4.00 mm
	TVSOP (16)	4.40 mm × 3.60 mm
	TSSOP (16)	4.40 mm × 5.00 mm
	SOIC (16)	3.91 mm × 9.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

## SN74AVCH4T245

SCES577E –JUNE 2004–REVISED NOVEMBER 2015

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### Table of Contents

<b>1 Features</b> .....	<b>1</b>	<b>9 Detailed Description</b> .....	<b>17</b>
<b>2 Applications</b> .....	<b>1</b>	9.1 Overview .....	17
<b>3 Description</b> .....	<b>1</b>	9.2 Functional Block Diagram .....	17
<b>4 Revision History</b> .....	<b>2</b>	9.3 Feature Description .....	17
<b>5 Description (continued)</b> .....	<b>3</b>	9.4 Device Functional Modes .....	18
<b>6 Pin Configuration and Functions</b> .....	<b>4</b>	<b>10 Application and Implementation</b> .....	<b>19</b>
<b>7 Specifications</b> .....	<b>5</b>	10.1 Application Information .....	19
7.1 Absolute Maximum Ratings .....	5	10.2 Typical Application .....	19
7.2 ESD Ratings .....	5	<b>11 Power Supply Recommendations</b> .....	<b>21</b>
7.3 Recommended Operating Conditions .....	5	<b>12 Layout</b> .....	<b>21</b>
7.4 Thermal Information .....	6	12.1 Layout Guidelines .....	21
7.5 Electrical Characteristics .....	7	12.2 Layout Example .....	22
7.6 Switching Characteristics, $V_{CCA} = 1.2\text{ V}$ .....	9	<b>13 Device and Documentation Support</b> .....	<b>23</b>
7.7 Switching Characteristics, $V_{CCA} = 1.5\text{ V} \pm 0.1\text{ V}$ .....	10	13.1 Documentation Support .....	23
7.8 Switching Characteristics, $V_{CCA} = 1.8\text{ V} \pm 0.15\text{ V}$ .....	11	13.2 Community Resources .....	23
7.9 Switching Characteristics, $V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}$ .....	12	13.3 Trademarks .....	23
7.10 Switching Characteristics, $V_{CCA} = 3.3\text{ V} \pm 0.3\text{ V}$ .....	13	13.4 Electrostatic Discharge Caution .....	23
7.11 Operating Characteristics .....	14	13.5 Glossary .....	23
7.12 Typical Characteristics .....	15	<b>14 Mechanical, Packaging, and Orderable Information</b> .....	<b>23</b>
<b>8 Parameter Measurement Information</b> .....	<b>16</b>		

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

### Changes from Revision D (June 2007) to Revision E

Page

• Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section .....	1
• Changed Pin Functions table. ....	4

## 5 Description (continued)

The  $V_{CC}$  isolation feature ensures that if either  $V_{CC}$  input is at GND, then both ports are in the high-impedance state. The bus-hold circuitry on the powered-up side always stays active.

Active bus-hold circuitry holds unused or undriven data inputs at a valid logic state. Use of pull-up or pull-down resistors with the bus-hold circuitry is not recommended. The bus-hold circuitry on the powered-up side always stays active.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

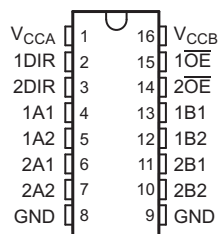
## SN74AVCH4T245

SCES577E –JUNE 2004–REVISED NOVEMBER 2015

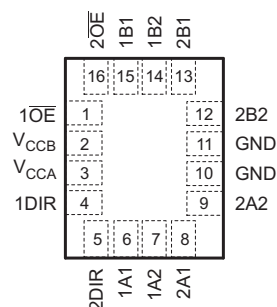
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## 6 Pin Configuration and Functions

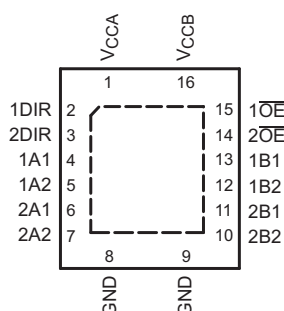
**D, DGV, or PW Packages  
16-Pin SOIC, TVSOP, or TSSOP  
Top View**



**RSV Package  
16-Pin UQFN  
Top View**



**RGY Package  
16-Pin VQFN  
Top View**



### Pin Functions

NAME	PIN		I/O	DESCRIPTION
	SOIC, TVSOP, TSSOP, VQFN	UQFN		
1A1	4	6	I/O	Input/output 1A1. Referenced to $V_{CCA}$ .
1A2	5	7	I/O	Input/output 1A2. Referenced to $V_{CCA}$ .
1B1	13	15	I/O	Input/output 1B1. Referenced to $V_{CCB}$ .
1B2	12	14	I/O	Input/output 1B2. Referenced to $V_{CCB}$ .
1DIR	2	4	I	Direction-control input for 1 ports
1OE	15	1	I	3-state output-mode enables. Pull $\overline{OE}$ high to place '1' outputs in 3-state mode. Referenced to $V_{CCA}$ .
2A1	6	8	I/O	Input/output 2A1. Referenced to $V_{CCA}$ .
2A2	7	9	I/O	Input/output 2A2. Referenced to $V_{CCA}$ .
2B1	11	13	I/O	Input/output 2B1. Referenced to $V_{CCB}$ .
2B2	10	12	I/O	Input/output 2B2. Referenced to $V_{CCB}$ .
2DIR	3	5	I	Direction-control input for 2 ports
2OE	14	16	I	3-state output-mode enables. Pull $\overline{OE}$ high to place 2 outputs in 3-state mode. Referenced to $V_{CCA}$ .
GND	8, 9	10, 11	—	Ground
$V_{CCA}$	1	3	—	A-port power supply voltage. $1.2\text{ V} \leq V_{CCA} \leq 3.6\text{ V}$
$V_{CCB}$	16	2	—	B-port power supply voltage. $1.2\text{ V} \leq V_{CCB} \leq 3.6\text{ V}$

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CCA</sub>	Supply voltage	−0.5	4.6	V
V <sub>CCB</sub>	Supply voltage	−0.5	4.6	V
V <sub>I</sub>	Input voltage <sup>(2)</sup>	I/O ports (A port)	−0.5	4.6
		I/O ports (B port)	−0.5	4.6
		Control inputs	−0.5	4.6
V <sub>O</sub>	Voltage applied to any output in the high-impedance or power-off state <sup>(2)</sup>	A port	−0.5	4.6
		B port	−0.5	4.6
V <sub>O</sub>	Voltage applied to any output in the high or low state <sup>(2)</sup> <sup>(3)</sup>	A port	−0.5	V <sub>CCA</sub> + 0.5
		B port	−0.5	V <sub>CCB</sub> + 0.5
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0	−50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0	−50	mA
I <sub>O</sub>	Continuous output current		±50	mA
	Continuous current through V <sub>CCA</sub> , V <sub>CCB</sub> , or GND		±100	mA
T <sub>stg</sub>	Storage temperature	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input voltage and output negative voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The output positive voltage rating may be exceeded up to 4.6V maximum if the output current rating is observed.

### 7.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±8000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000	
	Machine model	±200	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

see <sup>(1)</sup> <sup>(2)</sup> <sup>(3)</sup> <sup>(4)</sup> <sup>(5)</sup>

			V <sub>CCI</sub>	V <sub>CCO</sub>	MIN	MAX	UNIT
V <sub>CCA</sub>	Supply voltage				1.2	3.6	V
V <sub>CCB</sub>	Supply voltage				1.2	3.6	V
V <sub>IH</sub>	High-level input voltage	Data inputs <sup>(4)</sup>	1.2 V to 1.95 V		V <sub>CCI</sub> × 0.65		V
			1.95 V to 2.7 V		1.6		
			2.7 V to 3.6 V		2		
V <sub>IL</sub>	Low-level input voltage	Data inputs <sup>(4)</sup>	1.2 V to 1.95 V		V <sub>CCI</sub> × 0.35		V
			1.95 V to 2.7 V		0.7		
			2.7 V to 3.6 V		0.8		
V <sub>IH</sub>	High-level input voltage	DIR (referenced to V <sub>CCA</sub> ) <sup>(5)</sup>	1.2 V to 1.95 V		V <sub>CCA</sub> × 0.65		V
			1.95 V to 2.7 V		1.6		
			2.7 V to 3.6 V		2		

(1) V<sub>CCI</sub> is the V<sub>CC</sub> associated with the input port.

(2) V<sub>CCO</sub> is the V<sub>CC</sub> associated with the output port.

(3) All unused data inputs of the device must be held at V<sub>CCI</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

(4) For V<sub>CCI</sub> values not specified in the data sheet, V<sub>IH</sub> min = V<sub>CCI</sub> × 0.7 V, V<sub>IL</sub> max = V<sub>CCI</sub> × 0.3 V.

(5) For V<sub>CCA</sub> values not specified in the data sheet, V<sub>IH</sub> min = V<sub>CCA</sub> × 0.7 V, V<sub>IL</sub> max = V<sub>CCA</sub> × 0.3 V.

## SN74AVCH4T245

SCES577E –JUNE 2004–REVISED NOVEMBER 2015

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### Recommended Operating Conditions (continued)

see (1)(2)(3)(4)(5)

			V <sub>CCI</sub>	V <sub>CCO</sub>	MIN	MAX	UNIT
V <sub>IL</sub>	Low-level input voltage	DIR (referenced to V <sub>CCA</sub> ) <sup>(5)</sup>	1.2 V to 1.95 V		V <sub>CCA</sub> × 0.35		V
			1.95 V to 2.7 V		0.7		
			2.7 V to 3.6 V		0.8		
V <sub>I</sub>	Input voltage				0	3.6	V
V <sub>O</sub>	Output voltage	Active state			0	V <sub>CCO</sub>	V
		3-state			0	3.6	
I <sub>OH</sub>	High-level output current			1.2 V		−3	mA
				1.4 V to 1.6 V		−6	
				1.65 V to 1.95 V		−8	
				2.3 V to 2.7 V		−9	
				3 V to 3.6 V		−12	
I <sub>OL</sub>	Low-level output current			1.2 V		3	mA
				1.4 V to 1.6 V		6	
				1.65 V to 1.95 V		8	
				2.3 V to 2.7 V		9	
				3 V to 3.6 V		12	
Δt/Δv	Input transition rise or fall rate					5	ns/V
T <sub>A</sub>	Operating free-air temperature				−40	85	°C

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN74AVCH4T245					UNIT
		D (SOIC)	DGV (TVSOP)	PW (TSSOP)	RGY (VQFN)	RSV (UQFN)	
		16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance <sup>(2)</sup>	85.5	126.0	112.0	37.5	146.9	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	46.9	50.8	46.8	54.5	53.6	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	43.0	57.7	57.1	15.6	75.6	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	13.4	5.7	5.7	0.5	13.5	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	42.7	57.2	56.5	15.8	75.6	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	—	—	—	3.5	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

(2) The package thermal impedance is calculated in accordance with JESD 51-7.

## 7.5 Electrical Characteristics

All typical limits apply over  $T_A = 25^\circ\text{C}$ , and all maximum and minimum limits apply over  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  (unless otherwise noted).<sup>(1)(2)</sup>

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH}$	$I_{OH} = -100\ \mu\text{A}$ ; $V_{CCA} = 1.2\ \text{V}$ to $3.6\ \text{V}$ ; $V_{CCB} = 1.2\ \text{V}$ to $3.6\ \text{V}$ ; $V_I = V_{IH}$	$V_{CCO} - 0.2$			V
	$I_{OH} = -3\ \text{mA}$ ; $V_{CCA} = 1.2\ \text{V}$ ; $V_{CCB} = 1.2\ \text{V}$ ; $V_I = V_{IH}$		0.95		
	$I_{OH} = -6\ \text{mA}$ ; $V_{CCA} = 1.4\ \text{V}$ ; $V_{CCB} = 1.4\ \text{V}$ ; $V_I = V_{IH}$	1.05			
	$I_{OH} = -8\ \text{mA}$ ; $V_{CCA} = 1.65\ \text{V}$ ; $V_{CCB} = 1.65\ \text{V}$ ; $V_I = V_{IH}$	1.2			
	$I_{OH} = -9\ \text{mA}$ ; $V_{CCA} = 2.3\ \text{V}$ ; $V_{CCB} = 2.3\ \text{V}$ ; $V_I = V_{IH}$	1.75			
	$I_{OH} = -12\ \text{mA}$ ; $V_{CCA} = 3\ \text{V}$ ; $V_{CCB} = 3\ \text{V}$ ; $V_I = V_{IH}$	2.3			
$V_{OL}$	$I_{OL} = 100\ \mu\text{A}$ ; $V_{CCA} = 1.2\ \text{V}$ to $3.6\ \text{V}$ ; $V_{CCB} = 1.2\ \text{V}$ to $3.6\ \text{V}$ ; $V_I = V_{IL}$			0.2	V
	$I_{OL} = 3\ \text{mA}$ ; $V_{CCA} = 1.2\ \text{V}$ ; $V_{CCB} = 1.2\ \text{V}$ ; $V_I = V_{IL}$		0.15		
	$I_{OL} = 6\ \text{mA}$ ; $V_{CCA} = 1.4\ \text{V}$ ; $V_{CCB} = 1.4\ \text{V}$ ; $V_I = V_{IL}$			0.35	
	$I_{OL} = 8\ \text{mA}$ ; $V_{CCA} = 1.65\ \text{V}$ ; $V_{CCB} = 1.65\ \text{V}$ ; $V_I = V_{IL}$			0.45	
	$I_{OL} = 9\ \text{mA}$ ; $V_{CCA} = 2.3\ \text{V}$ ; $V_{CCB} = 2.3\ \text{V}$ ; $V_I = V_{IL}$			0.55	
	$I_{OL} = 12\ \text{mA}$ ; $V_{CCA} = 3\ \text{V}$ ; $V_{CCB} = 3\ \text{V}$ ; $V_I = V_{IL}$			0.7	
$I_I$ DIR input	$V_I = V_{CCA}$ or GND; $V_{CCA} = 1.2\ \text{V}$ to $3.6\ \text{V}$ ; $V_{CCB} = 1.2\ \text{V}$ to $3.6\ \text{V}$	$T_A = 25^\circ\text{C}$	$\pm 0.025$	$\pm 0.25$	$\mu\text{A}$
		$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$		$\pm 1$	
$I_{BHL}^{(3)}$	$V_I = 0.42\ \text{V}$ ; $V_{CCA} = 1.2\ \text{V}$ ; $V_{CCB} = 1.2\ \text{V}$		25		$\mu\text{A}$
	$V_I = 0.49\ \text{V}$ ; $V_{CCA} = 1.4\ \text{V}$ ; $V_{CCB} = 1.4\ \text{V}$	15			
	$V_I = 0.58\ \text{V}$ ; $V_{CCA} = 1.65\ \text{V}$ ; $V_{CCB} = 1.65\ \text{V}$	25			
	$V_I = 0.7\ \text{V}$ ; $V_{CCA} = 2.3\ \text{V}$ ; $V_{CCB} = 2.3\ \text{V}$	45			
	$V_I = 0.8\ \text{V}$ ; $V_{CCA} = 3.3\ \text{V}$ ; $V_{CCB} = 3.3\ \text{V}$	100			
$I_{BHH}^{(4)}$	$V_I = 0.78\ \text{V}$ ; $V_{CCA} = 1.2\ \text{V}$ ; $V_{CCB} = 1.2\ \text{V}$		-25		$\mu\text{A}$
	$V_I = 0.91\ \text{V}$ ; $V_{CCA} = 1.4\ \text{V}$ ; $V_{CCB} = 1.4\ \text{V}$	-15			
	$V_I = 1.07\ \text{V}$ ; $V_{CCA} = 1.65\ \text{V}$ ; $V_{CCB} = 1.65\ \text{V}$	-25			
	$V_I = 1.6\ \text{V}$ ; $V_{CCA} = 2.3\ \text{V}$ ; $V_{CCB} = 2.3\ \text{V}$	-45			
	$V_I = 2\ \text{V}$ ; $V_{CCA} = 3.3\ \text{V}$ ; $V_{CCB} = 3.3\ \text{V}$	-100			
$I_{BHLO}^{(5)}$	$V_I = 0$ to $V_{CCI}$	$V_{CCA} = 1.2\ \text{V}$ ; $V_{CCB} = 1.2\ \text{V}$	50		$\mu\text{A}$
		$V_{CCA} = 1.6\ \text{V}$ ; $V_{CCB} = 1.6\ \text{V}$	125		
		$V_{CCA} = 1.95\ \text{V}$ ; $V_{CCB} = 1.95\ \text{V}$	200		
		$V_{CCA} = 2.7\ \text{V}$ ; $V_{CCB} = 2.7\ \text{V}$	300		
		$V_{CCA} = 3.6\ \text{V}$ ; $V_{CCB} = 3.6\ \text{V}$	500		

(1)  $V_{CCO}$  is the  $V_{CC}$  associated with the output port.

(2)  $V_{CCI}$  is the  $V_{CC}$  associated with the input port.

(3) The bus-hold circuit can sink at least the minimum low sustaining current at  $V_{IL}$  max.  $I_{BHL}$  should be measured after lowering  $V_{IN}$  to GND and then raising it to  $V_{IL}$  max.

(4) The bus-hold circuit can source at least the minimum high sustaining current at  $V_{IH}$  min.  $I_{BHH}$  should be measured after raising  $V_{IN}$  to  $V_{CC}$  and then lowering it to  $V_{IH}$  min.

(5) An external driver must source at least  $I_{BHLO}$  to switch this node from low to high.



# SN74AVCH4T245

SCES577E –JUNE 2004–REVISED NOVEMBER 2015

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## Electrical Characteristics (continued)

All typical limits apply over  $T_A = 25^\circ\text{C}$ , and all maximum and minimum limits apply over  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  (unless otherwise noted).<sup>(1)(2)</sup>

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{\text{BHHO}}$ <sup>(6)</sup>		$V_I = 0$ to $V_{\text{CCI}}$	$V_{\text{CCA}} = 1.2\text{ V};$ $V_{\text{CCB}} = 1.2\text{ V}$	–50		$\mu\text{A}$
			$V_{\text{CCA}} = 1.6\text{ V};$ $V_{\text{CCB}} = 1.6\text{ V}$	–125		
			$V_{\text{CCA}} = 1.95\text{ V};$ $V_{\text{CCB}} = 1.95\text{ V}$	–200		
			$V_{\text{CCA}} = 2.7\text{ V};$ $V_{\text{CCB}} = 2.7\text{ V}$	–300		
			$V_{\text{CCA}} = 3.6\text{ V};$ $V_{\text{CCB}} = 3.6\text{ V}$	–500		
$I_{\text{off}}$	A port	$V_I$ or $V_O = 0$ to $3.6\text{ V}; V_{\text{CCA}} = 0\text{ V}; V_{\text{CCB}} = 0\text{ V}$ to $3.6\text{ V}$	$T_A = 25^\circ\text{C}$	$\pm 0.1$	$\pm 1$	$\mu\text{A}$
			$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$		$\pm 5$	
	B port	$V_I$ or $V_O = 0$ to $3.6\text{ V}; V_{\text{CCA}} = 0\text{ V}$ to $3.6\text{ V}; V_{\text{CCB}} = 0\text{ V}$	$T_A = 25^\circ\text{C}$	$\pm 0.1$	$\pm 1$	
			$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$		$\pm 5$	
$I_{\text{OZ}}$ <sup>(7)</sup>	A or B port	$V_O = V_{\text{CCO}}$ or GND, $V_I = V_{\text{CCI}}$ or GND; $\overline{\text{OE}} = V_{\text{IH}}; V_{\text{CCA}} = 3.6\text{ V}; V_{\text{CCB}} = 3.6\text{ V}$	$T_A = 25^\circ\text{C}$	$\pm 0.5$	$\pm 2.5$	$\mu\text{A}$
			$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$		$\pm 5$	
	B port	$V_O = V_{\text{CCO}}$ or GND, $V_I = V_{\text{CCI}}$ or GND; $\overline{\text{OE}} = \text{don't care}; V_{\text{CCA}} = 0\text{ V}; V_{\text{CCB}} = 3.6\text{ V}$			$\pm 5$	
	A port	$V_O = V_{\text{CCO}}$ or GND, $V_I = V_{\text{CCI}}$ or GND; $\overline{\text{OE}} = \text{don't care}; V_{\text{CCA}} = 3.6\text{ V}; V_{\text{CCB}} = 0\text{ V}$			$\pm 5$	
$I_{\text{CCA}}$		$V_I = V_{\text{CCI}}$ or GND, $I_O = 0$	$V_{\text{CCA}} = 1.2\text{ V}$ to $3.6\text{ V}; V_{\text{CCB}} = 1.2\text{ V}$ to $3.6\text{ V}$		8	$\mu\text{A}$
			$V_{\text{CCA}} = 0\text{ V}; V_{\text{CCB}} = 3.6\text{ V}$		–2	
			$V_{\text{CCA}} = 3.6\text{ V}; V_{\text{CCB}} = 0\text{ V}$		8	
$I_{\text{CCB}}$		$V_I = V_{\text{CCI}}$ or GND, $I_O = 0$	$V_{\text{CCA}} = 1.2\text{ V}$ to $3.6\text{ V}; V_{\text{CCB}} = 1.2\text{ V}$ to $3.6\text{ V}$		8	$\mu\text{A}$
			$V_{\text{CCA}} = 0\text{ V}; V_{\text{CCB}} = 3.6\text{ V}$		8	
			$V_{\text{CCA}} = 3.6\text{ V}; V_{\text{CCB}} = 0\text{ V}$		–2	
$I_{\text{CCA}} + I_{\text{CCB}}$		$V_I = V_{\text{CCI}}$ or GND, $I_O = 0; V_{\text{CCA}} = 1.2\text{ V}$ to $3.6\text{ V}; V_{\text{CCB}} = 1.2\text{ V}$ to $3.6\text{ V}$			16	$\mu\text{A}$
$C_i$	Control inputs	$V_I = 3.3\text{ V}$ or GND; $V_{\text{CCA}} = 3.3\text{ V}; V_{\text{CCB}} = 3.3\text{ V}$		3.5	4.5	pF
$C_{iO}$	A or B port	$V_O = 3.3\text{ V}$ or GND; $V_{\text{CCA}} = 3.3\text{ V}; V_{\text{CCB}} = 3.3\text{ V}$		6	7	pF

(6) An external driver must sink at least  $I_{\text{BHHO}}$  to switch this node from high to low.

(7) For I/O ports, the parameter  $I_{\text{OZ}}$  includes the input leakage current.

## 7.6 Switching Characteristics, $V_{CCA} = 1.2\text{ V}$

over recommended operating free-air temperature range (for parameter descriptions, see [Figure 3](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB}$	TYP	UNIT
$t_{PLH}$ , $t_{PHL}$	A	B	$V_{CCB} = 1.2\text{ V}$	3.4	ns
			$V_{CCB} = 1.5\text{ V} \pm 0.1\text{ V}$	2.9	
			$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$	2.7	
			$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$	2.6	
			$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	2.8	
$t_{PLH}$ , $t_{PHL}$	B	A	$V_{CCB} = 1.2\text{ V}$	3.6	ns
			$V_{CCB} = 1.5\text{ V} \pm 0.1\text{ V}$	3.1	
			$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$	2.8	
			$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$	2.6	
			$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	2.6	
$t_{PZH}$ , $t_{PZL}$	$\overline{OE}$	A	$V_{CCB} = 1.2\text{ V}$	5.6	ns
			$V_{CCB} = 1.5\text{ V} \pm 0.1\text{ V}$	4.7	
			$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$	4.3	
			$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$	3.9	
			$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	3.7	
$t_{PZH}$ , $t_{PZL}$	$\overline{OE}$	B	$V_{CCB} = 1.2\text{ V}$	5	ns
			$V_{CCB} = 1.5\text{ V} \pm 0.1\text{ V}$	4.3	
			$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$	3.9	
			$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$	3.6	
			$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	3.6	
$t_{PHZ}$ , $t_{PLZ}$	$\overline{OE}$	A	$V_{CCB} = 1.2\text{ V}$	6.2	ns
			$V_{CCB} = 1.5\text{ V} \pm 0.1\text{ V}$	5.2	
			$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$	5.2	
			$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$	4.3	
			$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	4.8	
$t_{PHZ}$ , $t_{PLZ}$	$\overline{OE}$	B	$V_{CCB} = 1.2\text{ V}$	5.9	ns
			$V_{CCB} = 1.5\text{ V} \pm 0.1\text{ V}$	5.1	
			$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$	5	
			$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$	4.7	
			$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	5.5	

## SN74AVCH4T245

SCES577E –JUNE 2004–REVISED NOVEMBER 2015

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### 7.7 Switching Characteristics, $V_{CCA} = 1.5\text{ V} \pm 0.1\text{ V}$

over recommended operating free-air temperature range (for parameter descriptions, see [Figure 3](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB}$	MIN	TYP	MAX	UNIT
$t_{PHL}$ , $t_{PLH}$	A	B	$V_{CCB} = 1.2\text{ V}$		3.2		ns
			$V_{CCB} = 1.5\text{ V} \pm 0.1\text{ V}$	0.3		6.3	
			$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$	0.3		5.2	
			$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$	0.4		4.2	
			$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	0.4		4.2	
$t_{PLH}$ , $t_{PHL}$	B	A	$V_{CCB} = 1.2\text{ V}$		3.3		ns
			$V_{CCB} = 1.5\text{ V} \pm 0.1\text{ V}$	0.7		6.3	
			$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$	0.5		6	
			$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$	0.4		5.7	
			$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	0.3		5.6	
$t_{PZH}$ , $t_{PZL}$	$\overline{OE}$	A	$V_{CCB} = 1.2\text{ V}$		4.9		ns
			$V_{CCB} = 1.5\text{ V} \pm 0.1\text{ V}$	1.4		9.6	
			$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$	1.1		9.5	
			$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$	0.7		9.4	
			$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	0.4		9.4	
$t_{PZH}$ , $t_{PZL}$	$\overline{OE}$	B	$V_{CCB} = 1.2\text{ V}$		4.5		ns
			$V_{CCB} = 1.5\text{ V} \pm 0.1\text{ V}$	1.4		9.6	
			$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$	1.1		7.7	
			$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$	0.9		5.8	
			$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	0.9		5.6	
$t_{PHZ}$ , $t_{PLZ}$	$\overline{OE}$	A	$V_{CCB} = 1.2\text{ V}$		5.6		ns
			$V_{CCB} = 1.5\text{ V} \pm 0.1\text{ V}$	1.8		10.2	
			$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$	1.5		10.2	
			$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$	1.3		10.2	
			$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	1.6		10.2	
$t_{PHZ}$ , $t_{PLZ}$	$\overline{OE}$	B	$V_{CCB} = 1.2\text{ V}$		5.2		ns
			$V_{CCB} = 1.5\text{ V} \pm 0.1\text{ V}$	1.9		10.3	
			$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$	1.9		9.1	
			$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$	1.4		7.4	
			$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	1.2		7.6	

## 7.8 Switching Characteristics, $V_{CCA} = 1.8\text{ V} \pm 0.15\text{ V}$

over recommended operating free-air temperature range (for parameter descriptions, see [Figure 3](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB}$	MIN	TYP	MAX	UNIT
$t_{PLH}$ , $t_{PHL}$	A	B	$V_{CCB} = 1.2\text{ V}$		2.9		ns
			$V_{CCB} = 1.5\text{ V} \pm 0.1\text{ V}$	0.1		6	
			$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$	0.1		4.9	
			$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$	0.1		3.9	
			$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	0.3		3.9	
$t_{PLH}$ , $t_{PHL}$	B	A	$V_{CCB} = 1.2\text{ V}$		3		ns
			$V_{CCB} = 1.5\text{ V} \pm 0.1\text{ V}$	0.6		5.3	
			$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$	0.5		4.9	
			$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$	0.3		4.6	
			$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	0.3		4.5	
$t_{PZH}$ , $t_{PZL}$	$\overline{OE}$	A	$V_{CCB} = 1.2\text{ V}$		4.4		ns
			$V_{CCB} = 1.5\text{ V} \pm 0.1\text{ V}$	1		7.4	
			$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$	1		7.3	
			$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$	0.6		7.3	
			$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	0.4		7.2	
$t_{PZH}$ , $t_{PZL}$	$\overline{OE}$	B	$V_{CCB} = 1.2\text{ V}$		4.1		ns
			$V_{CCB} = 1.5\text{ V} \pm 0.1\text{ V}$	1.2		9.2	
			$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$	1		7.4	
			$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$	0.8		5.3	
			$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	0.8		4.6	
$t_{PHZ}$ , $t_{PLZ}$	$\overline{OE}$	A	$V_{CCB} = 1.2\text{ V}$		5.4		ns
			$V_{CCB} = 1.5\text{ V} \pm 0.1\text{ V}$	1.6		8.6	
			$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$	1.8		8.7	
			$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$	1.3		8.7	
			$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	1.6		8.7	
$t_{PHZ}$ , $t_{PLZ}$	$\overline{OE}$	B	$V_{CCB} = 1.2\text{ V}$		5		ns
			$V_{CCB} = 1.5\text{ V} \pm 0.1\text{ V}$	1.7		9.9	
			$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$	1.6		8.7	
			$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$	1.2		6.9	
			$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	1		6.9	

## SN74AVCH4T245

SCES577E –JUNE 2004–REVISED NOVEMBER 2015

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### 7.9 Switching Characteristics, $V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}$

over recommended operating free-air temperature range (for parameter descriptions, see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB}$	MIN	TYP	MAX	UNIT
$t_{PLH}$ , $t_{PHL}$	A	B	$V_{CCB} = 1.2\text{ V}$		2.8		ns
			$V_{CCB} = 1.5\text{ V} \pm 0.1\text{ V}$	0.1		5.7	
			$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$	0.1		4.6	
			$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$	0.2		3.5	
			$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	0.1		3.6	
$t_{PLH}$ , $t_{PHL}$	B	A	$V_{CCB} = 1.2\text{ V}$		2.7		ns
			$V_{CCB} = 1.5\text{ V} \pm 0.1\text{ V}$	0.6		4.2	
			$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$	0.4		3.9	
			$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$	0.2		3.4	
			$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	0.2		3.3	
$t_{PZH}$ , $t_{PZL}$	$\overline{OE}$	A	$V_{CCB} = 1.2\text{ V}$		4		ns
			$V_{CCB} = 1.5\text{ V} \pm 0.1\text{ V}$	0.7		6.5	
			$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$	0.7		5.2	
			$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$	0.6		4.8	
			$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	0.4		4.8	
$t_{PZH}$ , $t_{PZL}$	$\overline{OE}$	B	$V_{CCB} = 1.2\text{ V}$		3.8		ns
			$V_{CCB} = 1.5\text{ V} \pm 0.1\text{ V}$	0.9		8.8	
			$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$	0.8		7	
			$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$	0.6		4.8	
			$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	0.6		4	
$t_{PHZ}$ , $t_{PLZ}$	$\overline{OE}$	A	$V_{CCB} = 1.2\text{ V}$		4.7		ns
			$V_{CCB} = 1.5\text{ V} \pm 0.1\text{ V}$	1		8.4	
			$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$	1		8.4	
			$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$	1		6.2	
			$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	1		6.6	
$t_{PHZ}$	$\overline{OE}$	B	$V_{CCB} = 1.2\text{ V}$		4.5		ns
			$V_{CCB} = 1.5\text{ V} \pm 0.1\text{ V}$	1.5		9.4	
			$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$	1.3		8.2	
			$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$	1.1		6.2	
			$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	0.9		5.2	
$t_{PLZ}$	$\overline{OE}$	B	$V_{CCB} = 1.2\text{ V}$		4.5		ns
			$V_{CCB} = 1.5\text{ V} \pm 0.1\text{ V}$	1.5		8.8	
			$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$	1.3		8.2	
			$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$	1.1		6.2	
			$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	0.9		5.2	

## 7.10 Switching Characteristics, $V_{CCA} = 3.3\text{ V} \pm 0.3\text{ V}$

over recommended operating free-air temperature range (for parameter descriptions, see [Figure 3](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB}$	MIN	TYP	MAX	UNIT
$t_{PLH}$ , $t_{PHL}$	A	B	$V_{CCB} = 1.2\text{ V}$		2.9		ns
			$V_{CCB} = 1.5\text{ V} \pm 0.1\text{ V}$	0.1		5.6	
			$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$	0.1		4.5	
			$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$	0.1		3.3	
			$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	0.1		2.9	
$t_{PLH}$ , $t_{PHL}$	B	A	$V_{CCB} = 1.2\text{ V}$		2.6		ns
			$V_{CCB} = 1.5\text{ V} \pm 0.1\text{ V}$	0.6		4.2	
			$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$	0.4		3.4	
			$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$	0.2		3	
			$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	0.1		2.8	
$t_{PZH}$ , $t_{PZL}$	$\overline{OE}$	A	$V_{CCB} = 1.2\text{ V}$		3.8		ns
			$V_{CCB} = 1.5\text{ V} \pm 0.1\text{ V}$	0.6		8.7	
			$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$	0.6		5.2	
			$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$	0.6		3.8	
			$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	0.4		3.8	
$t_{PZH}$ , $t_{PZL}$	$\overline{OE}$	B	$V_{CCB} = 1.2\text{ V}$		3.7		ns
			$V_{CCB} = 1.5\text{ V} \pm 0.1\text{ V}$	0.8		8.7	
			$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$	0.6		6.8	
			$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$	0.5		4.7	
			$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	0.5		3.8	
$t_{PHZ}$ , $t_{PLZ}$	$\overline{OE}$	A	$V_{CCB} = 1.2\text{ V}$		4.8		ns
			$V_{CCB} = 1.5\text{ V} \pm 0.1\text{ V}$	0.7		9.3	
			$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$	0.7		8.3	
			$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$	0.7		5.6	
			$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	0.7		6.6	
$t_{PHZ}$ , $t_{PLZ}$	$\overline{OE}$	B	$V_{CCB} = 1.2\text{ V}$		5.3		ns
			$V_{CCB} = 1.5\text{ V} \pm 0.1\text{ V}$	1.4		9.3	
			$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$	1.2		8.1	
			$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$	1		6.4	
			$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	0.8		6.2	

## SN74AVCH4T245

SCES577E –JUNE 2004–REVISED NOVEMBER 2015

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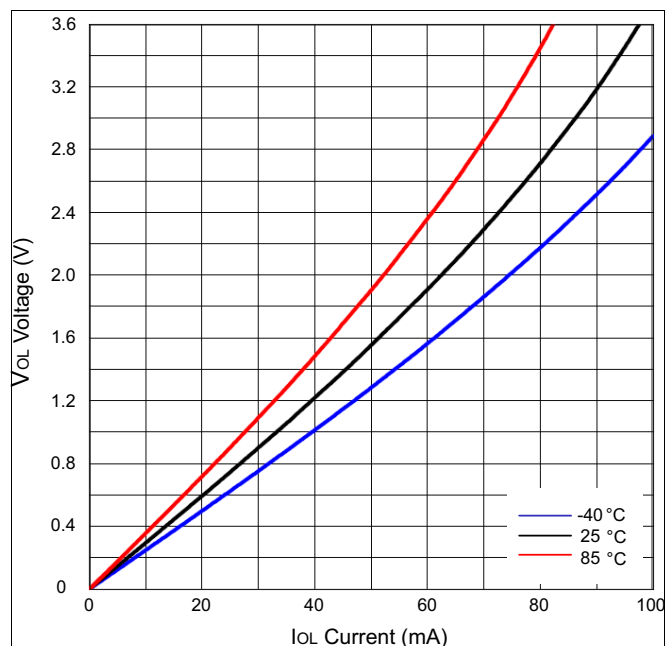
### 7.11 Operating Characteristics

T<sub>A</sub> = 25°C

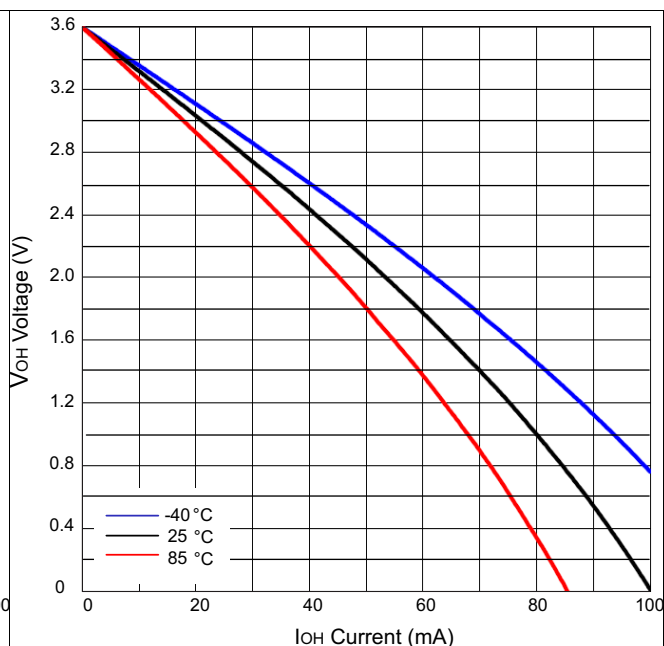
PARAMETER			TEST CONDITIONS	V <sub>CCA</sub>	TYP	UNIT
C <sub>pdA</sub> <sup>(1)</sup>	A to B	Outputs enabled	C <sub>L</sub> = 0, f = 10 MHz, t <sub>r</sub> = t <sub>f</sub> = 1 ns	V <sub>CCA</sub> = V <sub>CCB</sub> = 1.2 V	1	pF
				V <sub>CCA</sub> = V <sub>CCB</sub> = 1.5 V	1	
				V <sub>CCA</sub> = V <sub>CCB</sub> = 1.8 V	1	
				V <sub>CCA</sub> = V <sub>CCB</sub> = 2.5 V	1.5	
				V <sub>CCA</sub> = V <sub>CCB</sub> = 3.3 V	2	
	Outputs disabled		C <sub>L</sub> = 0, f = 10 MHz, t <sub>r</sub> = t <sub>f</sub> = 1 ns	V <sub>CCA</sub> = V <sub>CCB</sub> = 1.2 V	1	pF
				V <sub>CCA</sub> = V <sub>CCB</sub> = 1.5 V	1	
				V <sub>CCA</sub> = V <sub>CCB</sub> = 1.8 V	1	
				V <sub>CCA</sub> = V <sub>CCB</sub> = 2.5 V	1	
				V <sub>CCA</sub> = V <sub>CCB</sub> = 3.3 V	1	
	B to A	Outputs enabled	C <sub>L</sub> = 0, f = 10 MHz, t <sub>r</sub> = t <sub>f</sub> = 1 ns	V <sub>CCA</sub> = V <sub>CCB</sub> = 1.2 V	12	pF
				V <sub>CCA</sub> = V <sub>CCB</sub> = 1.5 V	12.5	
				V <sub>CCA</sub> = V <sub>CCB</sub> = 1.8 V	13	
				V <sub>CCA</sub> = V <sub>CCB</sub> = 2.5 V	14	
				V <sub>CCA</sub> = V <sub>CCB</sub> = 3.3 V	15	
		Outputs disabled	C <sub>L</sub> = 0, f = 10 MHz, t <sub>r</sub> = t <sub>f</sub> = 1 ns	V <sub>CCA</sub> = V <sub>CCB</sub> = 1.2 V	1	pF
				V <sub>CCA</sub> = V <sub>CCB</sub> = 1.5 V	1	
				V <sub>CCA</sub> = V <sub>CCB</sub> = 1.8 V	1	
				V <sub>CCA</sub> = V <sub>CCB</sub> = 2.5 V	1	
				V <sub>CCA</sub> = V <sub>CCB</sub> = 3.3 V	1	
C <sub>pdB</sub> <sup>(1)</sup>	A to B	Outputs enabled	C <sub>L</sub> = 0, f = 10 MHz, t <sub>r</sub> = t <sub>f</sub> = 1 ns	V <sub>CCA</sub> = V <sub>CCB</sub> = 1.2 V	12	pF
				V <sub>CCA</sub> = V <sub>CCB</sub> = 1.5 V	12.5	
				V <sub>CCA</sub> = V <sub>CCB</sub> = 1.8 V	13	
				V <sub>CCA</sub> = V <sub>CCB</sub> = 2.5 V	14	
				V <sub>CCA</sub> = V <sub>CCB</sub> = 3.3 V	15	
		Outputs disabled	C <sub>L</sub> = 0, f = 10 MHz, t <sub>r</sub> = t <sub>f</sub> = 1 ns	V <sub>CCA</sub> = V <sub>CCB</sub> = 1.2 V	1	pF
				V <sub>CCA</sub> = V <sub>CCB</sub> = 1.5 V	1	
				V <sub>CCA</sub> = V <sub>CCB</sub> = 1.8 V	1	
				V <sub>CCA</sub> = V <sub>CCB</sub> = 2.5 V	1	
				V <sub>CCA</sub> = V <sub>CCB</sub> = 3.3 V	1	
	B to A	Outputs enabled	C <sub>L</sub> = 0, f = 10 MHz, t <sub>r</sub> = t <sub>f</sub> = 1 ns	V <sub>CCA</sub> = V <sub>CCB</sub> = 1.2 V	1	pF
				V <sub>CCA</sub> = V <sub>CCB</sub> = 1.5 V	1	
				V <sub>CCA</sub> = V <sub>CCB</sub> = 1.8 V	1	
				V <sub>CCA</sub> = V <sub>CCB</sub> = 2.5 V	1	
				V <sub>CCA</sub> = V <sub>CCB</sub> = 3.3 V	2	
		Outputs disabled	C <sub>L</sub> = 0, f = 10 MHz, t <sub>r</sub> = t <sub>f</sub> = 1 ns	V <sub>CCA</sub> = V <sub>CCB</sub> = 1.2 V	1	pF
				V <sub>CCA</sub> = V <sub>CCB</sub> = 1.5 V	1	
				V <sub>CCA</sub> = V <sub>CCB</sub> = 1.8 V	1	
				V <sub>CCA</sub> = V <sub>CCB</sub> = 2.5 V	1	
				V <sub>CCA</sub> = V <sub>CCB</sub> = 3.3 V	1	

(1) Power dissipation capacitance per transceiver. Refer to TI application report, CMOS Power Consumption and Cpd Calculation (SCAA035)

## 7.12 Typical Characteristics



**Figure 1. Low-Level Output Voltage ( $V_{OL}$ ) vs Low-Level Current ( $I_{OL}$ )**



**Figure 2. High-Level Output Voltage ( $V_{OH}$ ) vs High-Level Current ( $I_{OH}$ )**

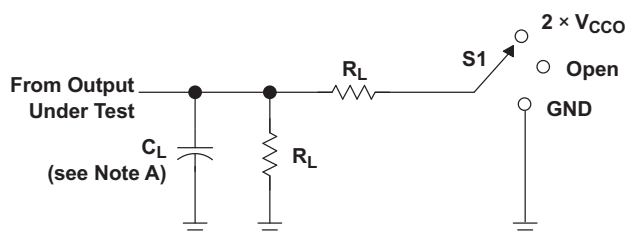


## SN74AVCH4T245

SCES577E –JUNE 2004–REVISED NOVEMBER 2015

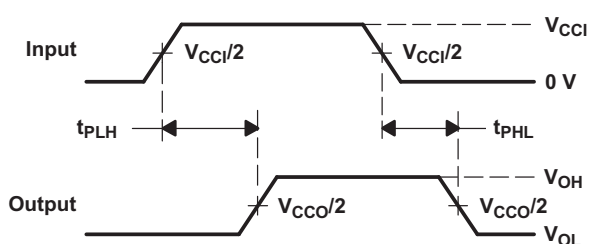
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## 8 Parameter Measurement Information



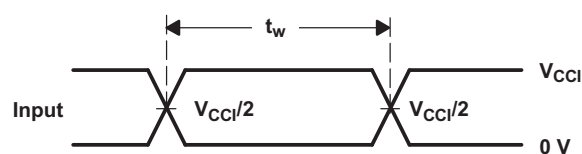
LOAD CIRCUIT

$V_{CCO}$	$C_L$	$R_L$	$V_{TP}$
1.2 V	15 pF	2 k $\Omega$	0.1 V
1.5 V $\pm$ 0.1 V	15 pF	2 k $\Omega$	0.1 V
1.8 V $\pm$ 0.15 V	15 pF	2 k $\Omega$	0.15 V
2.5 V $\pm$ 0.2 V	15 pF	2 k $\Omega$	0.15 V
3.3 V $\pm$ 0.3 V	15 pF	2 k $\Omega$	0.3 V

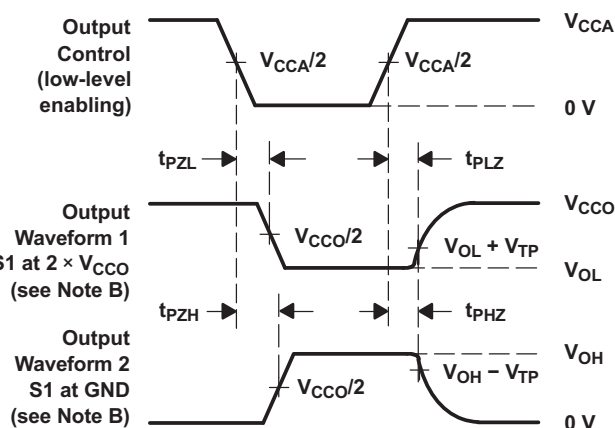


VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES

TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CCO}$
$t_{PHZ}/t_{PZH}$	GND



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics: PRR = 10 MHz,  $Z_O = 50 \Omega$ ,  $dv/dt \geq 1$  V/ns,  $dv/dt \geq 1$  V/ns.
  - The outputs are measured one at a time, with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - $V_{CCI}$  is the  $V_{CC}$  associated with the input port.
  - $V_{CCO}$  is the  $V_{CC}$  associated with the output port.

Figure 3. Load Circuit and Voltage Waveforms

## 9 Detailed Description

### 9.1 Overview

The SN74AVCH4T245 is a 4-bit, dual-supply noninverting bidirectional voltage level translation device. Ax pins and control pins (1DIR, 2DIR, 1OE, and 2OE) are supported by  $V_{CCA}$ , and Bx pins are supported by  $V_{CCB}$ . The A port is able to accept I/O voltages ranging from 1.2 V to 3.6 V, while the B port can accept I/O voltages from 1.2 V to 3.6 V. A high on DIR allows data transmission from Ax to Bx and a low on DIR allows data transmission from Bx to Ax when  $\overline{OE}$  is set to low. When  $\overline{OE}$  is set to high, both Ax and Bx pins are in the high-impedance state. Refer to the *AVC Logic Family Technology and Applications* Application Report (SCEA006).

### 9.2 Functional Block Diagram

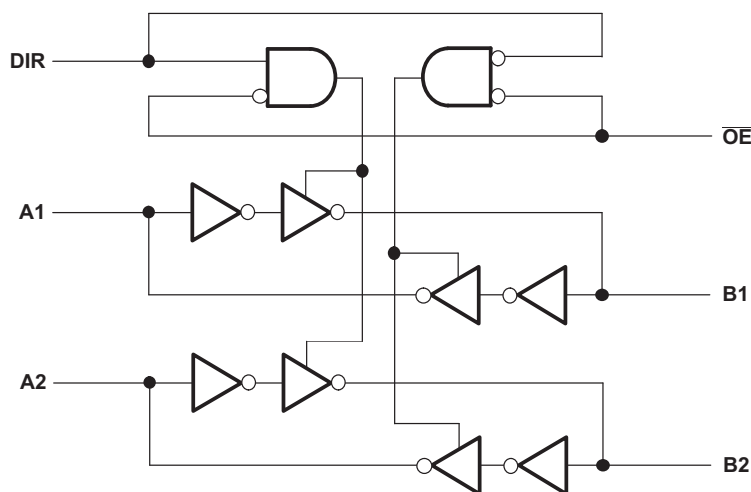


Figure 4. Logic Diagram (Positive Logic) for 1/2 of SN74AVCH4T245

### 9.3 Feature Description

#### 9.3.1 Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.2V to 3.6V Power-Supply Range

Both  $V_{CCA}$  and  $V_{CCB}$  can be supplied at any voltage between 1.2 V and 3.6 V; thus, making the device suitable for translating between any of the low voltage nodes (1.2 V, 1.8 V, 2.5 V, and 3.3 V).

#### 9.3.2 Supports High Speed Translation

The SN74AVCH4T245 device can support high data rate applications. The translated signal data rate can be up to 380 Mbps when the signal is translated from 1.8 V to 3.3 V.

#### 9.3.3 $I_{off}$ Supports Partial-Power-Down Mode Operation

$I_{off}$  will prevent backflow current by disabling I/O output circuits when device is in partial-power-down mode.

#### 9.3.4 Bus-Hold Circuitry

This device has active bus-hold circuitry that holds unused or undriven inputs at a valid logic state. Use of pull-up or pull-down resistors with the bus-hold circuitry is not recommended. (Refer to the *Bus-Hold Circuit* Application Report (SCLA015). Pullup and pulldown resistors are not recommended on the inputs of devices with bus-hold. Unused inputs can be left floating.

## SN74AVCH4T245

SCES577E –JUNE 2004–REVISED NOVEMBER 2015

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### Feature Description (continued)

#### 9.3.5 Vcc Isolation Feature

The VCC isolation feature ensures that if either  $V_{CCA}$  or  $V_{CCB}$  are at GND (or  $< 0.4V$ ), both ports will be in a high-impedance state (IOZ shown in [Electrical Characteristics](#)). This prevents false logic levels from being presented to either bus.

#### 9.4 Device Functional Modes

[Table 1](#) lists the functional modes of the SN74AVCH4T245.

**Table 1. Function Table (Each 2-Bit Section)**

CONTROL INPUTS <sup>(1)</sup>		OUTPUT CIRCUITS		OPERATION
$\overline{OE}$	DIR	A PORT	B PORT	
L	L	Enabled	Hi-Z	B data to A bus
L	H	Hi-Z	Enabled	A data to B bus
H	X	Hi-Z	Hi-Z	Isolation

(1) Input circuits of the data I/Os are always active.

## 10 Application and Implementation

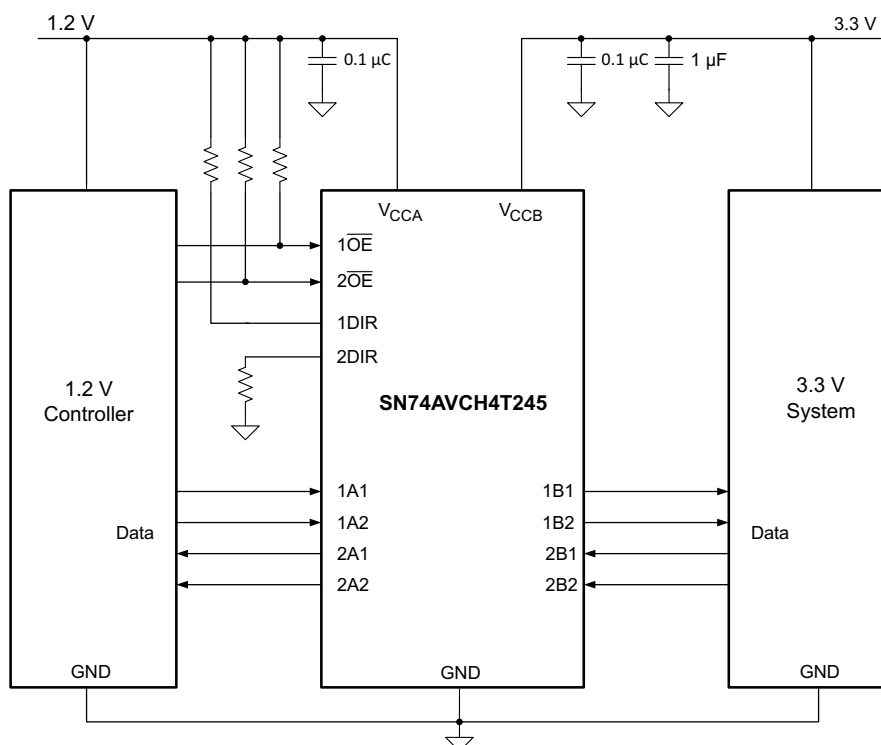
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 10.1 Application Information

The SN74AVCH4T245 device can be used in level-shifting applications for interfacing devices or systems operating at different interface voltages with one another. The SN74AVCH4T245 device is ideal for use in applications where a push-pull driver is connected to the data I/Os. The max data rate can be up to 380 Mbps when device translates a signal from 1.8 V to 3.3 V.

### 10.2 Typical Application



**Figure 5. Typical Application Diagram**

## SN74AVCH4T245

SCES577E –JUNE 2004–REVISED NOVEMBER 2015

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### Typical Application (continued)

#### 10.2.1 Design Requirements

For the design example shown in [Typical Application](#), use the parameters listed in [Table 2](#).

**Table 2. Design Parameters**

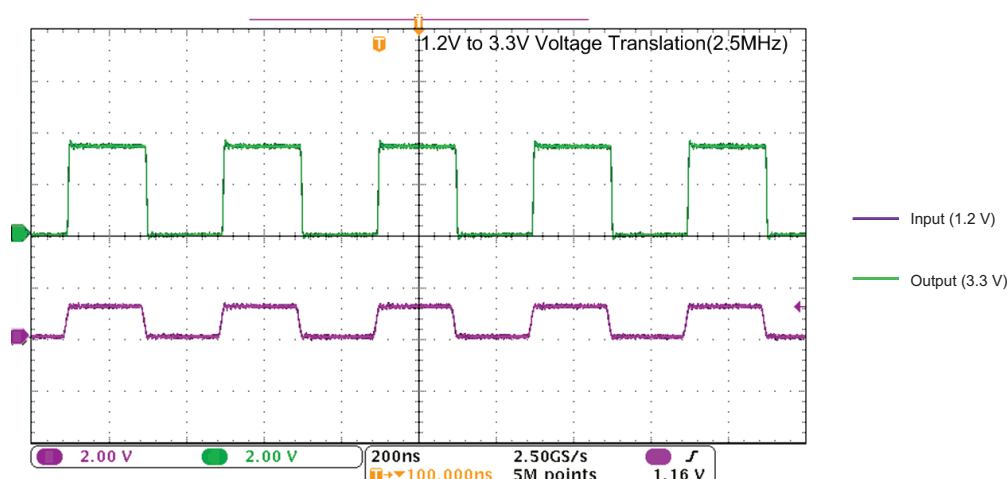
DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	1.2 V to 3.6 V
Output voltage range	1.2 V to 3.6 V

#### 10.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the SN74AVCH4T245 device to determine the input voltage range. For a valid logic high, the value must exceed the  $V_{IH}$  of the input port. For a valid logic low, the value must be less than the  $V_{IL}$  of the input port.
- Output voltage range
  - Use the supply voltage of the device that the SN74AVCH4T245 device is driving to determine the output voltage range.

#### 10.2.3 Application Curve



**Figure 6. Translation Up (1.2 V to 3.3 V) at 2.5 MHz**

## 11 Power Supply Recommendations

The SN74AVCH4T245 device uses two separate configurable power-supply rails,  $V_{CCA}$  and  $V_{CCB}$ .  $V_{CCA}$  accepts any supply voltage from 1.2 V to 3.6 V and  $V_{CCB}$  accepts any supply voltage from 1.2 V to 3.6 V. The A port and B port are designed to track  $V_{CCA}$  and  $V_{CCB}$  respectively allowing for low voltage bidirectional translation between any of the 1.2-V, 1.5-V, 1.8-V, 2.5-V, and 3.3-V voltage nodes.

The output-enable ( $\overline{OE}$ ) input circuit is designed so that it is supplied by  $V_{CCA}$  and when the  $\overline{OE}$  input is high, all outputs are placed in the high-impedance state. To ensure the high-impedance state of the outputs during power up or power down, the  $\overline{OE}$  input pin must be tied to  $V_{CCA}$  through a pull-up resistor and must not be enabled until  $V_{CCA}$  and  $V_{CCB}$  are fully ramped and stable. The minimum value of the pull-up resistor to  $V_{CCA}$  is determined by the current-sinking capability of the driver.

$V_{CCA}$  or  $V_{CCB}$  can be powered up first. If the SN74AVCH4T245 is powered up in a permanently enabled state, pull-up resistors are recommended at the input. This ensures proper/glitch-free power-up. (Refer to *Designing with SN74LVCXT245 and SN74LVCHXT245 Family of Direction Controlled Voltage Translators/Level-Shifters* Application Note ([SLVA746](#)).)

## 12 Layout

### 12.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines is recommended.

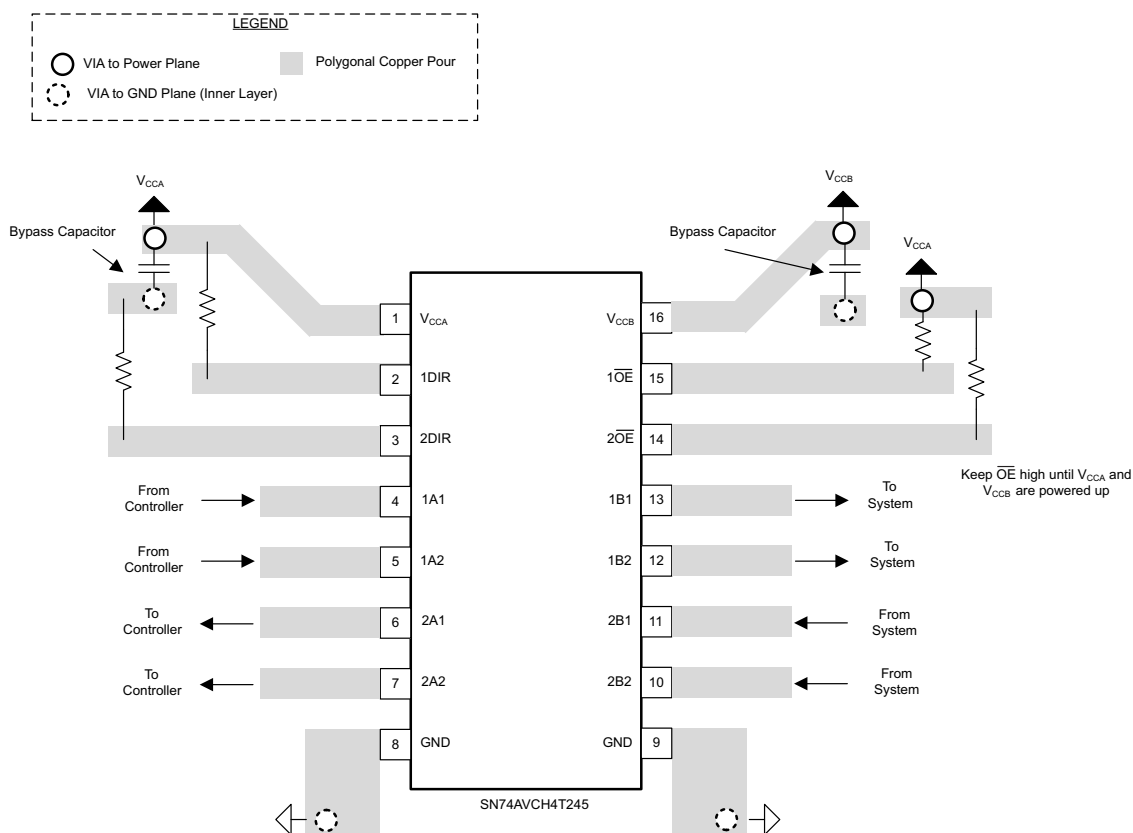
- Bypass capacitors should be used on power supplies.
- Short trace lengths should be used to avoid excessive loading.
- Place pads on the signal paths for loading capacitors or pull-up resistors to help adjust rise and fall times of signals, depending on the system requirements.

## SN74AVCH4T245

SCES577E –JUNE 2004–REVISED NOVEMBER 2015

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### 12.2 Layout Example



**Figure 7. Layout Recommendation**

## 13 Device and Documentation Support

### 13.1 Documentation Support

#### 13.1.1 Related Documentation

For related documentation, see the following:

- *Designing with SN74LVCXT245 and SN74LVCHXT245 Family of Direction Controlled Voltage Translators/Level-Shifters*, [SLVA746](#)
- *Bus-Hold Circuit*, [SCLA015](#)
- *AVC Logic Family Technology and Applications*, [SCEA006](#)

### 13.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 13.3 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

### 13.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 13.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74AVCH4T245PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	WS245	<a href="#">Samples</a>
74AVCH4T245PWTE4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	WS245	<a href="#">Samples</a>
74AVCH4T245PWTE4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	WS245	<a href="#">Samples</a>
74AVCH4T245RGYRG4	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	WS245	<a href="#">Samples</a>
74AVCH4T245RSVRG4	ACTIVE	UQFN	RSV	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZWV	<a href="#">Samples</a>
SN74AVCH4T245D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVCH4T245	<a href="#">Samples</a>
SN74AVCH4T245DGVR	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	WS245	<a href="#">Samples</a>
SN74AVCH4T245DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVCH4T245	<a href="#">Samples</a>
SN74AVCH4T245DT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVCH4T245	<a href="#">Samples</a>
SN74AVCH4T245PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	WS245	<a href="#">Samples</a>
SN74AVCH4T245PWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	WS245	<a href="#">Samples</a>
SN74AVCH4T245PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	WS245	<a href="#">Samples</a>
SN74AVCH4T245PWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	WS245	<a href="#">Samples</a>
SN74AVCH4T245RGYR	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	WS245	<a href="#">Samples</a>
SN74AVCH4T245RSVR	ACTIVE	UQFN	RSV	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZWV	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.



**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74AVCH4T245 :**

- Enhanced Product: [SN74AVCH4T245-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## PACKAGE MATERIALS INFORMATION

### TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AVCH4T245DGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74AVCH4T245DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74AVCH4T245PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AVCH4T245PWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AVCH4T245RSVR	UQFN	RSV	16	3000	180.0	12.4	2.1	2.9	0.75	4.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



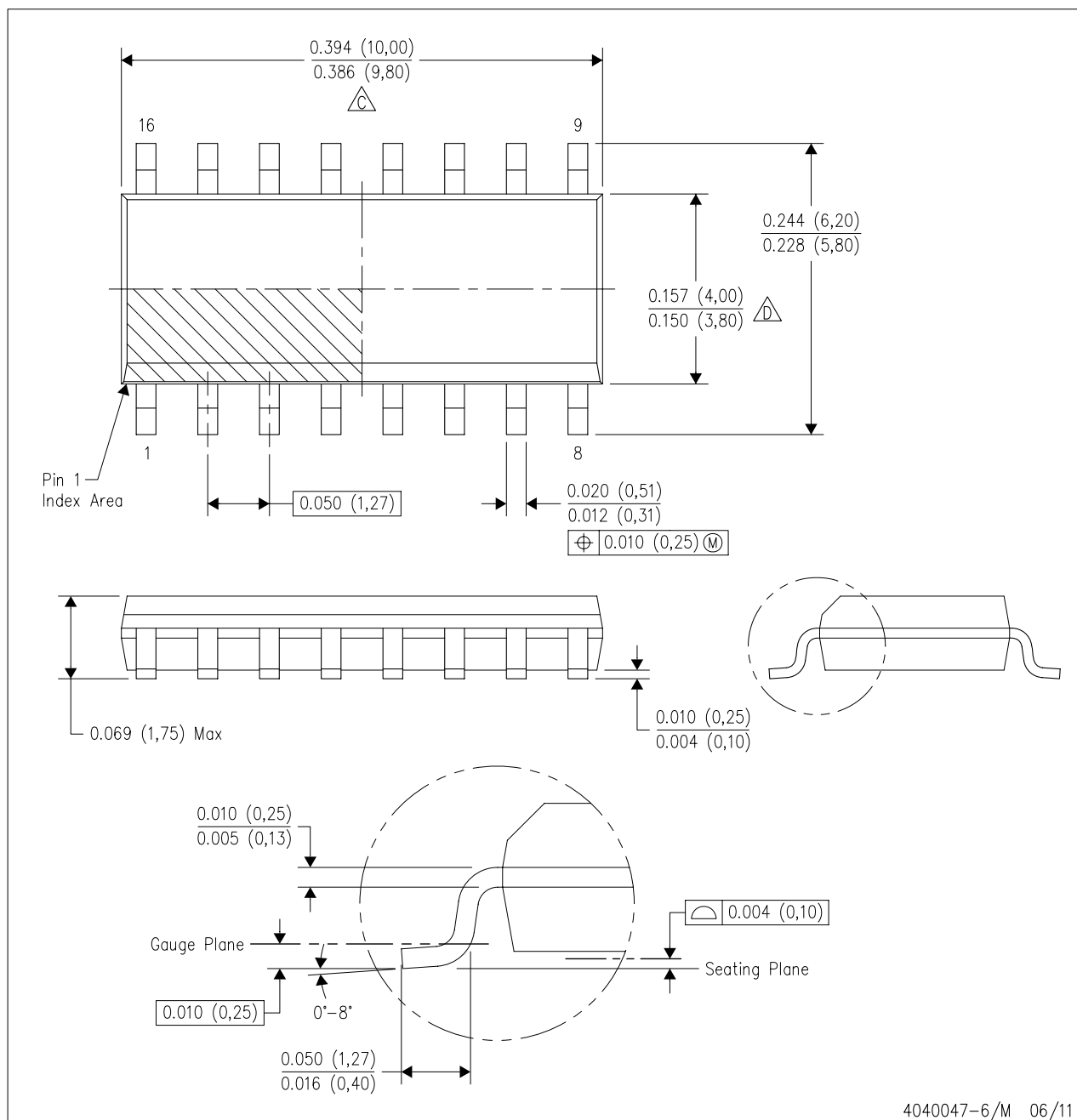
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AVCH4T245DGVR	TVSOP	DGV	16	2000	367.0	367.0	35.0
SN74AVCH4T245DR	SOIC	D	16	2500	333.2	345.9	28.6
SN74AVCH4T245PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74AVCH4T245PWT	TSSOP	PW	16	250	367.0	367.0	35.0
SN74AVCH4T245RSVR	UQFN	RSV	16	3000	203.0	203.0	35.0

## MECHANICAL DATA

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



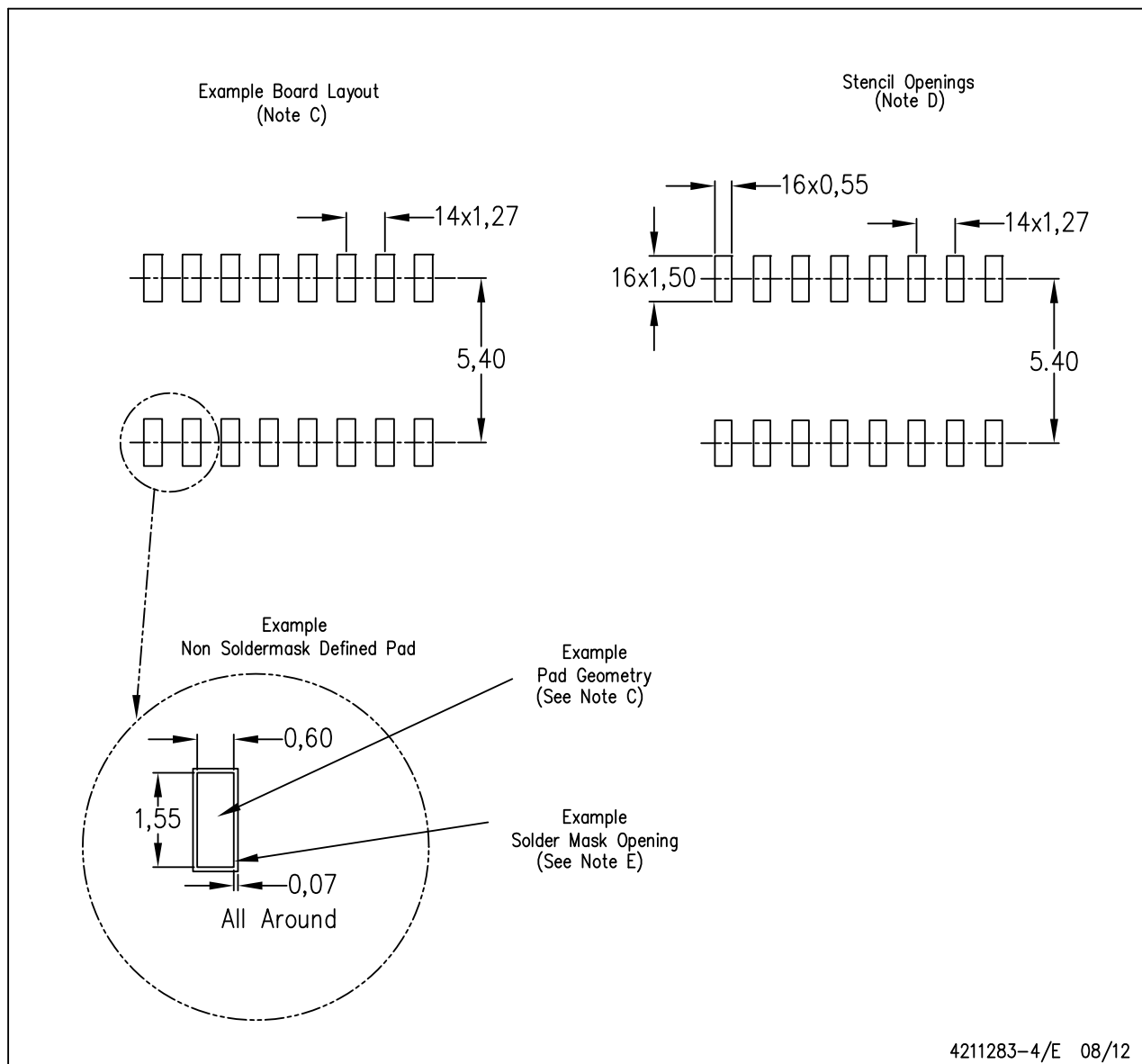
**NOTES:**

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.

## LAND PATTERN DATA

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

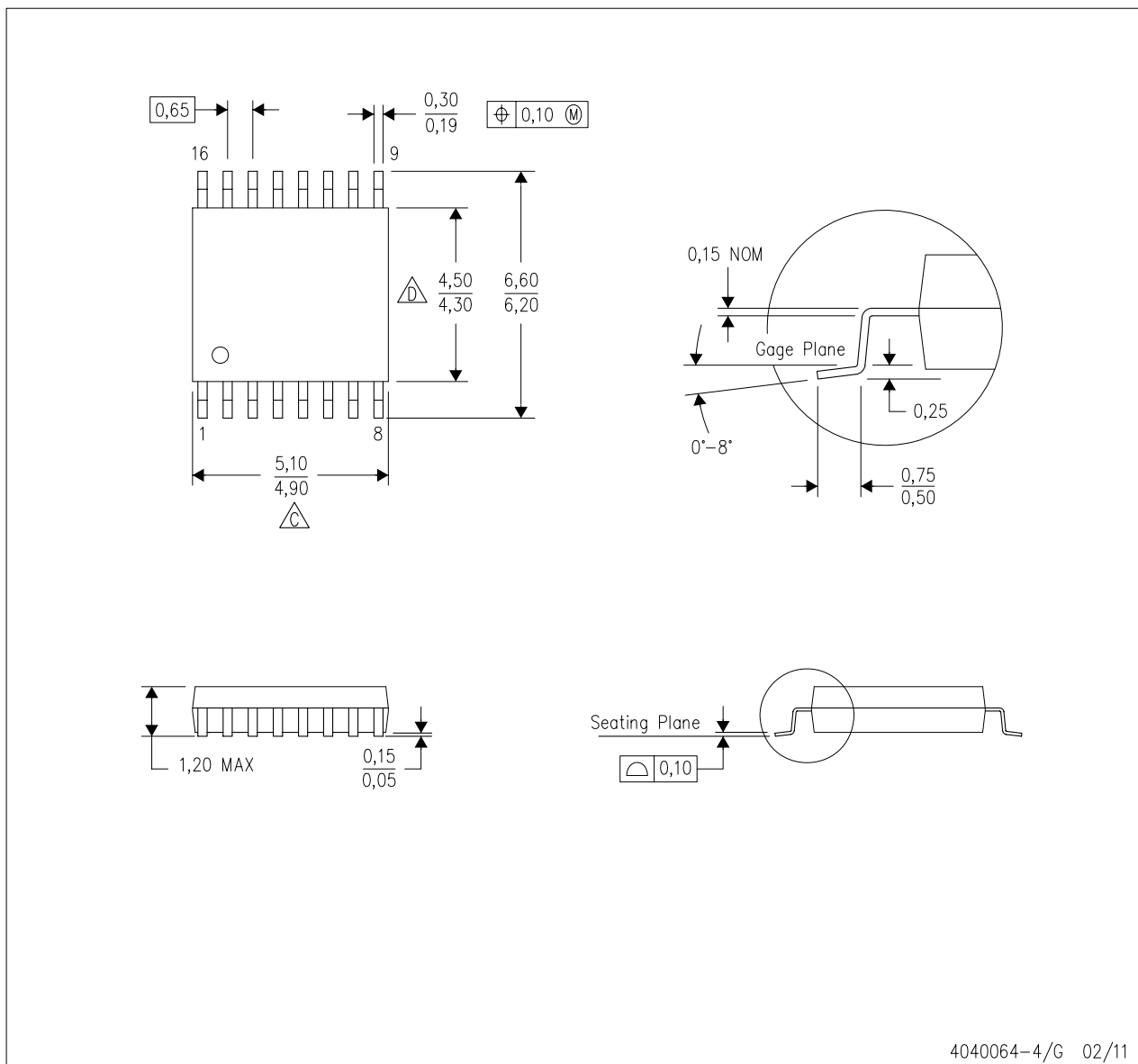


- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## MECHANICAL DATA

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE

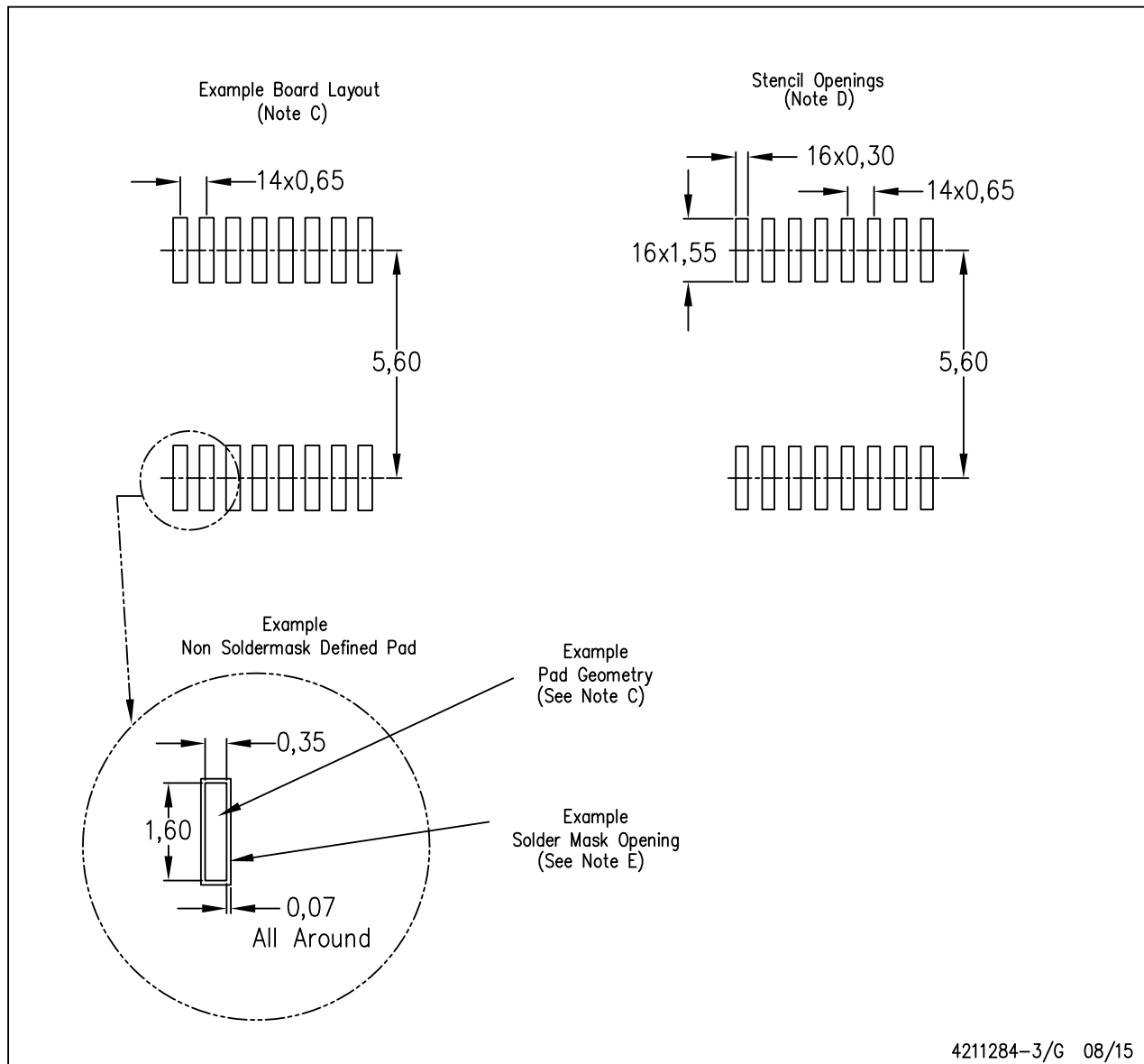


- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

## LAND PATTERN DATA

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



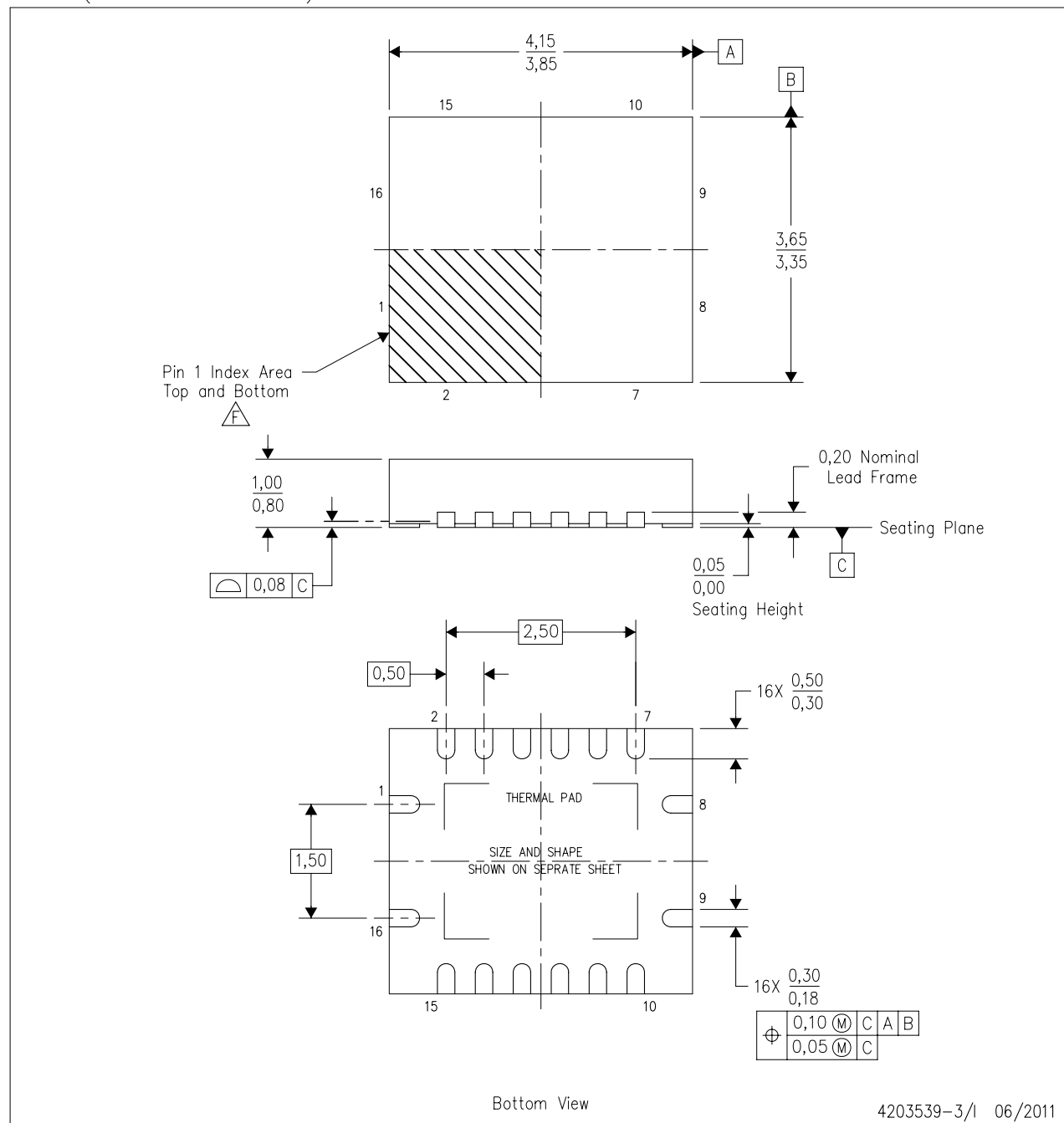
- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



## MECHANICAL DATA

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4203539-3/1 06/2011

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) package configuration.
  - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - G. Package complies to JEDEC MO-241 variation BA.

## THERMAL PAD MECHANICAL DATA

RGY (R-PVQFN-N16)

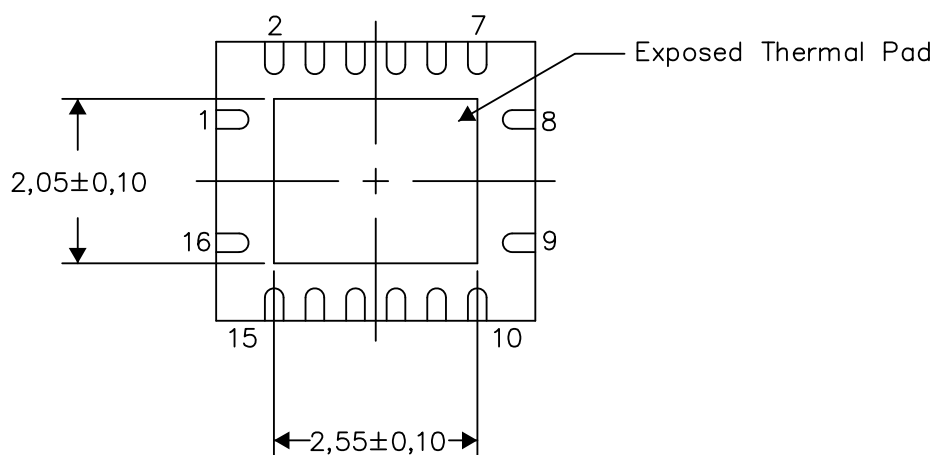
PLASTIC QUAD FLATPACK NO-LEAD

### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

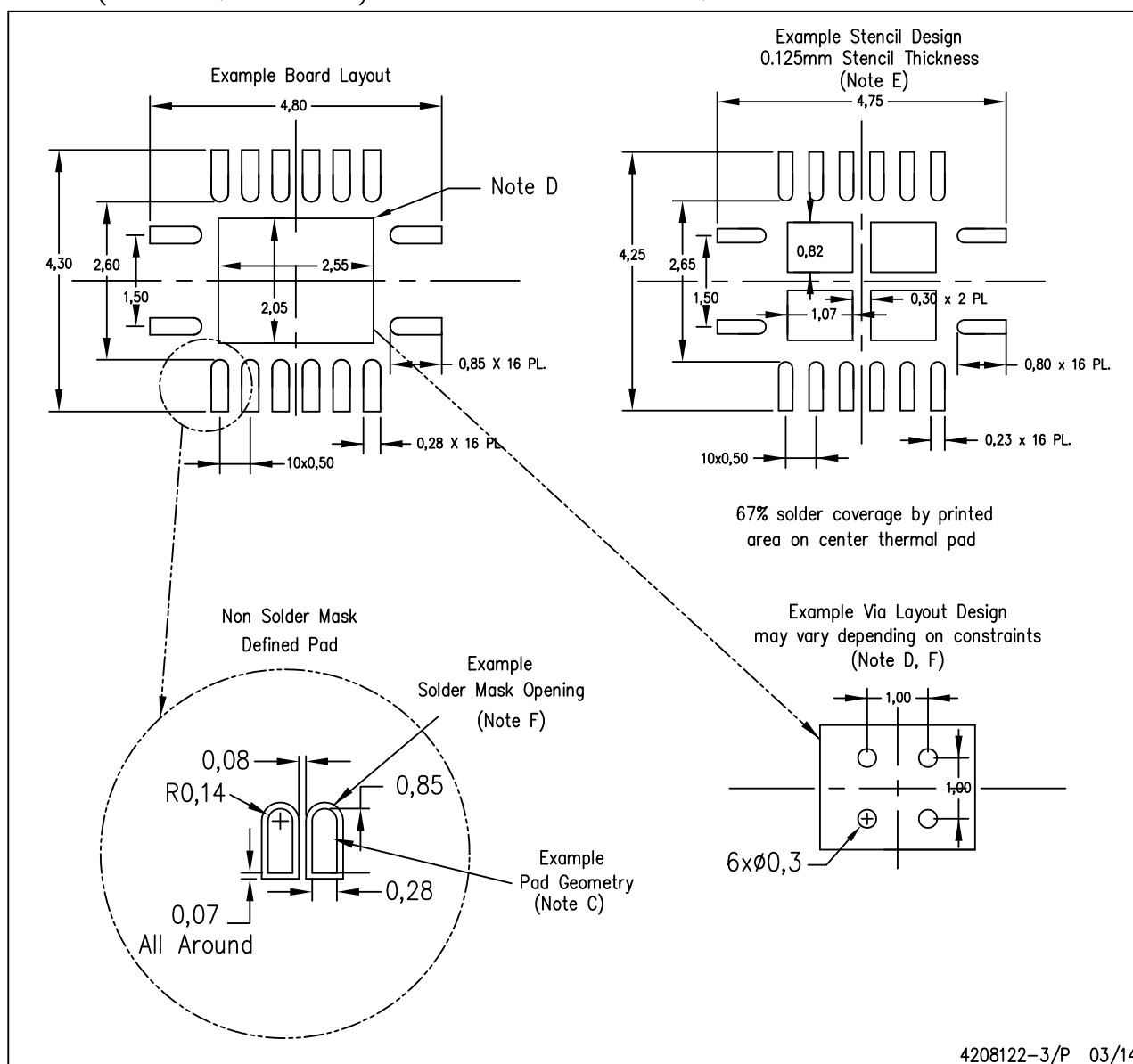
4206353-3/P 03/14

NOTE: All linear dimensions are in millimeters

## LAND PATTERN DATA

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



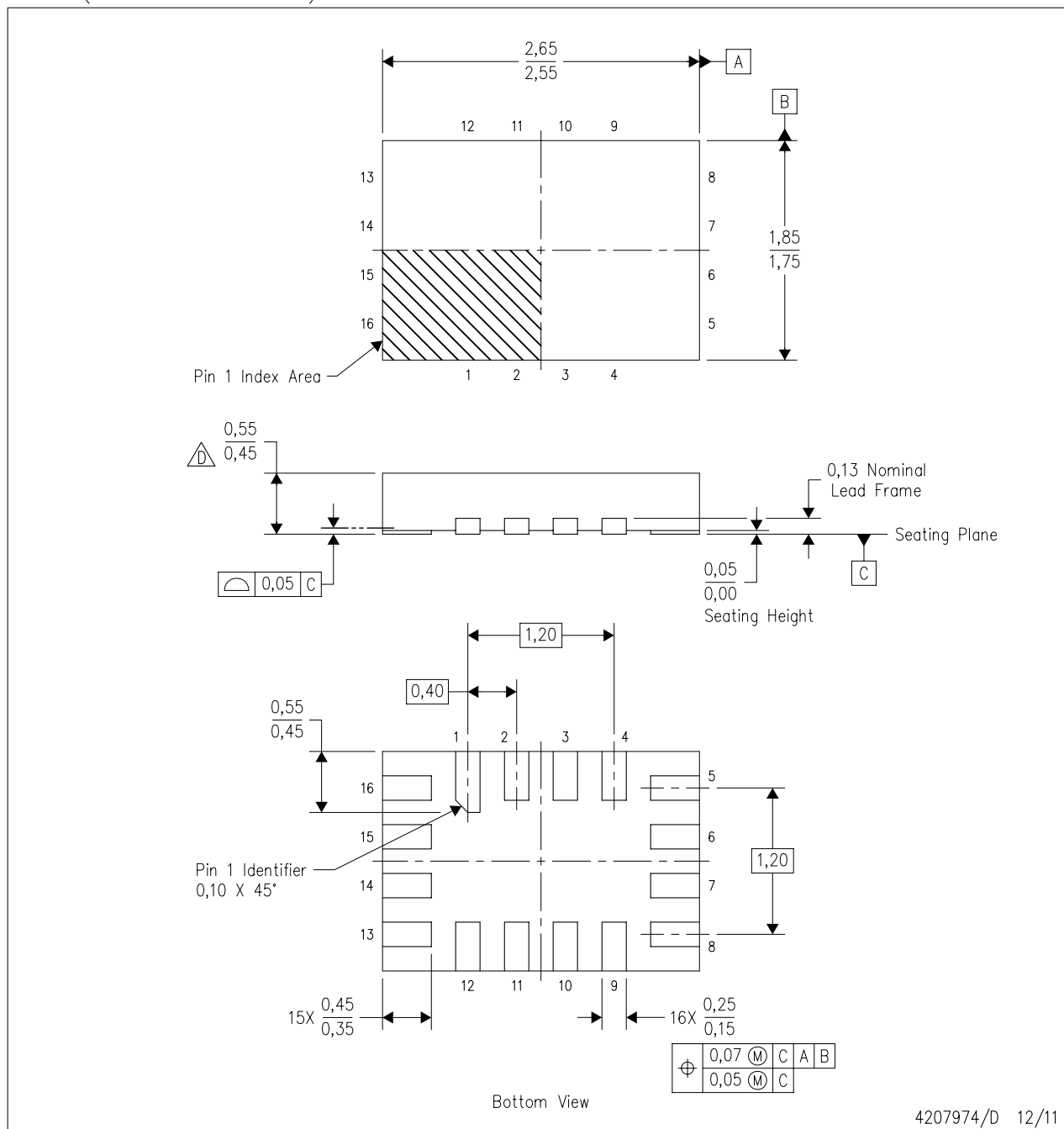
4208122-3/P 03/14

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

## MECHANICAL DATA

RSV (R-PUQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4207974/D 12/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

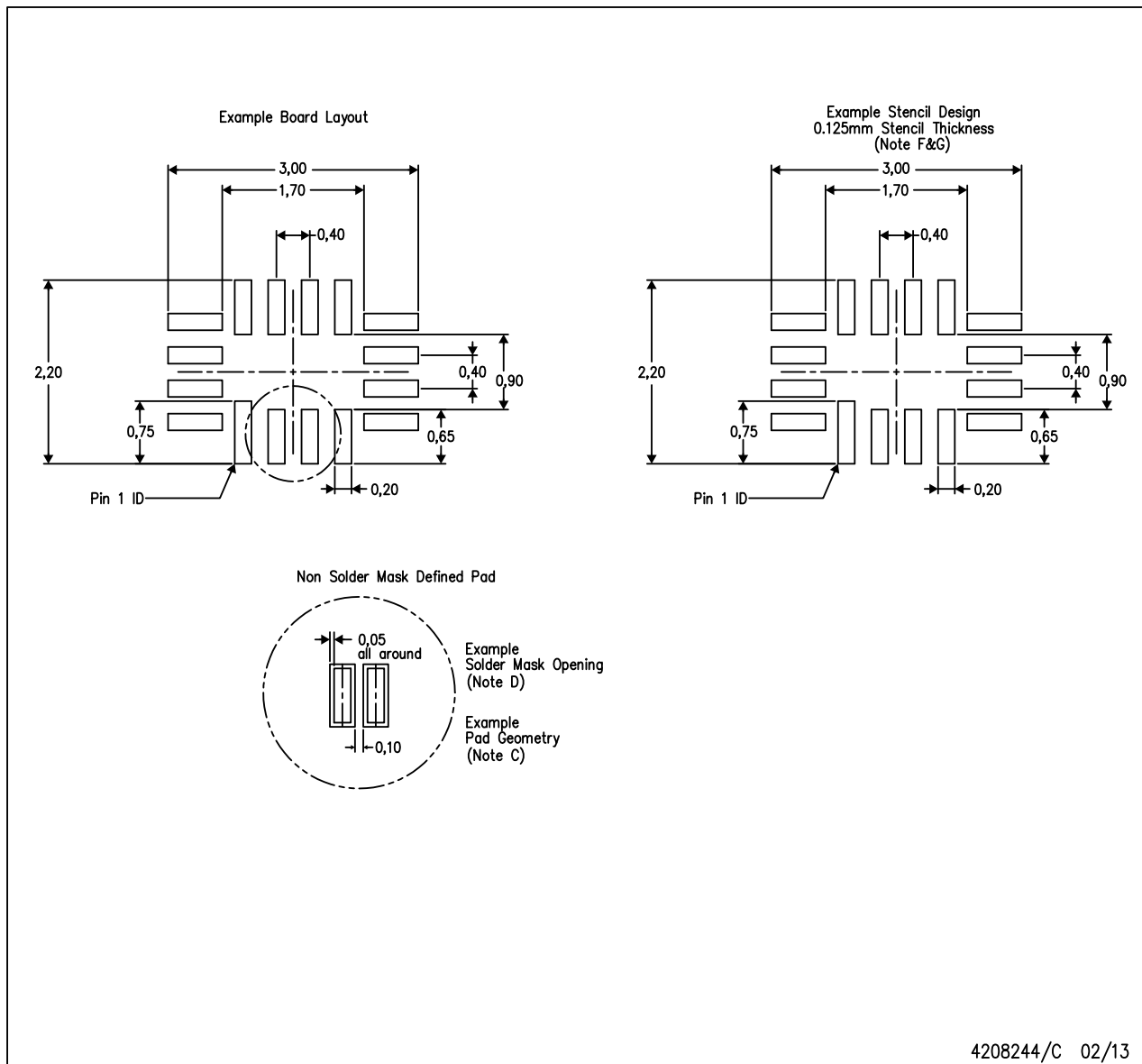
C. QFN (Quad Flatpack No-Lead) package configuration.

This package complies to JEDEC MO-288 variation UFHE, except minimum package thickness.

## LAND PATTERN DATA

RSV (R-PUQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
  - Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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