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[Vishay/Siliconix](#)
[IRFP450NPBF](#)

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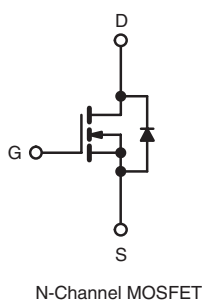
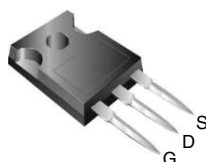
IRFP450N, SiHFP450N

Vishay Siliconix

Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	500	
$R_{DS(on)}$ (Max.) (Ω)	$V_{GS} = 10\text{ V}$	0.37
Q_g (Max.) (nC)	77	
Q_{gs} (nC)	26	
Q_{gd} (nC)	34	
Configuration	Single	

TO-247



FEATURES

- Low Gate Charge Q_g Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Effective C_{oss} Specified
- Lead (Pb)-free


 RoHS
COMPLIANT

APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching

TYPICAL SMPS TOPOLOGIES

- Two Transistor Forward
- Half Bridge and Full Bridge
- PFC Boost

ORDERING INFORMATION	
Package	TO-247
Lead (Pb)-free	IRFP450NPbF SiHFP450N-E3
SnPb	IRFP450N SiHFP450N

ABSOLUTE MAXIMUM RATINGS $T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	V_{DS}	500	V	
Gate-Source Voltage	V_{GS}	± 30		
Continuous Drain Current	V_{GS} at 10 V	$T_C = 25\text{ }^\circ\text{C}$	14	A
		$T_C = 100\text{ }^\circ\text{C}$	8.8	
Pulsed Drain Current ^a		I_{DM}	56	
Linear Derating Factor			1.6	W/ $^\circ\text{C}$
Single Pulse Avalanche Energy ^b	E_{AS}	170	mJ	
Repetitive Avalanche Current ^a	I_{AR}	14	A	
Repetitive Avalanche Energy ^a	E_{AR}	20	mJ	
Maximum Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	P_D	200	W
Peak Diode Recovery dV/dt^c		dV/dt	5.0	V/ns
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to + 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature)	for 10 s		300 ^d	
Mounting Torque	6-32 or M3 screw		10	
			1.1	N · m

Notes


- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting $T_J = 25\text{ }^\circ\text{C}$, $L = 1.7\text{ mH}$, $R_G = 25\text{ }\Omega$, $I_{AS} = 14\text{ A}$ (see fig. 12).
- $I_{SD} \leq 14\text{ A}$, $dI/dt \leq 510\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^\circ\text{C}$.
- 1.6 mm from case.

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THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	40	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.24	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.64	

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	500	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}, I_D = 1\text{ mA}$	-	0.59	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	3.0	-	5.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 30\text{ V}$	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}$	-	-	25	μA
		$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 8.4\text{ A}^b$	-	-	0.37	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 50\text{ V}, I_D = 8.4\text{ A}$	7.9	-	-	S
Dynamic						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}, \text{ see fig. 5}$	-	2260	-	pF
Output Capacitance	C_{oss}		-	210	-	
Reverse Transfer Capacitance	C_{rss}		-	14	-	
Output Capacitance	C_{oss}	$V_{GS} = 0\text{ V}$	$V_{DS} = 1.0\text{ V}, f = 1.0\text{ MHz}$	-	2410	-
			$V_{DS} = 400\text{ V}, f = 1.0\text{ MHz}$	-	59	-
Effective Output Capacitance	$C_{oss\text{ eff.}}$	$V_{DS} = 0\text{ V to } 400\text{ V}^c$	-	110	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}, I_D = 14\text{ A}, V_{DS} = 400\text{ V}, \text{ see fig. 6 and 13}^b$	-	-	77	nC
Gate-Source Charge	Q_{gs}		-	-	26	
Gate-Drain Charge	Q_{gd}		-	-	34	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 250\text{ V}, I_D = 14\text{ A}, R_G = 6.2\text{ }\Omega, V_{GS} = 10\text{ V}, \text{ see fig. 10}^b$	-	20	-	ns
Rise Time	t_r		-	63	-	
Turn-Off Delay Time	$t_{d(off)}$		-	29	-	
Fall Time	t_f		-	25	-	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	14	A
Pulsed Diode Forward Current ^a	I_{SM}		-	-	56	
Body Diode Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = 14\text{ A}, V_{GS} = 0\text{ V}^b$	-	-	1.4	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_F = 14\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}^b$	-	430	650	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	3.7	5.6	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width $\leq 400\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.
- c. $C_{oss\text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80 % V_{DS} .



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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

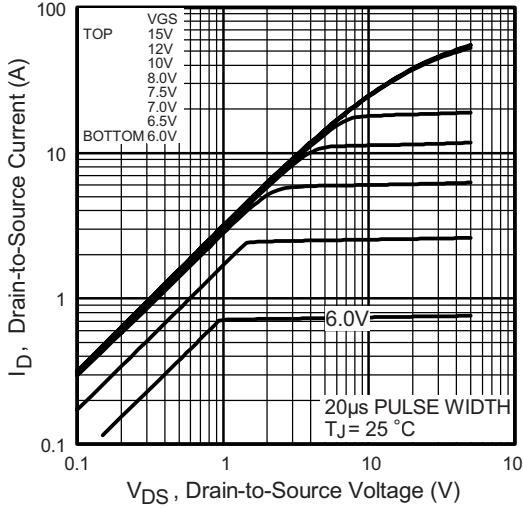


Fig. 1 - Typical Output Characteristics

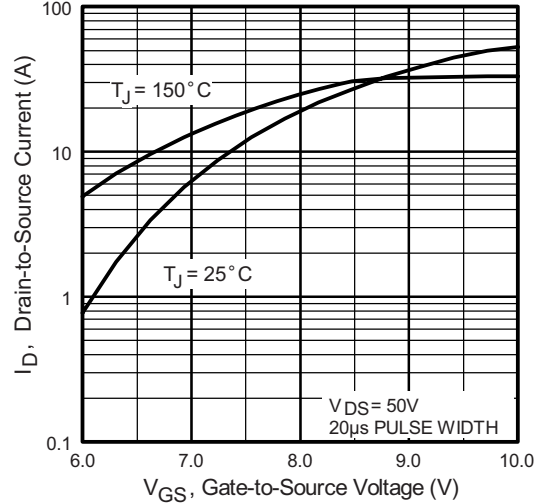


Fig. 3 - Typical Transfer Characteristics

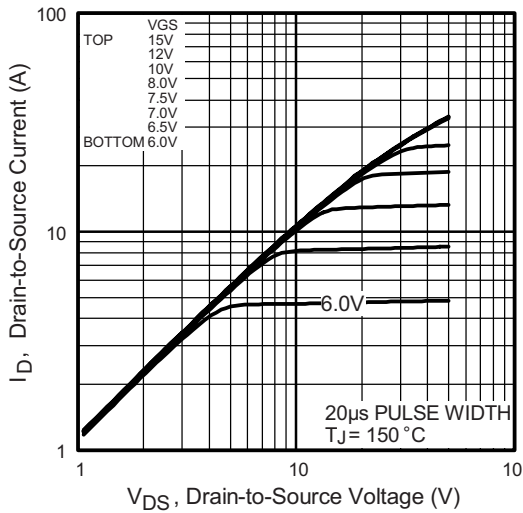


Fig. 2 - Typical Output Characteristics

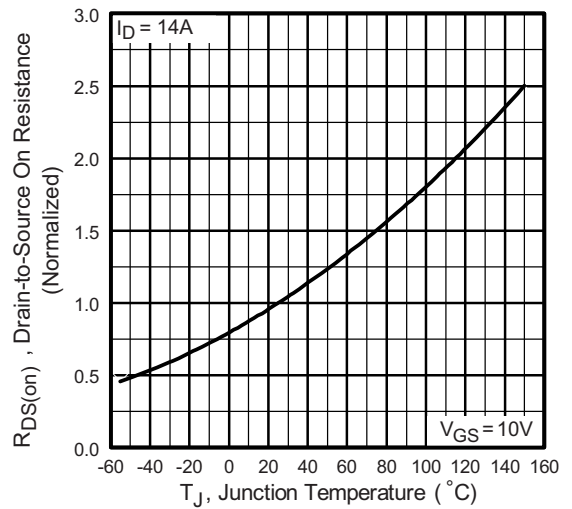


Fig. 4 - Normalized On-Resistance vs. Temperature

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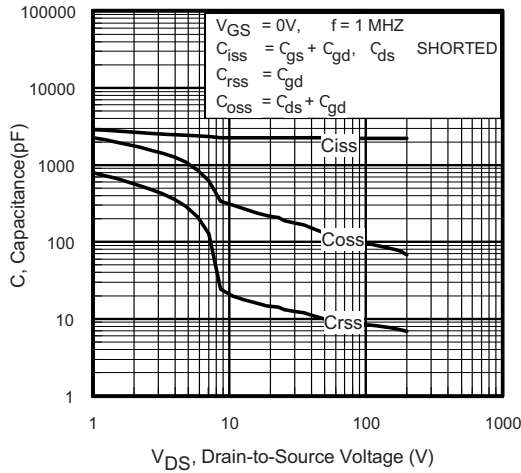


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

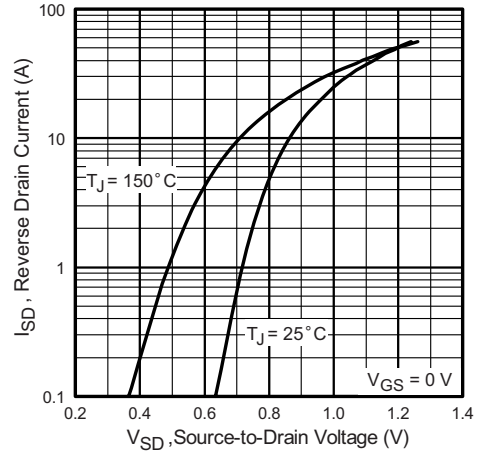


Fig. 7 - Typical Source-Drain Diode Forward Voltage

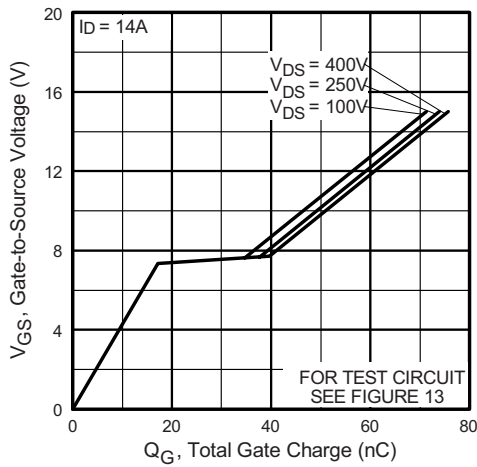


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

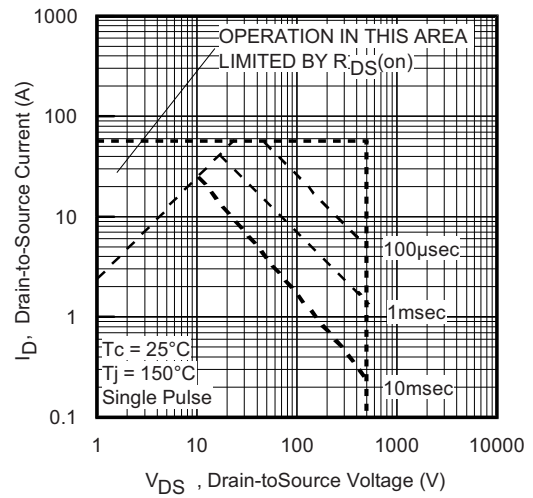


Fig. 8 - Maximum Safe Operating Area



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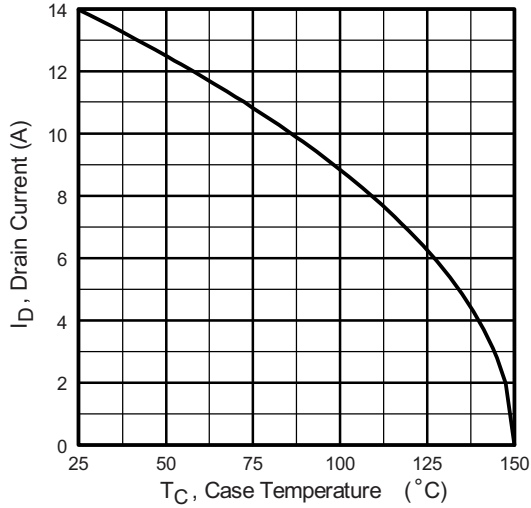


Fig. 9 - Maximum Drain Current vs. Case Temperature

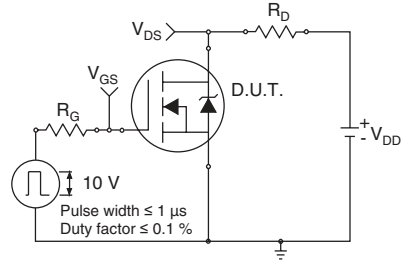


Fig. 10a - Switching Time Test Circuit

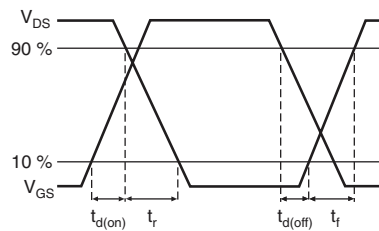


Fig. 10b - Switching Time Waveforms

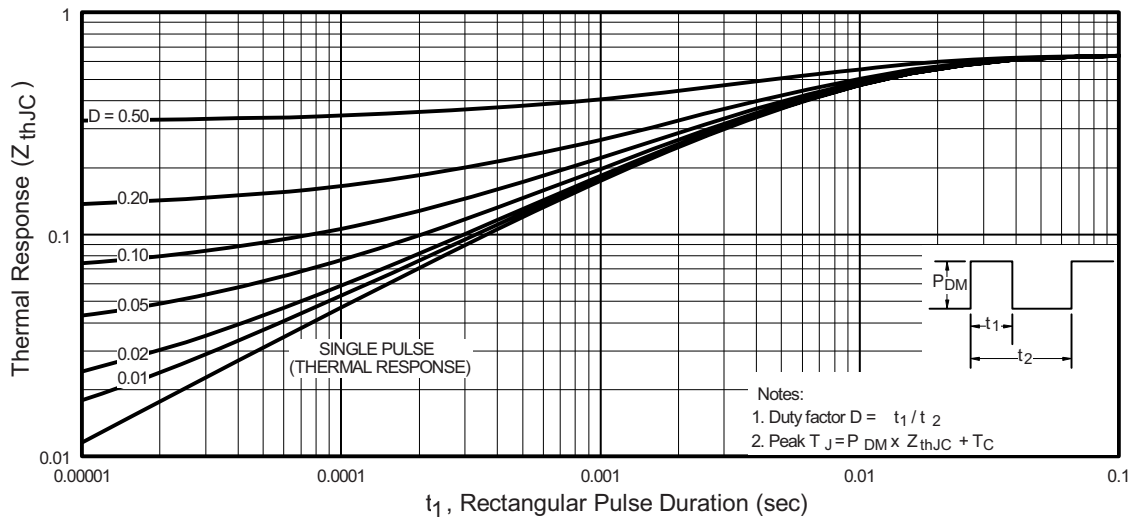


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

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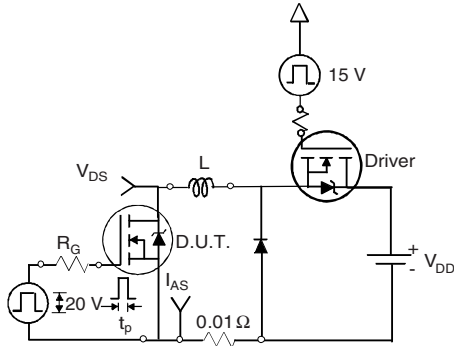


Fig. 12a - Unclamped Inductive Test Circuit

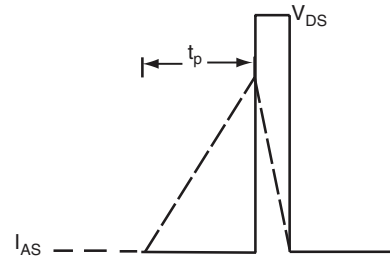


Fig. 12b - Unclamped Inductive Waveforms

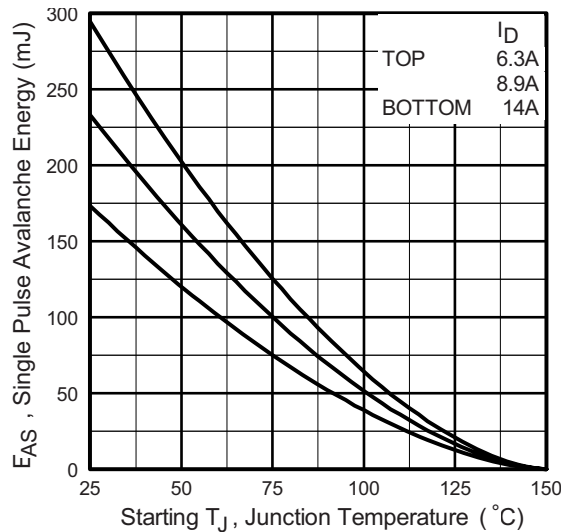


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

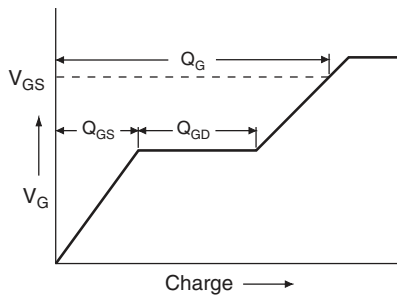


Fig. 13a - Basic Gate Charge Waveform

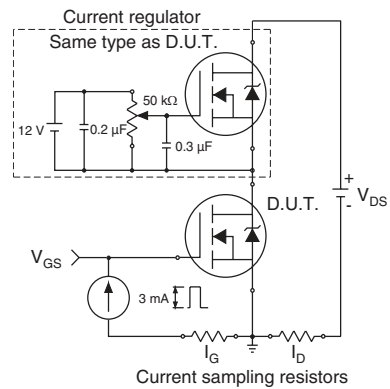


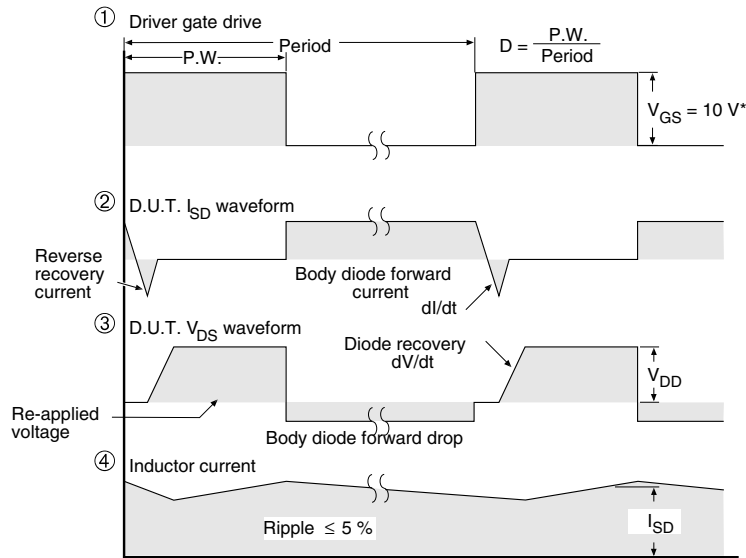
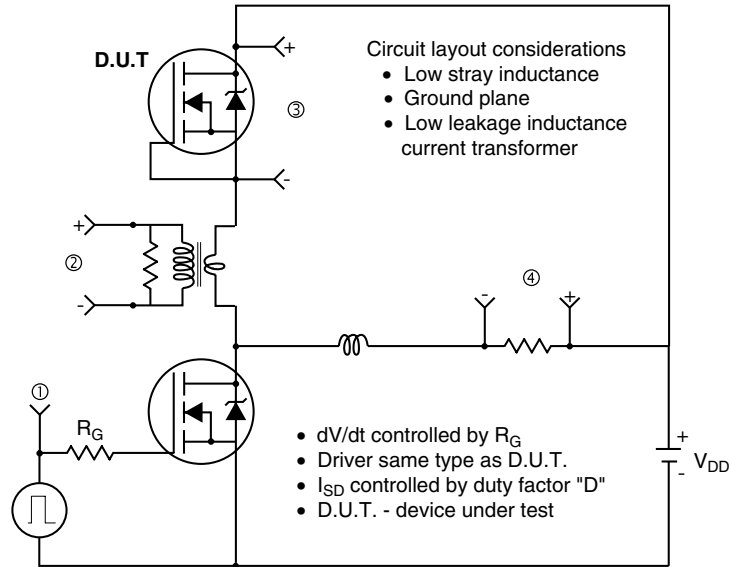
Fig. 13b - Gate Charge Test Circuit



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Peak Diode Recovery dV/dt Test Circuit



* $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 14 - For N-Channel

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