

Excellent Integrated System Limited

Stocking Distributor

Click to view price, real time Inventory, Delivery & Lifecycle Information:

[Intersil](#)
[ISL6173DRZA](#)

For any questions, you can email us directly:
sales@integrated-circuit.com

Dual Low Voltage Hot Swap Controller

This IC targets dual voltage hot swap applications across the +2.5V to +3.3V (nominal) bias supply voltage range with a second lower voltage rail down to less than 1V. It features a charge pump for driving external N-Channel MOSFETs, regulated current protection and duration, output undervoltage monitoring and reporting, optional latch-off or retry response, and adjustable soft-start.

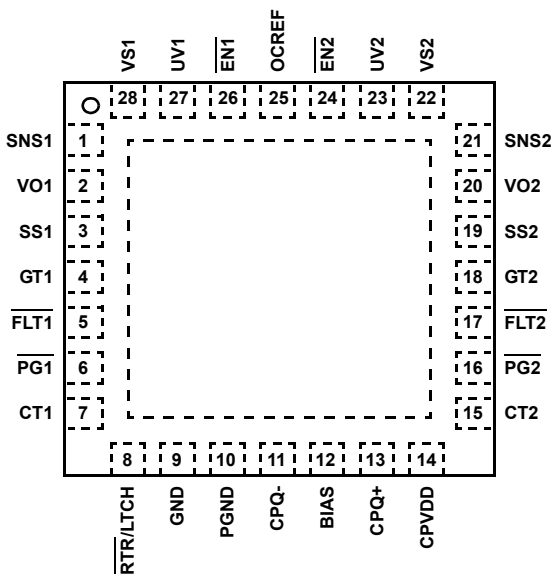
The current regulation level (CR) for each rail is set by two external resistors and each CR duration is set by an external capacitor on the TIM pin. After the CR duration has expired the IC then quickly pulls down the associated GATE(s) output turning off its external FET(s). The ISL6173 offers a latched output or indefinite auto retry mode of operation.

Ordering Information

| PART NUMBER (Note) | PART MARKING | TEMP. RANGE (°C) | PACKAGE (Pb-Free) | PKG. DWG. # |
|--------------------|---------------------|------------------|------------------------------|-------------|
| ISL6173DRZA | ISL6173DRZ | 0 to +85 | 28 Ld 5x5 QFN | L28.5x5 |
| ISL6173DRZA-T | ISL6173DRZ | 0 to +85 | 28 Ld 5x5 QFN Tape & Reel | L28.5x5 |
| ISL6173EVAL3 | Evaluation Platform | | | |

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinout ISL6173 (28 LD QFN) TOP VIEW



Features

- Fast Current Regulation amplifier quickly responds to overcurrent fault conditions
- Less than 1µs response Time to Dead Short
- Programmable Current Regulation Level and Duration
- Two Levels of Overcurrent Detection Provide Fast Response to Varying Fault Conditions
- Overcurrent Circuit Breaker and Fault Isolation functions
- Adjustable Current Regulation Threshold as low as 20mV
- Selectable Latch-off or Auto Retry Response to Fault conditions
- Adjustable voltage ramp-up for In-rush Protection During Turn-On
- Rail Independent Control, Monitoring and Reporting I/O
- Dual Supply Hot Swap Power Distribution Control to <1V
- Charge Pump Allows the use of N-Channel MOSFETs
- QFN Package:
 - Compliant to JEDEC PUB95 MO-220 QFN - Quad Flat No Leads - Package Outline
 - Near Chip Scale Package footprint, which improves PCB efficiency and has a thinner profile
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- Power Supply Sequencing, Distribution and Control
- Hot Swap/Electronic Breaker Circuits

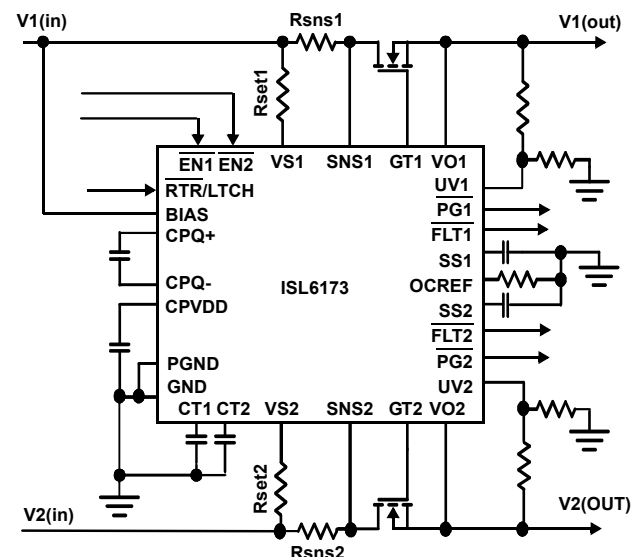


FIGURE 1. TYPICAL APPLICATION

ISL6173

Block Diagram

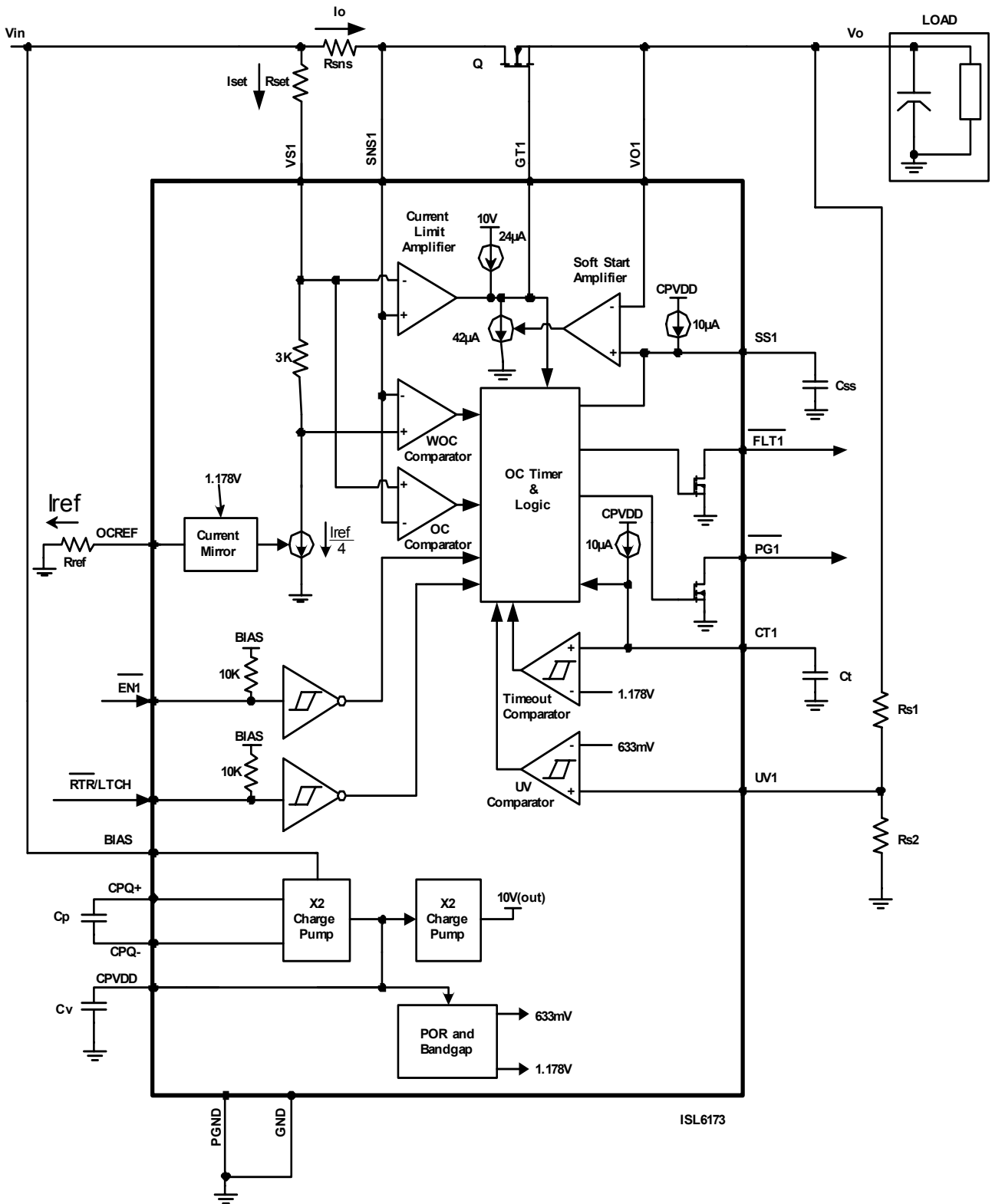
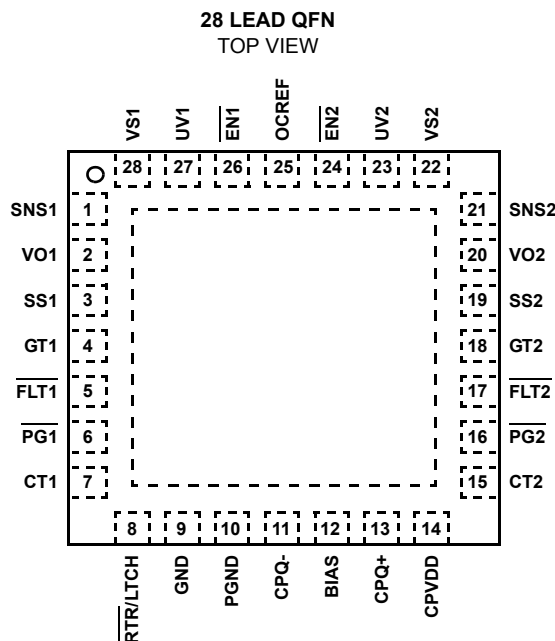


FIGURE 2. ISL6173 - INTERNAL BLOCK-DIAGRAM OF THE IC - CHANNEL ONE ONLY

ISL6173

Pinout



Pin Descriptions

| PIN | NAME | FUNCTION | DESCRIPTION |
|-----|----------|-------------------------------|---|
| 1 | SNS1 | Current Sense Input | This pin is connected to the current sense resistor and control MOSFET Drain node. It provides current sense signal to the internal comparator and amplifier in conjunction with VS1 pin. |
| 2 | VO1 | Output Voltage 1 | This pin is connected to the control MOSFET switch source, which connects to a load. Internally, this voltage is used for SS control. |
| 3 | SS1 | Soft-Start Duration Set Input | A capacitor from this pin to ground sets the output soft-start ramp slope. This capacitor is charged by the internal 10µA current source setting the soft-start ramp. The output voltage ramp tracks the SS ramp by controlled enhancement of FET gate. Once ramp-up is completed, the capacitor continues to charge to the CPVDD voltage rail. If common capacitor is used (by tying SS1, SS2 together and the capacitor to GND from the connection) then both the outputs track each other as they ramp up. |
| 4 | GT1 | Gate Drive Output | Direct connection to the gate of the external N-Channel MOSFET. At turn-on the Gate will charge to 4 X Vbias or 10V(max) from the 24µA source. |
| 5 | FLT1 | Fault Output | This is an open drain output. It asserts (pulls low) once the current regulation duration (determined by the CTx timeout cap) has expired. This output is valid for Vbias>1V. |
| 6 | PG1 | Power Good Output | This is an active low, open drain output. When asserted (logic zero), it indicates that the voltage on UV1 pin is more than 643mV (633mV + 10mV hysteresis). This output is valid at VBIAS >1V. |
| 7 | CT1 | Timer Capacitor | A capacitor from this pin to ground controls the current regulation duration from the onset of current regulation to channel shutdown (current limit time-out). Once the voltage on CTx cap reaches V_{CT_Vth} the GATE output is pulled down and the FLT is asserted. $The\ duration\ of\ current\ limit\ time-out = (C_{TIM} * 1.178) / 10\mu A$ When the OC comparator trips AND the RTR/LTCH pin is pulled low, the IC's faulty channel remains shut down for 64 cycles (each cycle length is equal to the current limit time-out duration). |
| 8 | RTR/LTCH | Retry Or Latch Input | This input dictates the IC behavior (for either channel) under OC condition. If it is pulled high (or left floating), the IC will shut down upon OC time-out. If it is pulled low, the IC will go into retry mode after an interval determined by the capacitor on CTx pin. The faulting channel will remain shut down for 64 cycles and will try to come out of it on the 65th cycle. Each cycle length is determined by the formula shown in CT pin description. |
| 9 | GND | Chip Gnd | This pin is also internally shorted to the metal tab at the bottom of the IC. |
| 10 | PGND | | Charge pump ground. Both GND and PGND must be tied together externally. |

ISL6173

Pin Descriptions (Continued)

| PIN | NAME | FUNCTION | DESCRIPTION |
|-----|--------------------------|---------------------------------|--|
| 11 | CPQ- | Charge Pump Capacitor Low Side | Flying cap lowside. |
| 12 | BIAS | Chip Bias Voltage | Provides IC Bias. Should be 2V to 4V for IC to function normally. This pin can be powered from a supply voltage that is not being controlled. It is preferable to use 3.3V even if the channels being controlled are 2.5V or lower because more gate drive voltage will be available to the MOSFETs. |
| 13 | CPQ+ | Charge Pump Capacitor High Side | Flying cap highside. Use of 0.1 μ F for 2.5V bias and 0.022 μ F for 3.3V bias is recommended. |
| 14 | CPVDD | Charge Pump Output | This is the voltage used for some internal pullups and bias. Use of 0.47 μ F (minimum) is recommended. |
| 15 | CT2 | Timer Capacitor | Same function as pin 7 |
| 16 | $\overline{\text{PG2}}$ | Power Good Output | Same function as pin 6 |
| 17 | $\overline{\text{FLT2}}$ | Fault Output | Same as pin 5 |
| 18 | GT2 | Gate Drive Output | Same as pin 4 |
| 19 | SS2 | Soft-Start Duration Set Input | Same as pin 3 |
| 20 | VO2 | Output Voltage 2 | Same as pin 2 |
| 21 | SNS2 | Current Sense Input | Same as pin 1 |
| 22 | VS2 | Current Sense Reference | Voltage input for one of the two voltages. Provides a 20 μ A current source for the ISET series resistor which sets the voltage to which the sense resistor IR drop is compared. |
| 23 | UV2 | Undervoltage Monitor Input | This pin is one of the two inputs to the undervoltage comparator. The other input is the 633mV reference. It is meant to sense the output voltage through a resistor divider. If the output voltage drops so that the voltage on the UV pin goes below 633mV, $\overline{\text{PG2}}$ is deasserted. |
| 24 | $\overline{\text{EN2}}$ | Enable | This is an active low input. When asserted (pulled low), the SS and gate drive are released and the output voltage gets enabled. When deasserted (pulled high or left floating), the reverse happens. |
| 25 | OCREF | Ref. Current Adj. | Allows adjustment of the reference current through R _{SET} and the internal current regulation set resistor, thus setting the thresholds for CR, OC and WOC. |
| 26 | $\overline{\text{EN1}}$ | Enable Input | Same as pin 24 |
| 27 | UV1 | Undervoltage Monitor Input | Same as pin 23 |
| 28 | VS1 | Current Sense Reference | Same as pin 22 |

ISL6173

Absolute Maximum Ratings

| | |
|---|-------------------------|
| VBIAS | +5.5V |
| GTx, CPQ+ | -0.3V to +12V |
| ENx, RTR/LTCH, SNSx, PGx, FLTx, VSx, CTx, UVx, SSx, CPQ-, CPVDD | -0.3V to 5.5VDC |
| Output Current | Short Circuit Protected |
| ESD Rating | |
| Human Body Model (Per MIL-STD-883 Method 3015.7) | 1750V |
| Machine Model (Per EIAJ ED-4701 Method C-111) | 125V |
| Charged Device Model (Per EOS/ESD DS5.3, 4/14/93) | 1750V |

Thermal Information

| | | |
|---|----------------------|----------------------|
| Thermal Resistance (Typical, Notes 1, 4) | θ_{JA} (°C/W) | θ_{JC} (°C/W) |
| 5x5 QFN Package | 42 | 12.5 |
| Maximum Junction Temperature | 150°C | |
| Maximum Storage Temperature Range | -65°C to 150°C | |
| For recommended soldering conditions, see Tech Brief TB389. (QFN - Leads Only) | | |

Operating Conditions

| | |
|-------------------------------------|------------------|
| VBIAS/VIN1 Supply Voltage Range | +2.25V to +3.63V |
| Temperature Range (T _A) | 0°C to 85°C |

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

- θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
- All voltages are relative to GND, unless otherwise specified.
- 1V (min) on the BIAS pin required for \overline{FLT} to be valid.
- For θ_{JC} , the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications $V_{DD} = 2.5V$ to $+3.3V$, $V_S = 1V$, $T_A = T_J = 0^\circ C - 85^\circ C$, Unless Otherwise Specified.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|-----------------------|--|-------|-------|-------|---------|
| CURRENT REGULATION CONTROL | | | | | | |
| ISET Current | I _{SET_ft} | R _{OCREF} = 14.7k Ω | 18.7 | 20 | 21.3 | μA |
| Partial Temp Range I _{SET} Current | I _{SET_pt} | R _{OCREF} = 14.7k Ω T _J = 25°C to 60°C | 19 | 20 | 21 | μA |
| Current Limit Amp Offset Voltage | V _{io_ft} | V _{VS} - V _{SNS} with I _{OUT} = 0A | -2 | | 2 | mV |
| Partial Temp. Current Limit Amp Offset Voltage | V _{io_pt} | V _{VS} - V _{SNS} with I _{OUT} = 0A T _J = 25°C to 60°C | -1 | | 1 | mV |
| Current Regulation Threshold Voltage | V _{CRVTH_1} | R _{ISET} = 1.25K, I _{SET} = 20 μA | 23 | 25 | 27 | mV |
| Current Regulation Accuracy | V _{CRVTH_1R} | R _{ISET} = 1.25K, I _{SET} = 20 μA | -8 | | +8 | % |
| Current Regulation Threshold Voltage | V _{CRVTH_2} | R _{ISET} = 2.50K, I _{SET} = 20 μA | 48 | 50 | 52 | mV |
| Current Regulation Accuracy | V _{CRVTH_2R} | R _{ISET} = 2.50K, I _{SET} = 20 μA | -4 | | +4 | % |
| Current Regulation Threshold Voltage | V _{CRVTH_3} | R _{ISET} = 0.499K, I _{SET} = 20 μA | 8 | 10 | 12 | mV |
| Current Regulation Accuracy | V _{CRVTH_3R} | R _{ISET} = 0.499K, I _{SET} = 20 μA | -20 | | +20 | % |
| CT Threshold Voltage | V _{CT_vth} | | 1.128 | 1.178 | 1.202 | V |
| CT Charging Current | I _{CT} | | | 10 | | μA |
| GATE DRIVE | | | | | | |
| GATE Response Time from WOC (Open) | pd_woc_open | GATE open 100mV of overdrive on the WOC comparator | | 3 | | ns |
| GATE Response Time from WOC (Loaded) | pd_woc_load | GATE = 1nF | | 100 | | ns |
| GATE Response Time in Current Regulation mode (Loaded) | pd_cr_load | GATE = 1nF 120% Load Current | | 5 | | μs |
| GATE Turn-On Current | IGATE | GATE = 2V, V _{VS} = 2V, V _{SNS} = 2.1V | 21 | 24 | 27 | μA |

ISL6173

Electrical Specifications $V_{DD} = 2.5V$ to $+3.3V$, $V_S = 1V$, $T_A = T_J = 0^\circ C - 85^\circ C$, Unless Otherwise Specified. (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--------------------|---|-------|------|------|---------|
| GATE Voltage | V_{GATE} | Bias = 2.5V (see graph on page 7) | 7.5 | | 9.0 | V |
| | | $2.1 < \text{Bias} < 2.5$ (see graph on page 7) | | 8 | | V |
| BIAS | | | | | | |
| Supply Current | I_{BIAS} | $V_{BIAS} = 3.3V$ | | 9 | 17 | mA |
| POR Rising Threshold | $V_{IN_POR_L2H}$ | | | | 2.12 | V |
| POR Falling Threshold | $V_{IN_POR_H2L}$ | | | | 2.10 | V |
| POR Threshold Hysteresis | $V_{IN_POR_HYS}$ | | 5 | | | mV |
| I/O | | | | | | |
| Undervoltage Comparator Falling Threshold | V_{UV_VTHF} | | 620 | 635 | 650 | mV |
| Undervoltage Comparator Hysteresis | V_{UV_HYST} | | 7 | 16 | 25 | mV |
| \overline{EN} Rising Threshold | PWR_Vth_R | $V_{BIAS} = 2.5V$ | 1.55 | 1.95 | 2.19 | V |
| \overline{EN} Falling Threshold | PWR_Vth_F | $V_{BIAS} = 2.5V$ | 0.97 | 1.10 | 1.30 | V |
| \overline{EN} Hysteresis | PWR_HYST | $V_{BIAS} = 2.5V$ | 600 | 850 | 1100 | mV |
| \overline{PG} Pull-Down Voltage | VOL_PG | $I_{PG} = 8mA$ | 0.047 | | 0.4 | V |
| \overline{FLT} Pull-Down Voltage (Note 3) | VOL_FLT | $I_{FLT} = 8mA$ | 0.047 | | 0.4 | V |
| Soft-Start Charging Current | I_{Q_SS} | $V_{SS} = 1V$ | | 10 | | μA |
| CHARGE PUMP | | | | | | |
| CPVDD | V_CPVDD | $V_{BIAS} = 3.3V$ | 4.9 | 5.2 | 5.5 | V |
| CPVDD | V_CPVDD | $V_{BIAS} = 3.3V$ $T = 25^\circ C$ External User Load = 6mA | | 5.0 | | V |

ISL6173

Typical Performance Curves (at 25°C unless otherwise specified)

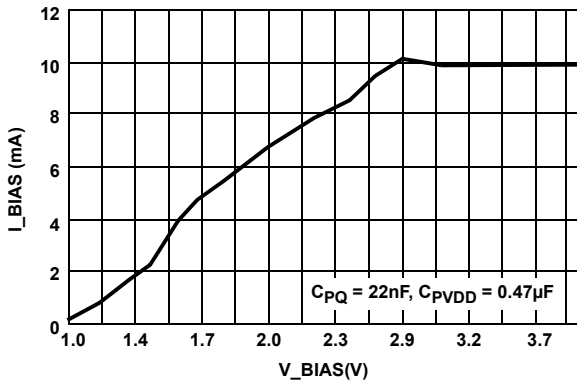


FIGURE 3. I_BIAS vs V_BIAS

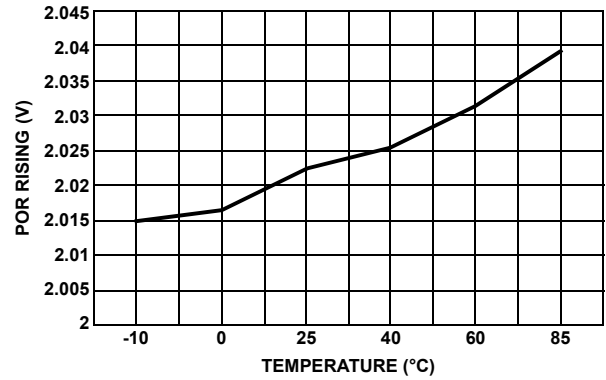


FIGURE 4. POR RISING THRESHOLD vs TEMPERATURE

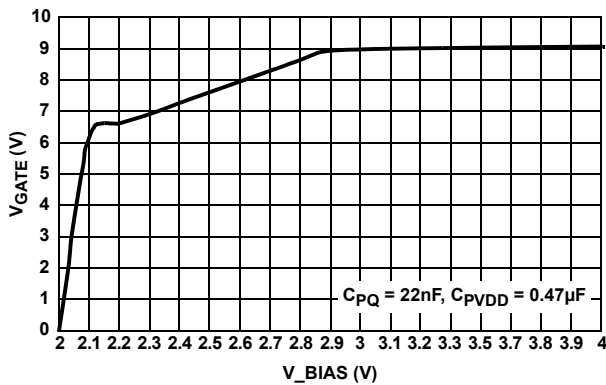


FIGURE 5. V_GATE vs V_BIAS

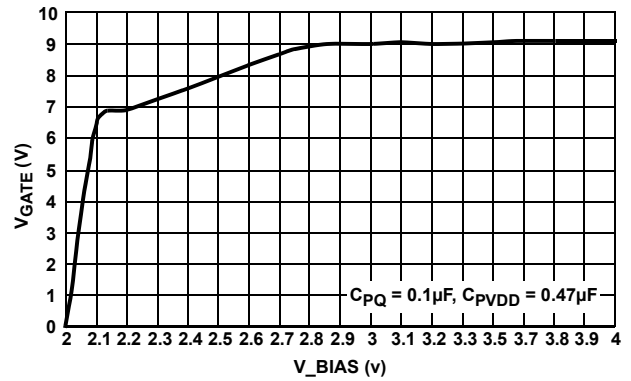


FIGURE 6. V_GATE vs V_BIAS

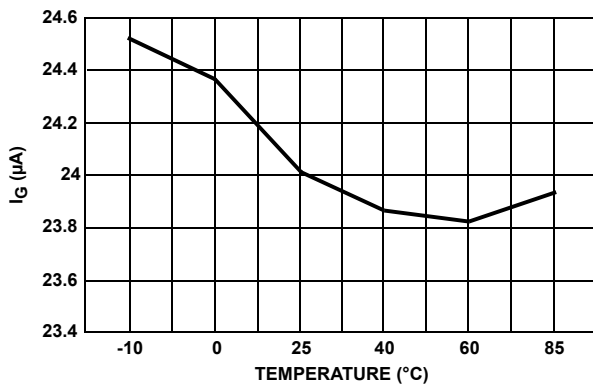


FIGURE 7. GATE DRIVE vs TEMPERATURE

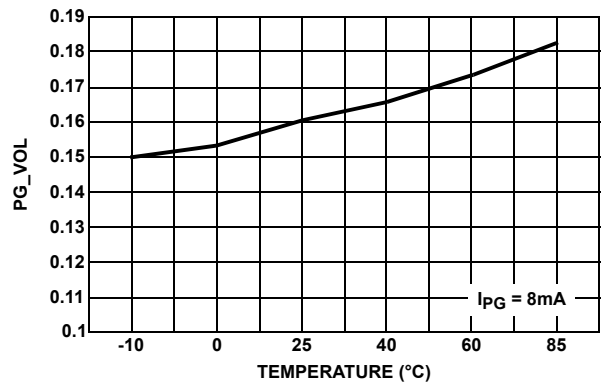


FIGURE 8. PG_VOL vs TEMPERATURE

ISL6173

Typical Performance Curves (at 25°C unless otherwise specified) (Continued)

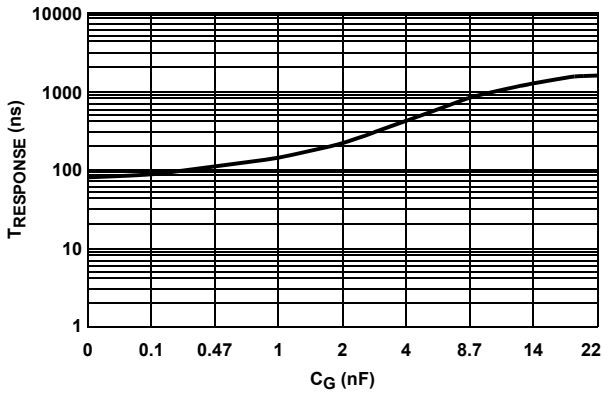


FIGURE 9. WOC RESPONSE vs LOAD CAPACITANCE

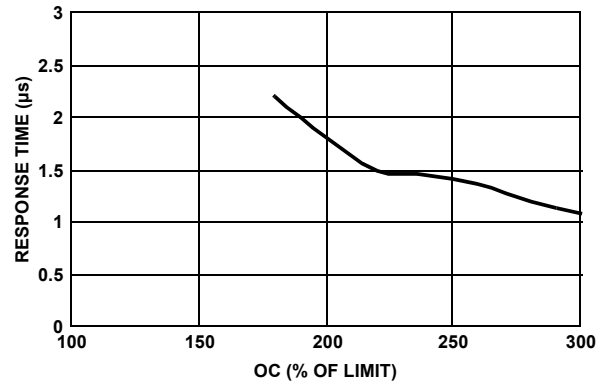


FIGURE 10. RESPONSE TIME vs $I_O \cdot R_{SNS}$

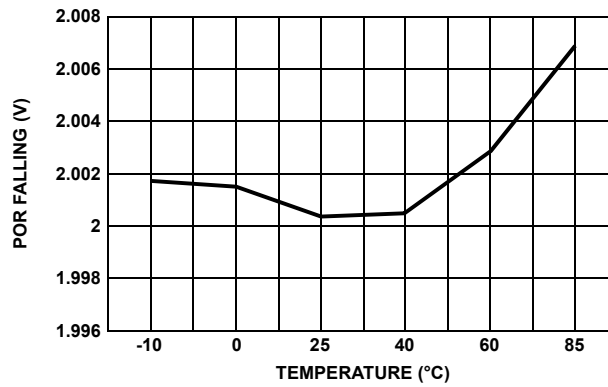


FIGURE 11. POR FALLING vs TEMPERATURE

ISL6173

Detailed Description of Operation

ISL6173 targets dual voltage hot-swap applications with a bias of 2.1V to 3.6VDC and the voltages being controlled down to 0.7VDC. The IC's main function is to limit and regulate the inrush current into the loads. This is achieved by enhancing an external MOSFET in a controlled manner. In order to fully enhance the MOSFET, the IC must provide adequate gate to source voltage, which is typically 5V or greater. Hence, the final steady-state voltage on Gate (GT) pin must be 5V above the load voltage. Two internal charge-pumps allow this to happen.

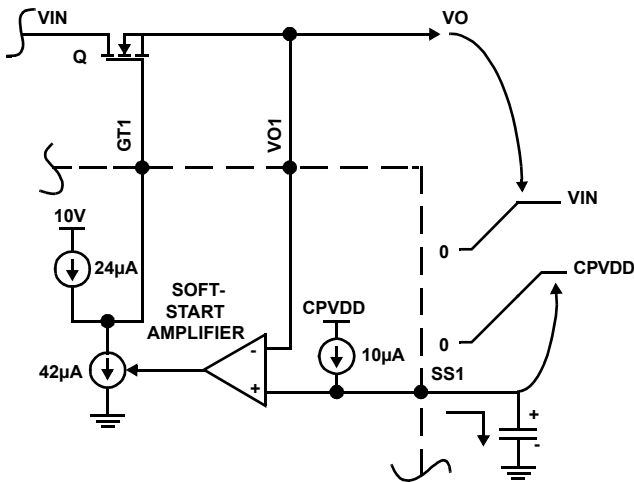


FIGURE 12. SOFT-START OPERATION

Controlled Soft-Start

The output voltages are monitored through the Vo pins and slew up at a rate determined by the capacitors on the Soft-start (SS) pin, as illustrated in Figure 12. 24µA of gate charge current is available. The soft-start amplifier controls the output voltage by robbing some of the gate charge current thus slowing down the MOSFET enhancement. When the load voltage reaches its set level, as sensed by its respective UV pin through an external resistor divider, the Power Good (PG) output goes active.

Current Monitoring and Protection

The IC monitors the load current (Io) by sensing the voltage-drop across the low value current sense resistor (RSNS), which is connected in series with the MOSFET as shown in the diagram on page 2, through Sense (SNS) and voltage set (VS) pins. The latter is through a resistor, RSET, as shown. Two levels of overcurrent detection are available to protect against all possible fault scenarios. These levels are:

1. Current Limit or Current Regulation (CR)
2. Way Overcurrent (WOC)

Each of these modes is described in detail as follows:

1. Current Limit or Current Regulation (CR) Mode: - When the load current reaches the current regulation threshold, the current amplifier loop closes and the circuit behaves like a current source. The Current Limit Amplifier is a folded cascode type with source follower output capable of pulling down the gate very fast in response to fast overload transients. The current regulation threshold is set by setting a reference current, ISET, through RSET by selecting an appropriate resistor between OCREF and GND, which sets IREF. The relationship between IREF and ISET is IREF = 4*ISET, where IREF = Vocref/Rocref = 1.178/Rocref. IREF would typically be set at 80µA.

Selecting appropriate values for RSET and RSNS such that when Io = ICR,

$$I_o * R_{SNS} = I_{SET} * R_{SET} \tag{EQ. 1}$$

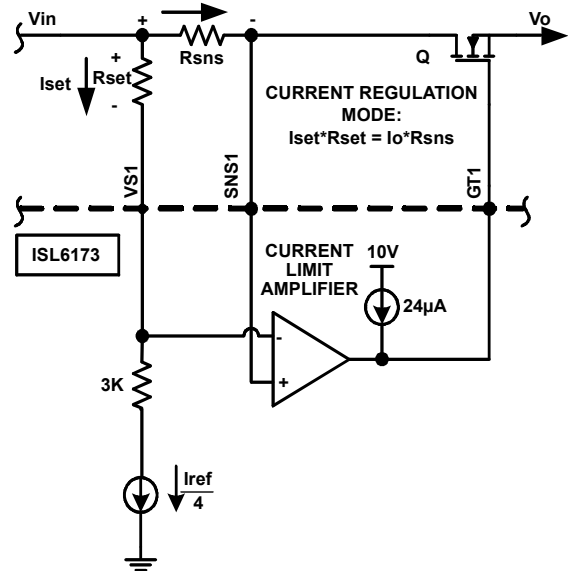


FIGURE 13. CURRENT REGULATION OPERATION

The operating mode is shown in Figure 13. When the circuit enters this mode, the OC comparator detects it and sets off the timer. CT begins to charge from an internal 10µA current source. The amount of time it takes for this cap to charge to 1.178V sets up the current regulation duration. Upon expiration of this time-out period, the MOSFET gate is pulled down quickly by the current limit amplifier, unless the load current level had already dropped back to a level below the current regulation threshold level prior to that. In that case, the current regulation mode is no longer active, the MOSFET is allowed to fully enhance and the IC discharges the CT Cap. If RTR/LTCH pin is left open or pulled to BIAS, the output remains latched off after the expiration of the time-out period determined by CT. If RTR/LTCH pin is pulled to GND, the IC

ISL6173

automatically retries to turn on the MOSFET after a wait period, during which C_T is charged and discharged 64 times and the retry attempt takes place on the 65th time. This wait period allows the MOSFET junction to cool down.

2. Way Overcurrent (WOC) Mode - This mode is designed to handle very fast, very low impedance shorts on the load side, which can result in very high di/dt. Typically, the current limit set for this mode is 300% of the current regulation limit. This mode uses a very fast comparator, which directly looks at the voltage drop across R_{SNS} and pulls the gate very quickly to GND (as shown in Figure 14) and immediately releases it. If the WOC is still present, the IC enters current regulation mode and the rest of the current regulation behavior follows as described earlier in undercurrent regulation mode.

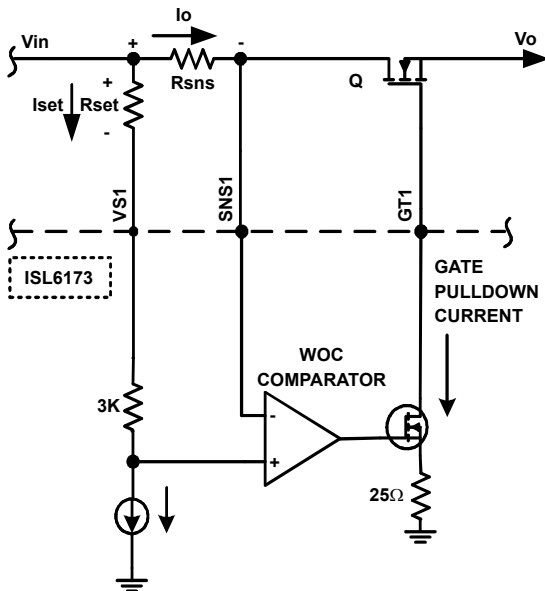


FIGURE 14. WOC OPERATION

Additionally, as shown in the block diagram, there is also an “OC comparator”, which also looks at the Rsense voltage drop. When this drop exceeds the Current Limit set point, it triggers the timeout circuit, which starts ticking and CT_x is allowed to charge. If the current limit condition remains in effect until after the time-out period expires (CT_x voltage exceeding 1.178V), the gate of the MOSFET is pulled down, the SS_x capacitor is discharged, \overline{FLT} is asserted and a new SS sequence is allowed to begin after \overline{EN}_x recycle or by keeping the $\overline{RTR}/\overline{LTCH}$ pin pulled low.

The voltage on $OCREF$ pin is the same as the internal band-gap reference voltage, which is 1.178V (nominal). A resistor to GND from this pin sets the reference current (and hence the reference voltage) for the current limit amplifier and OC/WOC comparators. The current regulation (CR) duration is set by the capacitor on CT pin to GND. Once the voltage

on this pin reaches 1.178V, the CR duration expires. Fault (\overline{FLT}) pin goes active (pulls low), signaling the load of a fault condition and the gate (GT) pin gets pulled low.

Retry vs Latched Fault Operational Modes:

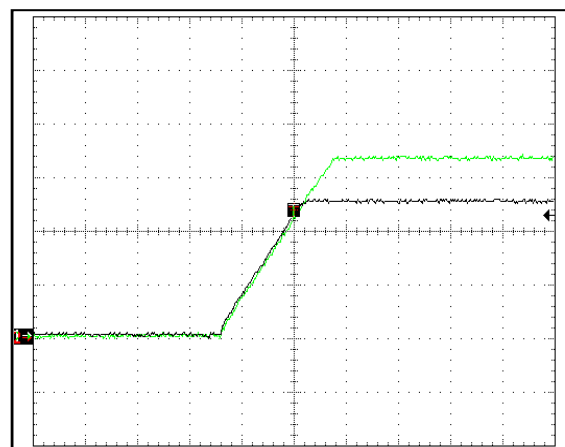
$\overline{RTR}/\overline{LTCH}$ pin dictates the IC behavior after the gate (GT) pin pulls down following OC timeout expiration. If the $\overline{RTR}/\overline{LTCH}$ pin is left floating, the gate pin will remain latched off. It can only be released by de-asserting and reasserting the enable (\overline{EN}) input. If $\overline{RTR}/\overline{LTCH}$ pin is pulled to GND, then the Retry mode will be activated. In this mode the IC will automatically attempt to turn-on the MOSFET after a delay, determined by the capacitor on CT pin. In the Retry mode, the internal logic charges and discharges the CT cap 64 times during “wait” period. On the 65th time, the \overline{FLT} output clears during retry attempt. If the overcurrent condition persists after the soft-start, the CT pin will again start charging and the process repeats.

Bias and Charge Pump Voltages:

The BIAS pin feeds the chip bias voltage directly to the first of the two internal charge pumps, which are cascaded. The output of the first charge pump, in addition to feeding the second charge pump, is accessible on the $CPVDD$ pin. The voltage on the $CPVDD$ pin is approximately 5V. It also provides power to the POR and band-gap circuitry as shown in the block diagram. A capacitor connected externally across $CPQ+$ and $CPQ-$ pins of the IC is the “flying” cap for the charge-pump.

The second charge-pump is used exclusively to drive the gates of the MOSFETs through the $24\mu A$ current sources, one for each channel. The output of this charge pump is approximately 10V as shown in the block diagram.

Tracking



CH1: V_{O1} , CH2: V_{O2} , T = 2ms/DIV, $C_{SS} = 0.066\mu F$

FIGURE 15. TRACKING MODE WAVEFORMS

ISL6173

The two channels can be forced to track each other by simply tying their SS pins together and using a common SS capacitor. In addition, their $\overline{\text{EN}}$ pins also must be tied together. Typical Start-up waveforms in this mode are shown in Figure 15. If one channel goes down for any reason, the other one will too. One important thing to note here is that only the overcurrent latch-off mode will work. Auto-retry feature WILL NOT work. Retry must be controlled manually through EN.

Typical Hot-plug Power Up Sequence

1. When power is applied to the IC on the BIAS pin, the first charge pump immediately powers up.
2. If the BIAS voltage is 2.1V or higher, the IC comes out of POR. Both SS and CT caps remain discharged and the gate (GT) voltage remains low.
3. $\overline{\text{EN}}$ pin, when pulled low (below it's specified threshold), enables the respective channel.
4. SSx cap begins to charge up through the internal 10 μ A current source, the gate (GT) voltage begins to rise and the corresponding output voltage begins to rise at the

same rate as the SS cap voltage. This is tightly controlled by the soft-start amplifier shown in the block diagram.

5. SS cap begins to charge but the corresponding CTx cap is held discharged.
6. Fault ($\overline{\text{FLT}}$) remains deasserted (stays high) and the output voltage continues to rise.
7. If the load current on the output exceeds the set current limit for greater than the OC timeout period, $\overline{\text{FLT}}$ gets asserted and the channel shutdown occurs.
8. If the voltage on UV pin exceeds 633mV threshold as a result of rising Vo, the Power Good ($\overline{\text{PG}}$) output goes active.
9. At the end of the SS interval, the SS cap voltage reaches CPVDD and remains charged as long as $\overline{\text{EN}}$ remains asserted or there is no other fault condition present that would attempt to pull down the gate.

State Diagram

This is shown in Figure 16. It provides a quick overview of the IC operation and can also be used as a troubleshooting road map.

ISL6173

IC Operation State Diagram

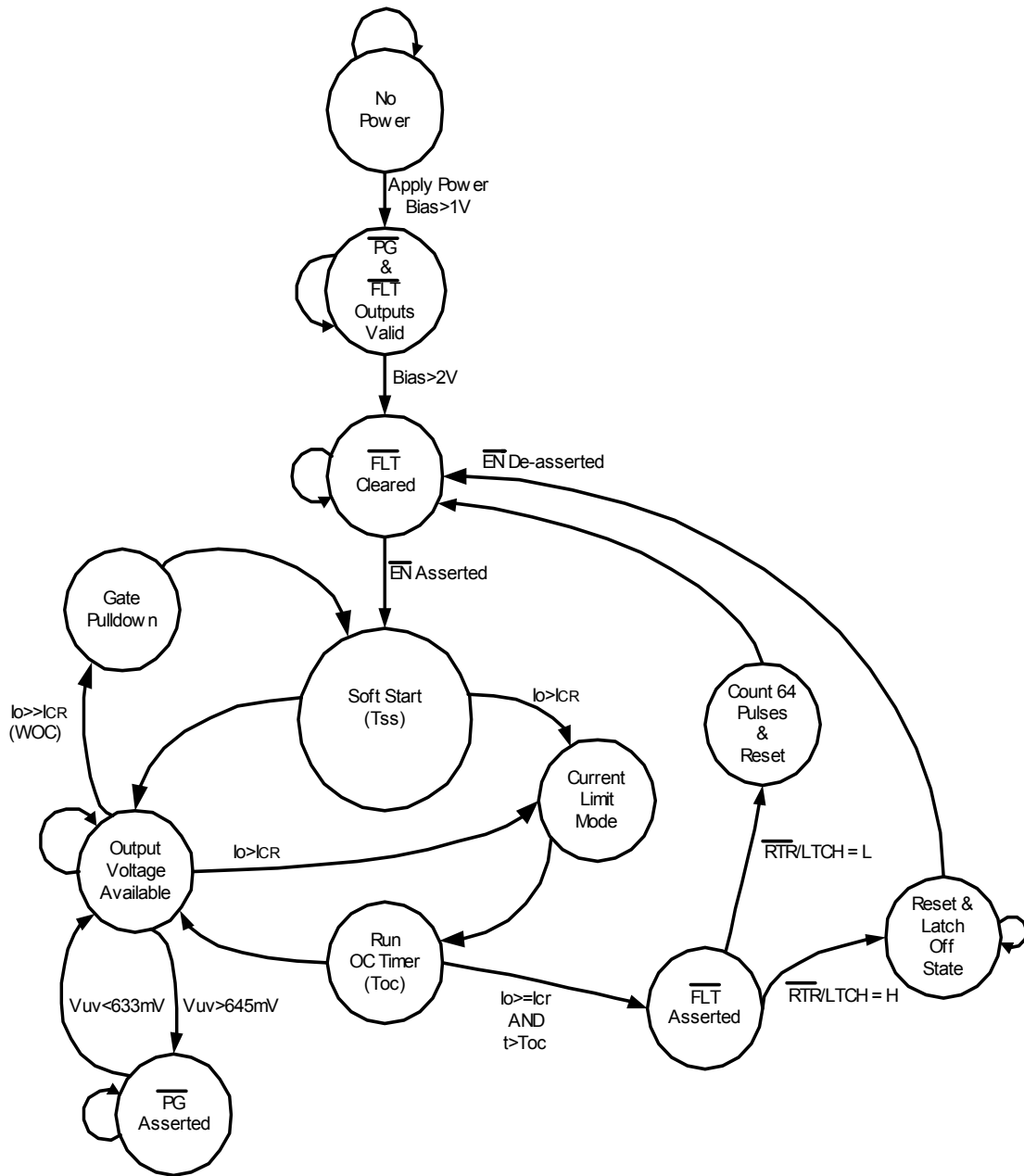


FIGURE 16.

ISL6173

Applications Information

Selection of External Components

The typical application circuit of Figure 2 has been used for this section, which provides guidelines to select the external component values.

MOSFET (Q1)

This component should be selected on the basis of its $r_{DS(ON)}$ specification at the expected V_{gs} (gate to source voltage) and the effective input gate capacitance (C_{iss}). One needs to ensure that the combined voltage drop across the R_{sense} and $r_{DS(ON)}$ at the desired maximum current (including transients) will still keep the output voltage above the minimum required level. Power dissipation in the device under short circuit condition should also be an important consideration especially in auto-retry mode (RTR/LTCH pin pulled low). Using ISL6173 in latched off mode results in lower power dissipation in the MOSFET.

C_{iss} of the MOSFET influences the overcurrent response time. It is recommended that a MOSFET with C_{iss} of less than 10nF be chosen. C_{iss} will also have an impact on the SS cap value selection as seen later.

Current Sense Resistor (R_{SNS})

The voltage drop across this resistor, which represents the load current (I_o), is compared against the set threshold of the current regulation amplifier. The value of this resistor is determined by how much combined voltage drop is tolerable between the source and the load. It is recommended that at least 20mV drop be allowed across this resistor at max load current. This resistor is expected to carry maximum full load current indefinitely. Hence, the power rating of this resistor must be greater than $I_{O(MAX)}^2 \cdot R_{SNS}$.

This resistor is typically a low value resistor and hence the voltage signal appearing across it is also small. In order to maintain high current sense accuracy, current sense trace routing is critical. It is recommended that either a four wire resistor or the following routing method be used:

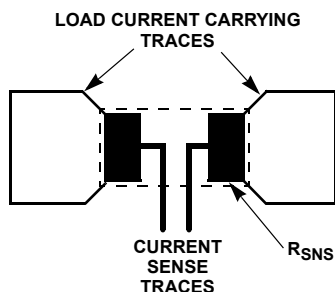


FIGURE 17. RECOMMENDED CURRENT SENSE RESISTOR PCB LAYOUT

Current Set Resistor (R_{SET})

This resistor directly sets the threshold for the current regulation amplifier and indirectly sets the same for the OC and WOC comparators in conjunction with R_{SNS} . Once R_{SNS} has been selected, use Equation 1 (on page 9) to calculate R_{SET} . Use 20 μ A for I_{SET} in a typical application.

Reference Current Set Resistor (R_{REF})

This resistor sets up the current in the internal current source, $I_{REF}/4$, shown in Figure 2 for the comparators. The voltage at the OCREF pin is the same as the internal bandgap reference. The current (I_{REF}) flowing through this resistor is simply:

$$I_{REF} = 1.178/R_{REF}$$

This current, I_{REF} , should be set at 80 μ A to force 20 μ A in the internal current source as shown in Figure 2, because of the 4:1 current mirror. This equates to the resistor value of 14.7K.

Selection of R_{s1} and R_{s2}

These resistors set the UV detect point. The UV comparator detects the undervoltage condition when it sees the voltage at UV pin drop below 0.633V. The resistor divider values should be selected accordingly.

Charge Pump Capacitor Selection (C_P and C_V)

C_P is the "flying cap" and C_V is the smoothing cap of the charge pump, which operates at 450kHz set internally. The output resistance of the charge pump, which affects the regulation, is dependent on the C_P value and its ESR, charge-pump switch resistance, and the frequency and ESR of the smoothing cap, C_V .

It is recommended that C_P be kept within 0.022 μ F (minimum) to 0.1 μ F (maximum) range. Only ceramic capacitors are recommended. Use 0.1 μ F cap if CPVDD output is expected to power an external circuit, in which case the current draw from CPVDD must be kept below 10mA.

C_V should at least be 0.47 μ F (ceramic only). Higher values may be used if low ripple performance is desired.

Time-out Capacitor Selection (C_T)

This capacitor controls the current regulation time-out period. As shown in Figure 2, when the voltage across this capacitor exceeds 1.178V, the time-out comparator detects it and pulls down the gate voltage thus shutting down the channel. An internal 10 μ A current source charges this capacitor. Hence, the value of this capacitor is determined by the following equation:

$$C_T = (10\mu A \cdot T_{OUT})/1.178$$

Where,

T_{OUT} = Desired time-out period.

ISL6173

Soft-Start Capacitor Selection (C_{SS})

The rate of change of voltage (dv/dt) on this capacitor, which is determined by the internal 10 μ A current source, is the same as that on the output load capacitance. Hence, the value of this capacitor directly controls the inrush current amplitude during hot swap operation.

$$C_{SS} = C_O * (10\mu A / I_{INRUSH})$$

Where,

C_O = Load Capacitance

I_{INRUSH} = Desired Inrush Current

I_{INRUSH} is the sum of the dc steady-state load current and the load capacitance charging current. If the dc steady-state load remains disabled until after the soft-start period expires (PGx could be used as a load enable signal, for example), then only the capacitor charging current should be used as I_{INRUSH} . The C_{SS} value should always be more than (1/2.4) of that of C_{ISS} of the MOSFET to ensure proper soft-start operation. This is because the C_{ISS} is charged from 24 μ A current source whereas the C_{SS} gets charged from a 10 μ A current source (please refer to Figure 12). In order to make sure both V_{SS} and V_O track during the soft-start, this condition is necessary.

ISL6173 Evaluation Platform

The **ISL6173EVAL1** is the primary evaluation board for this IC. The board is a standalone evaluation platform and it only needs input bias and test voltages. The schematic for this board is shown in Figures 20 and 21. The component placement diagram is shown in Figure 22.

The evaluation board has been designed with a typical application and accessibility to all the features in mind to enable a user to understand and verify these features of the IC. The circuit is designed for 2A for each input rail but it can easily be scaled up or down by adjusting some component values. LED indicators are provided to indicate Fault and Power Good status. Switches are there to perform Enable function for each channel, to select auto-retry or latching mode and to check WOC and CR modes.

There are two input voltages, one for each channel plus there is "+5V" input. The latter is to test the pull-up capability of \overline{FLT} and \overline{PG} outputs to +5V and also to power the LEDs and the dynamic load circuitry. ISL6173 does not require 5V.

Pins SS1 and SS2 of the IC are available on header J2 as test points so that they can be tied together to achieve tracking between V_{O1} and V_{O2} . Both the Enable (\overline{EN}) switches (SW1 and SW2) must be turned ON to check this function.

Each channel is preloaded with capacitive load. Extra load can be externally applied as required.

The outputs are brought out to banana sockets to allow external loading if desired.

J1 and J3 are wire jumpers. A user can replace them with wire loops to attach a scope current probe. However, doing so may reduce the di/dt enough to prevent WOC comparator from tripping. The internal current regulation amplifier is fast enough to respond to very fast di/dt. Hence, it is advisable to use the on board dynamic load circuitry, as will be described, if a user wants to check the WOC performance.

The dynamic load circuitry, shown in Figure 21, is included on the board on both channels to ensure minimum inductance in the current flow path. Two sets of load are available per output:

- 1) CR Load: This load is set at 1 Ω (approximately 3.3A for 3.3V output), which is higher than the 2.2A of CR limit but less than WOC limit (6.6A) set on the board.
- 2) WOC Load: This load is set at 340m Ω , which is roughly 10A for 3.3V supply. This is higher than 6.6A WOC limit set on the board.

A function/pulse generator is required to activate the dynamic load circuitry. The function/pulse generator should have adjustable pulse-width (3ms), single pulse (manual trigger) and 5V pulse amplitude capability. Agilent model No: 33220A or equivalent is a good choice. The function generator needs to be connected through a co-ax cable to J11 or J12 for channel 1 or channel 2 respectively. WOC or CR load can be activated by turning SW4 or SW5 (channel 1) and SW6 or SW7 (channel 2) ON followed by applying the pulse generator to turn on an appropriate load.

The load circuit consists of a MOSFET driver (EL7202), MOSFET (IRF7821) and surface mount load resistors. The MOSFET drivers, U2 and U3, respond to a pulse from the generator to turn on the MOSFET for the duration of the pulse, which should be set less than the timeout period described in "Time-out Capacitor Selection". On this board the timeout capacitor value is 0.15 μ F, which corresponds to a timeout period of 17.67ms.

One way to tell if the WOC mode is active would be by looking at the Gate waveform of the control MOSFET (M1 or M2). The WOC comparator when tripped, pulls down the Gate hard. The following waveform shows WOC operation:

ISL6173

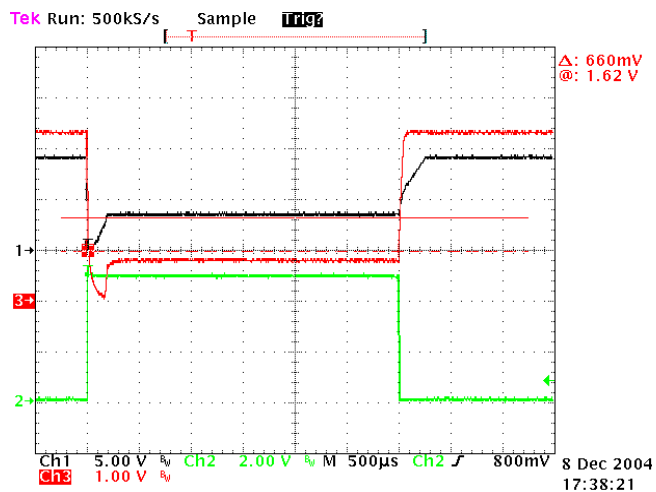


FIGURE 18. WOC OPERATION

Channel 1 is Vgate, Channel 2 is the pulse generator output and Channel 3 is Vout. Note how Vgate gets immediately pulled down to zero volts up on load application.

In CR mode, however, Vgate always remains above zero volts because WOC comparator never trips. This can be seen on the following scope shot:

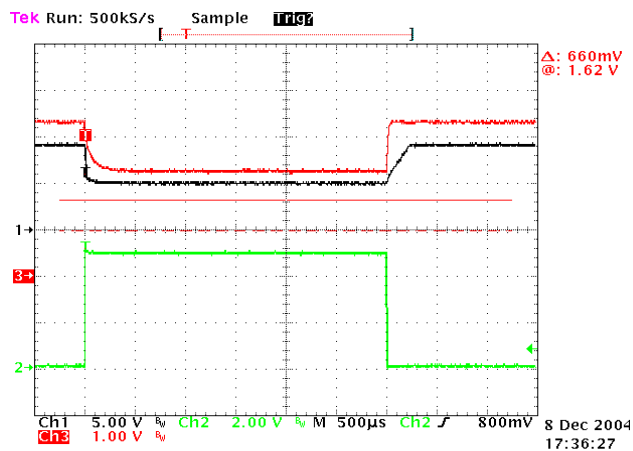


FIGURE 19. CURRENT REGULATION OPERATION

It is also important to note that in WOC mode, although Vgate gets pulled down to zero initially, the gate is quickly released and slowly rises until the CR amplifier takes control.

ISL6173

Bill of Materials for ISL6173 Eval 1 Board

| ITEM | QTY | REFERENCE | PART | PKG | MFG P/N | MANUFACTURER |
|------|-----|--|---------------|-----------|--------------------|-------------------------|
| 1 | 2 | C1, C18 | 220 μ F | Leaded | UPM1E221MPH6 or eq | Nichicon |
| 2 | 2 | C2, C17 | 47 μ F | Leaded | UPM1E470MEH or eq | Nichicon |
| 3 | 2 | C3, C4 | 0.1 μ F | 0805 | | Any |
| 4 | 2 | C5, C6 | 1000pF | 0805 | | Any |
| 5 | 2 | C9, C10 | 0.033 μ F | 0805 | | Any |
| 6 | 2 | C11, C12 | 0.15 μ F | 0805 | | Any |
| 7 | 1 | C13 | 0.47 μ F | 0805 | | Any |
| 8 | 1 | C14 | 2.2 μ F | 1206 | | Any |
| 9 | 2 | C19, C20 | 0.01 μ F | 0805 | | Any |
| 10 | 1 | C21 | 10 μ F | 7343 | | Any |
| 11 | 1 | C22 | 0.022 μ F | 0805 | | Any |
| 12 | 2 | D1, D6 | MBR130P | SMA | MBR130P | ON Semi |
| 13 | 2 | D3, D4 | LED GRN | 1206 | PG1101W | Stanley |
| 14 | 2 | D2, D5 | LED RED | 1206 | BR1101W | Stanley |
| 15 | 1 | J2 | 2 Pin Header | | | Any |
| 16 | 2 | J1, J3 | Jumper | | | Any |
| 17 | 2 | J11, J12 | BNC Jack | | | |
| 18 | 6 | M1, M2, M3, M4, M5, M6 | IRF7821 | SO8 | IRF7821 | International Rectifier |
| 19 | 10 | RS1, RS2, R10, R12, R30, R31 R55, R56, R57, R58 | 1K | 0805 | | Any |
| 20 | 6 | R1, R27, R49, R50, R51, R52 | 0.01 | 2512 | | Any |
| 21 | 4 | R2, R3, R25, R26 | 390 | 0805 | | Any |
| 22 | 1 | R8 | 3.57K | 0805 | | Any |
| 23 | 1 | R9 | 2.55K | 0805 | | Any |
| 24 | 1 | R11 | 14.7K | 0805 | | Any |
| 25 | 3 | R14, R15, R20 | 0 | 0805 | | Any |
| 26 | 4 | R16, R17, R18, R19 | 10K | 0805 | | Any |
| 27 | 2 | R29, R32 | 1.1K | 0805 | | Any |
| 28 | 4 | R33, R34, R35, R36 | 10 | 0805 | | Any |
| 29 | 6 | R37, R38, R42, R43, R44, R45 | 1 | 2512 | | Any |
| 30 | 10 | R39, R40, R41, R46, R47, R48 R61, R62, R63, R64 | 5 | 2512 | | Any |
| 31 | 2 | R53, R54 | 100 | 1206 | | Any |
| 32 | 2 | R59, R60 | 49.9 | 0805 | | Any |
| 34 | 1 | U1 | ISL6173 | QFN28 5x5 | ISL6172 | Intersil |
| 35 | 2 | U2, U3 | EL7202/SO | SO8 | | Intersil |
| 38 | 7 | SW5, SW6, SW7, SW8, SW9, SW10, SW11 | Toggle Switch | | GT11MCKE | C & K |

Schematic, ISL6173 Eval1

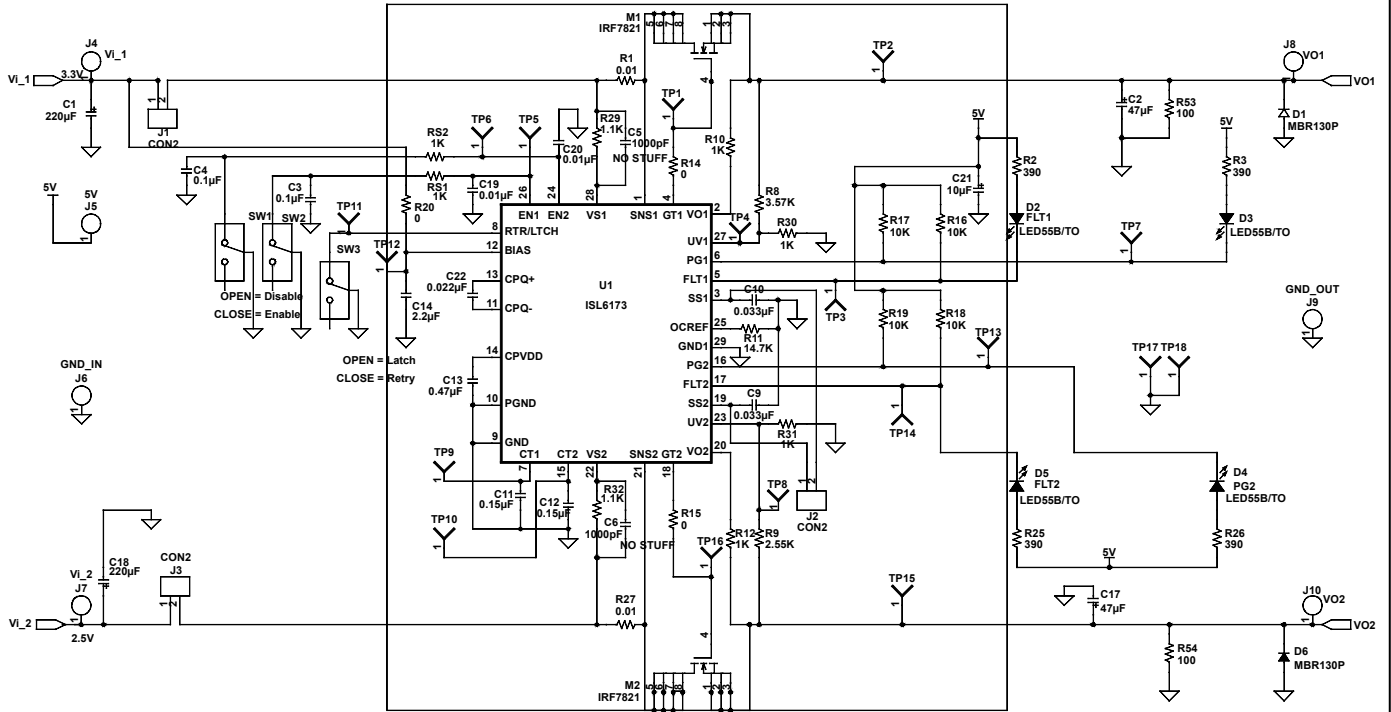


FIGURE 20.

Schematic, ISL6173 Eval1 (Continued)

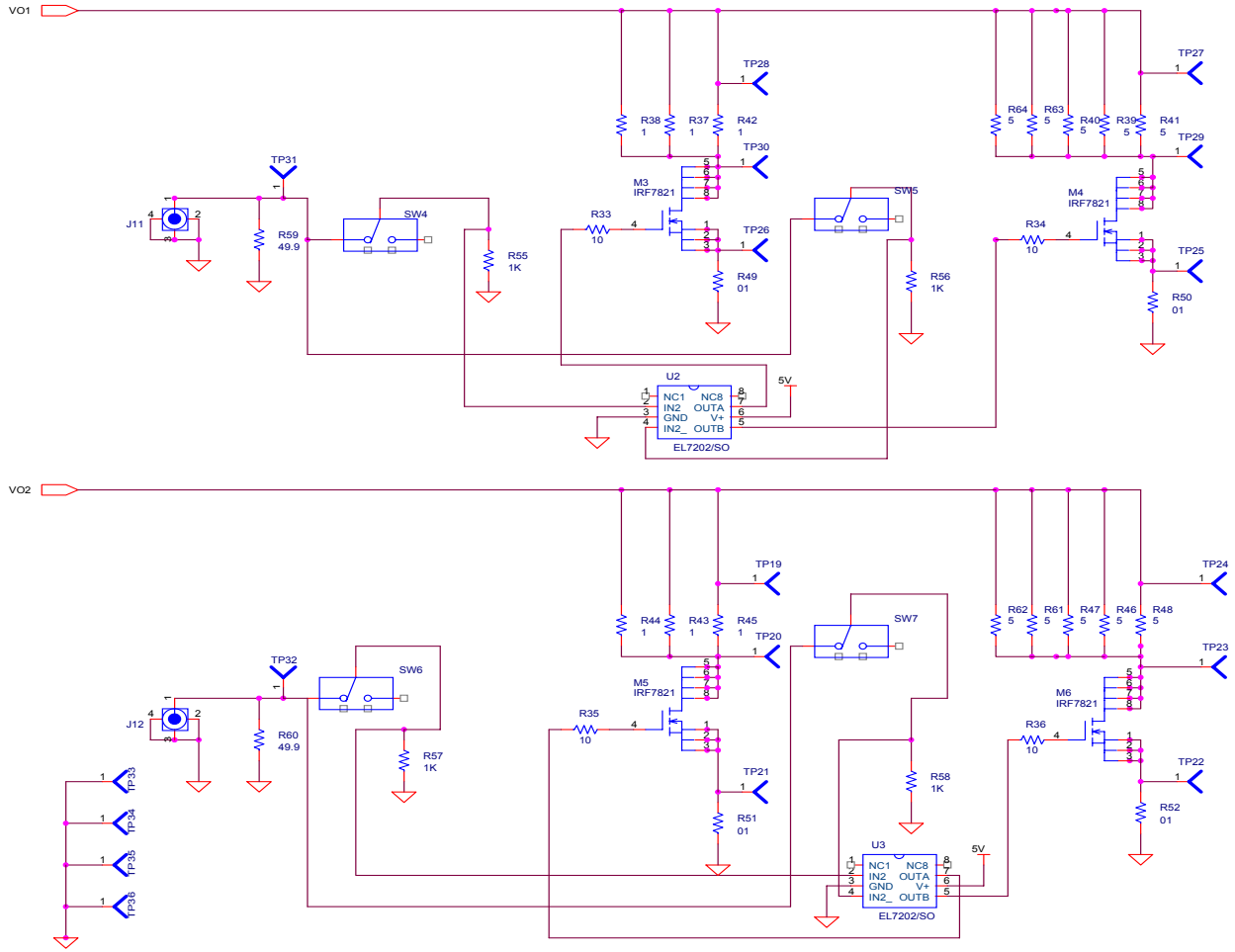


FIGURE 21.

ISL6173 Eval 1 - Component Layout

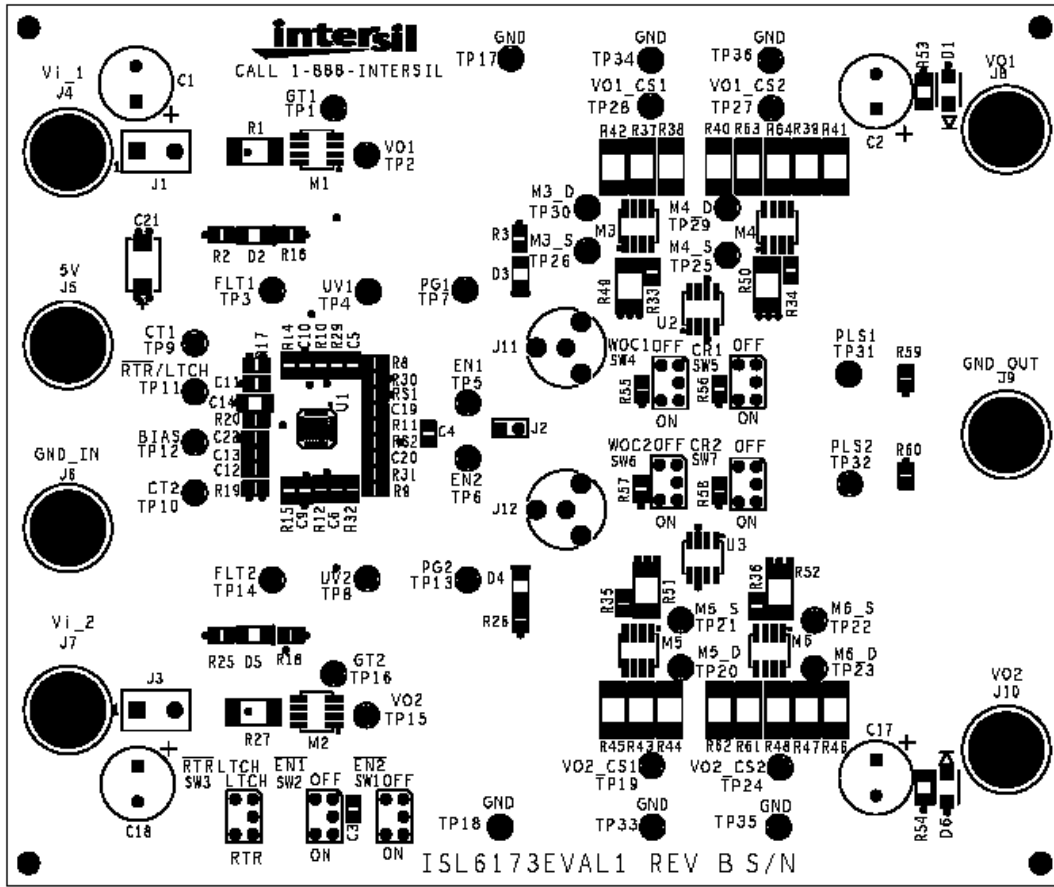
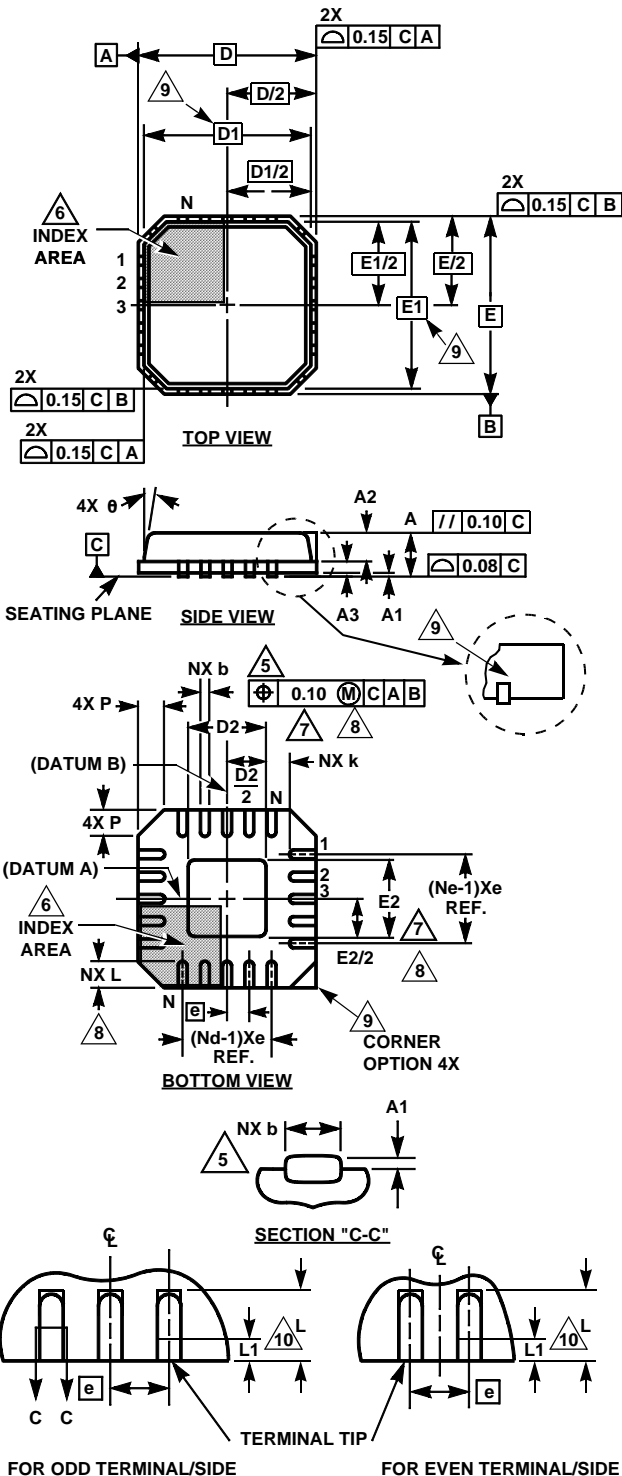


FIGURE 22.

ISL6173

**Quad Flat No-Lead Package (QFN)
 Micro Lead Frame Plastic Package (MLFP)**

**L28.5x5
 28 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
 (COMPLIANT TO JEDEC MO-220VHHD-1 ISSUE I)**



| SYMBOL | MILLIMETERS | | | NOTES |
|--------|-------------|---------|------|-------|
| | MIN | NOMINAL | MAX | |
| A | 0.80 | 0.90 | 1.00 | - |
| A1 | - | 0.02 | 0.05 | - |
| A2 | - | 0.65 | 1.00 | 9 |
| A3 | 0.20 REF | | | 9 |
| b | 0.18 | 0.25 | 0.30 | 5,8 |
| D | 5.00 BSC | | | - |
| D1 | 4.75 BSC | | | 9 |
| D2 | 2.95 | 3.10 | 3.25 | 7,8 |
| E | 5.00 BSC | | | - |
| E1 | 4.75 BSC | | | 9 |
| E2 | 2.95 | 3.10 | 3.25 | 7,8 |
| e | 0.50 BSC | | | - |
| k | 0.20 | - | - | - |
| L | 0.50 | 0.60 | 0.75 | 8 |
| N | 28 | | | 2 |
| Nd | 7 | | | 3 |
| Ne | 7 | | | 3 |
| P | - | - | 0.60 | 9 |
| θ | - | - | 12 | 9 |

Rev. 1 11/04

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.

FOR ODD TERMINAL/SIDE

FOR EVEN TERMINAL/SIDE

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems.

Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com