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MUN5334DW1, NSBC124XPDXV6

Complementary Bias Resistor Transistors R1 = 22 kΩ, R2 = 47 kΩ

NPN and PNP Transistors with Monolithic Bias Resistor Network

This series of digital transistors is designed to replace a single device and its external resistor bias network. The Bias Resistor Transistor (BRT) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. The BRT eliminates these individual components by integrating them into a single device. The use of a BRT can reduce both system cost and board space.

Features

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- S and NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable*
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS

(T_A = 25°C both polarities Q₁ (PNP) & Q₂ (NPN), unless otherwise noted)

Rating	Symbol	Max	Unit
Collector-Base Voltage	V _{CBO}	50	Vdc
Collector-Emitter Voltage	V _{CEO}	50	Vdc
Collector Current – Continuous	I _C	100	mAdc
Input Forward Voltage	V _{IN(fwd)}	40	Vdc
Input Reverse Voltage	V _{IN(rev)}	7	Vdc

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ORDERING INFORMATION

Device	Package	Shipping†
MUN5334DW1T1G, NSVMUN5334DW1T1G*	SOT-363	3,000/Tape & Reel
NSBC124XPDXV6T1G, NSVBC124XPDXV6T1G*	SOT-563	4,000/Tape & Reel

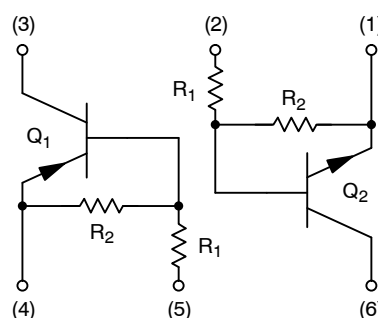
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



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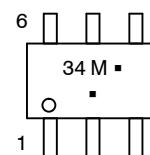
PIN CONNECTIONS



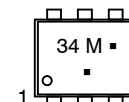
MARKING DIAGRAMS



SOT-363
CASE 419B



SOT-563
CASE 463A



34 = Specific Device Code
 M = Date Code*
 ■ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation may vary depending upon manufacturing location.

MUN5334DW1, NSBC124XPDXV6

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
MUN5334DW1 (SOT-363) ONE JUNCTION HEATED			
Total Device Dissipation $T_A = 25^\circ\text{C}$ (Note 1) (Note 2)	P_D	187	mW
Derate above 25°C (Note 1) (Note 2)		256	mW/ $^\circ\text{C}$
		1.5	
		2.0	
Thermal Resistance, Junction to Ambient (Note 1) (Note 2)	$R_{\theta JA}$	670	$^\circ\text{C}/\text{W}$
		490	
MUN5334DW1 (SOT-363) BOTH JUNCTION HEATED (Note 3)			
Total Device Dissipation $T_A = 25^\circ\text{C}$ (Note 1) (Note 2)	P_D	250	mW
Derate above 25°C (Note 1) (Note 2)		385	mW/ $^\circ\text{C}$
		2.0	
		3.0	
Thermal Resistance, Junction to Ambient (Note 1) (Note 2)	$R_{\theta JA}$	493	$^\circ\text{C}/\text{W}$
		325	
Thermal Resistance, Junction to Lead (Note 1) (Note 2)	$R_{\theta JL}$	188	$^\circ\text{C}/\text{W}$
		208	
Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$
NSBC124XPDXV6 (SOT-563) ONE JUNCTION HEATED			
Total Device Dissipation $T_A = 25^\circ\text{C}$ (Note 1) (Note 1)	P_D	357	mW
Derate above 25°C (Note 1)		2.9	mW/ $^\circ\text{C}$
Thermal Resistance, Junction to Ambient (Note 1)	$R_{\theta JA}$	350	$^\circ\text{C}/\text{W}$
NSBC124XPDXV6 (SOT-563) BOTH JUNCTION HEATED (Note 3)			
Total Device Dissipation $T_A = 25^\circ\text{C}$ (Note 1) (Note 1)	P_D	500	mW
Derate above 25°C (Note 1)		4.0	mW/ $^\circ\text{C}$
Thermal Resistance, Junction to Ambient (Note 1)	$R_{\theta JA}$	250	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

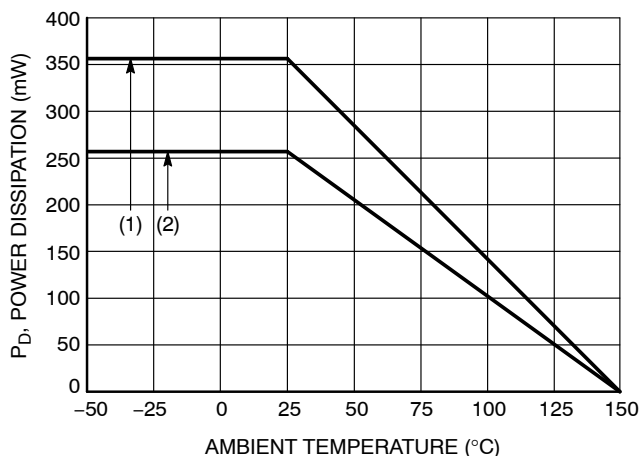
- FR-4 @ Minimum Pad.
- FR-4 @ 1.0×1.0 Inch Pad.
- Both junction heated values assume total power is sum of two equally powered channels.

MUN5334DW1, NSBC124XPDXV6

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ both polarities Q_1 (PNP) & Q_2 (NPN), unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Base Cutoff Current ($V_{CB} = 50\text{ V}, I_E = 0$)	I_{CBO}	-	-	100	nA _{dc}
Collector-Emitter Cutoff Current ($V_{CE} = 50\text{ V}, I_B = 0$)	I_{CEO}	-	-	500	nA _{dc}
Emitter-Base Cutoff Current ($V_{EB} = 6.0\text{ V}, I_C = 0$)	I_{EBO}	-	-	0.13	mA _{dc}
Collector-Base Breakdown Voltage ($I_C = 10\ \mu\text{A}, I_E = 0$)	$V_{(BR)CBO}$	50	-	-	V _{dc}
Collector-Emitter Breakdown Voltage (Note 4) ($I_C = 2.0\text{ mA}, I_B = 0$)	$V_{(BR)CEO}$	50	-	-	V _{dc}
ON CHARACTERISTICS					
DC Current Gain (Note 4) ($I_C = 5.0\text{ mA}, V_{CE} = 10\text{ V}$)	h_{FE}	80	150	-	
Collector-Emitter Saturation Voltage (Note 4) ($I_C = 10\text{ mA}, I_B = 1.0\text{ mA}$)	$V_{CE(sat)}$	-	-	0.25	V
Input Voltage (Off) ($V_{CE} = 5.0\text{ V}, I_C = 100\ \mu\text{A}$) (NPN) ($V_{CE} = 5.0\text{ V}, I_C = 100\ \mu\text{A}$) (PNP)	$V_{i(off)}$	-	0.8 0.9	-	V _{dc}
Input Voltage (On) ($V_{CE} = 0.2\text{ V}, I_C = 3.0\text{ mA}$) (NPN) ($V_{CE} = 0.2\text{ V}, I_C = 3.0\text{ mA}$) (PNP)	$V_{i(on)}$	-	1.3 1.3	-	V _{dc}
Output Voltage (On) ($V_{CC} = 5.0\text{ V}, V_B = 2.5\text{ V}, R_L = 1.0\text{ k}\Omega$)	V_{OL}	-	-	0.2	V _{dc}
Output Voltage (Off) ($V_{CC} = 5.0\text{ V}, V_B = 0.5\text{ V}, R_L = 1.0\text{ k}\Omega$)	V_{OH}	4.9	-	-	V _{dc}
Input Resistor	R1	15.4	22	28.6	k Ω
Resistor Ratio	R_1/R_2	0.38	0.47	0.56	

4. Pulsed Condition: Pulse Width = 300 ms, Duty Cycle \leq 2%.



(1) SOT-363; 1.0 x 1.0 Inch Pad
(2) SOT-563; Minimum Pad

Figure 1. Derating Curve

MUN5334DW1, NSBC124XPDXV6

**TYPICAL CHARACTERISTICS – NPN TRANSISTOR
 MUN5334DW1, NSBC124XPDXV6**

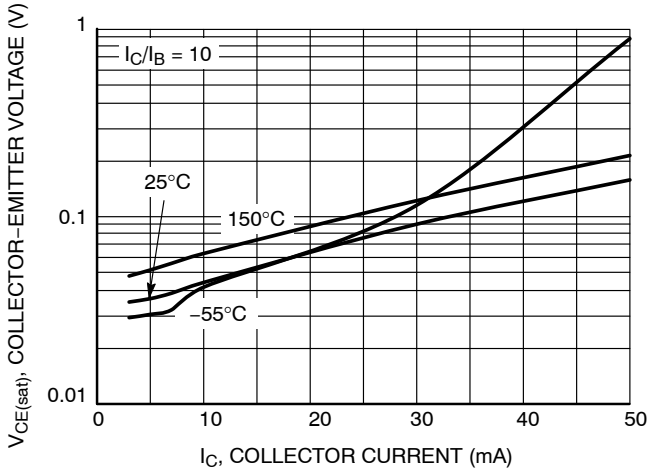


Figure 2. $V_{CE(sat)}$ vs. I_C

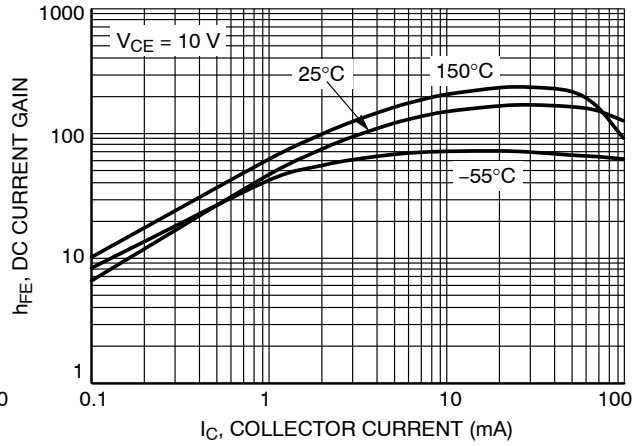


Figure 3. DC Current Gain

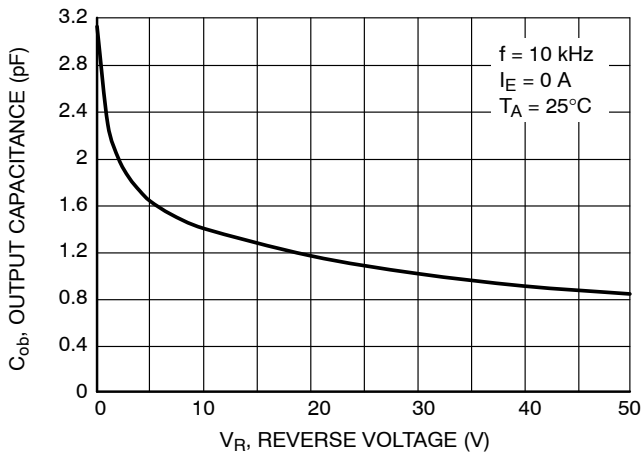


Figure 4. Output Capacitance

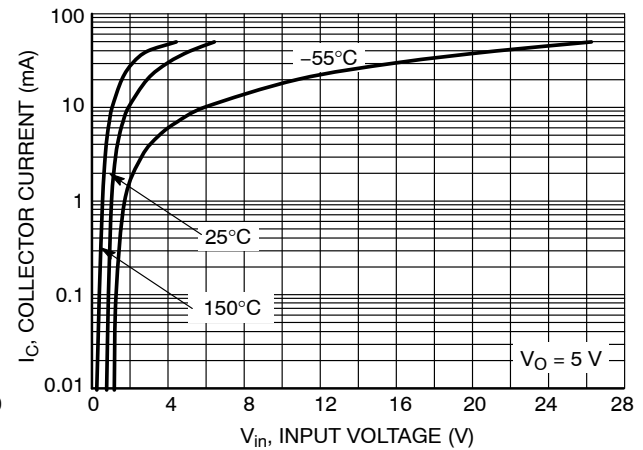


Figure 5. Output Current vs. Input Voltage

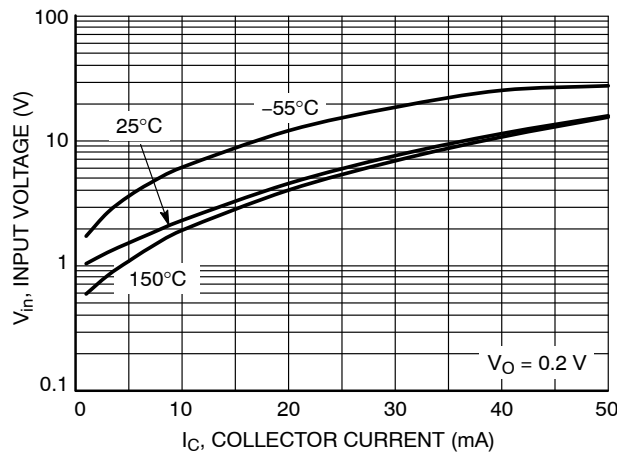


Figure 6. Input Voltage vs. Output Current

MUN5334DW1, NSBC124XPDXV6

**TYPICAL CHARACTERISTICS – PNP TRANSISTOR
 MUN5334DW1, NSBC124XPDXV6**

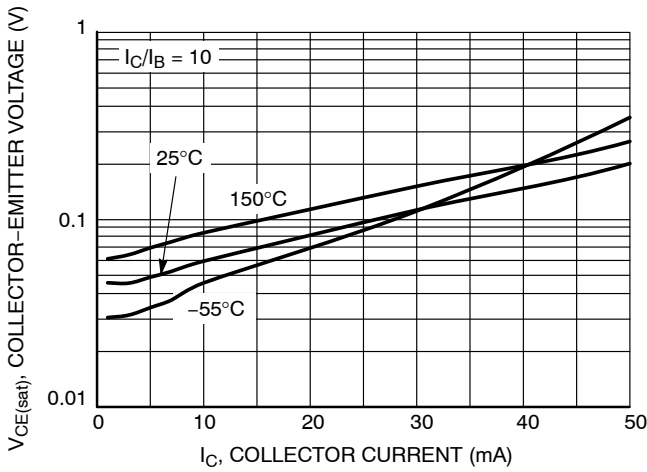


Figure 7. $V_{CE(sat)}$ vs. I_C

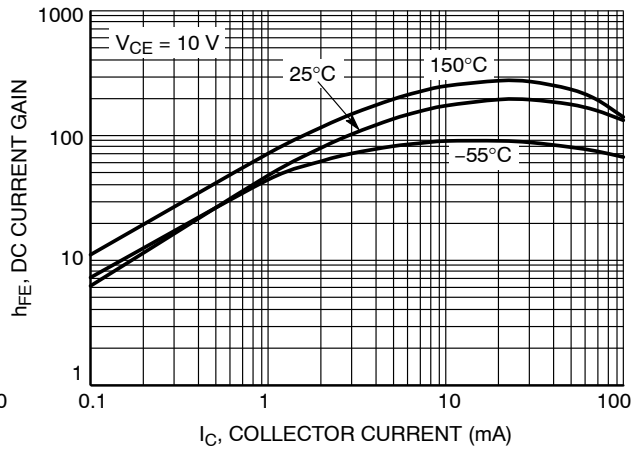


Figure 8. DC Current Gain

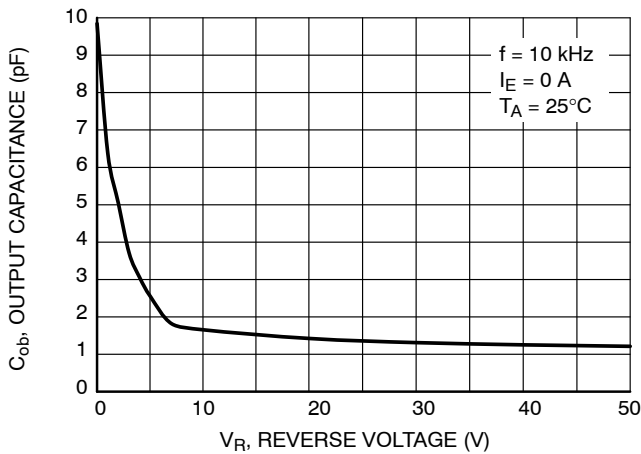


Figure 9. Output Capacitance

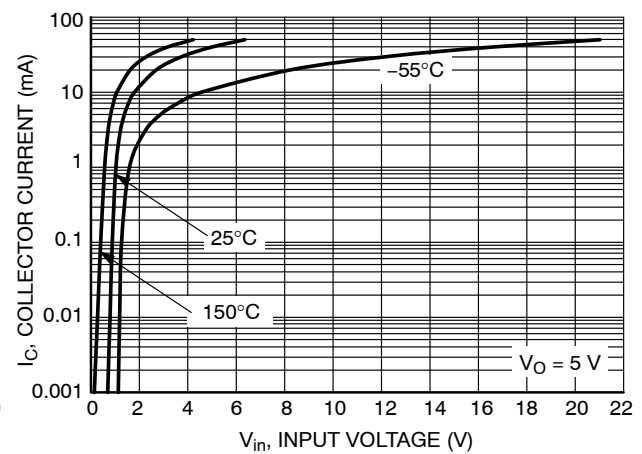


Figure 10. Output Current vs. Input Voltage

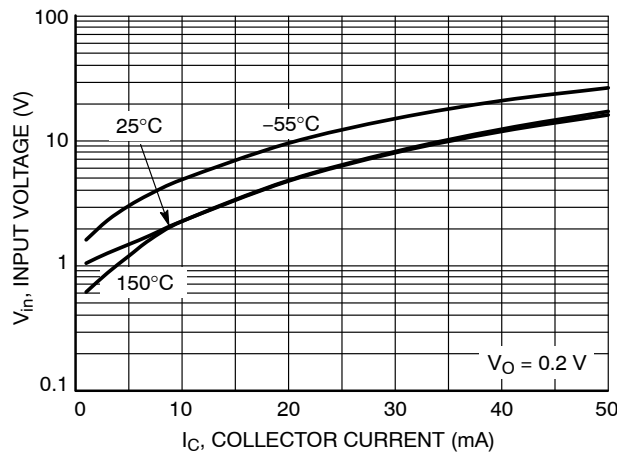
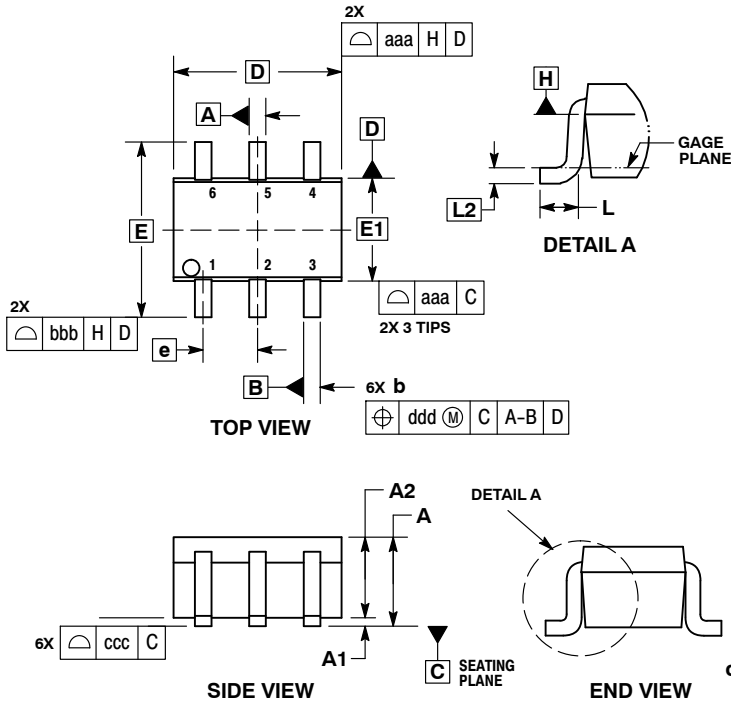


Figure 11. Input Voltage vs. Output Current

MUN5334DW1, NSBC124XPDXV6

PACKAGE DIMENSIONS

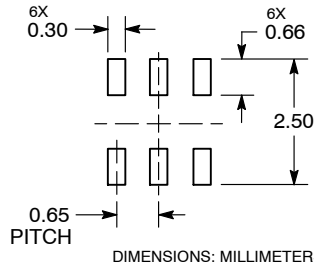
SC-88/SC70-6/SOT-363
 CASE 419B-02
 ISSUE Y



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
 4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
 5. DATUMS A AND B ARE DETERMINED AT DATUM H.
 6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
 7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.10	---	---	0.043
A1	0.00	---	0.10	0.000	---	0.004
A2	0.70	0.90	1.00	0.027	0.035	0.039
b	0.15	0.20	0.25	0.006	0.008	0.010
C	0.08	0.15	0.22	0.003	0.006	0.009
D	1.80	2.00	2.20	0.070	0.078	0.086
E	2.00	2.10	2.20	0.078	0.082	0.086
E1	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65 BSC			0.026 BSC		
L	0.26	0.36	0.46	0.010	0.014	0.018
L2	0.15 BSC			0.006 BSC		
aaa	0.15			0.006		
bbb	0.30			0.012		
ccc	0.10			0.004		
ddd	0.10			0.004		

RECOMMENDED SOLDERING FOOTPRINT*

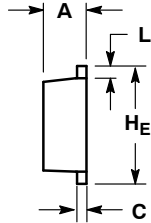
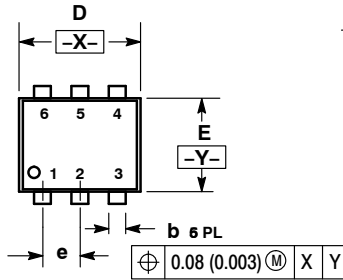


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MUN5334DW1, NSBC124XPDXV6

PACKAGE DIMENSIONS

SOT-563, 6 LEAD
 CASE 463A
 ISSUE G

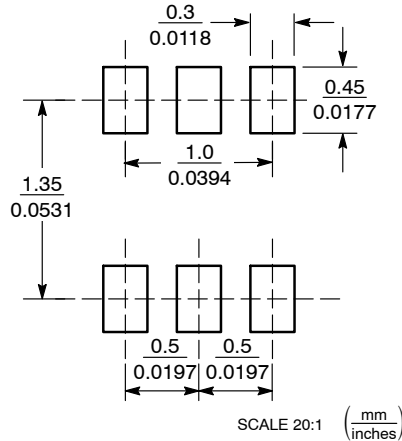


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.020	0.021	0.023
b	0.17	0.22	0.27	0.007	0.009	0.011
C	0.08	0.12	0.18	0.003	0.005	0.007
D	1.50	1.60	1.70	0.059	0.062	0.066
E	1.10	1.20	1.30	0.043	0.047	0.051
e	0.5 BSC			0.02 BSC		
L	0.10	0.20	0.30	0.004	0.008	0.012
HE	1.50	1.60	1.70	0.059	0.062	0.066

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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