

Excellent Integrated System Limited

Stocking Distributor

Click to view price, real time Inventory, Delivery & Lifecycle Information:

[ON Semiconductor](#)
[NTMS4N01R2G](#)

For any questions, you can email us directly:

sales@integrated-circuit.com

NTMS4N01R2

Power MOSFET 4.2 Amps, 20 Volts N-Channel Enhancement-Mode Single SO-8 Package

Features

- High Density Power MOSFET with Ultra Low $R_{DS(on)}$ Providing Higher Efficiency
- Miniature SO-8 Surface Mount Package Saving Board Space; Mounting Information for the SO-8 Package is Provided
- I_{DSS} Specified at Elevated Temperature
- Drain-to-Source Avalanche Energy Specified
- Diode Exhibits High Speed, Soft Recovery
- Pb-Free Package is Available

Applications

- Power Management in Portable and Battery-Powered Products, i.e.: Computers, Printers, PCMCIA Cards, Cellular & Cordless Telephones

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	20	V
Drain-to-Gate Voltage ($R_{GS} = 1.0\text{ m}\Omega$)	V_{DGR}	20	V
Gate-to-Source Voltage - Continuous	V_{GS}	± 10	V
Thermal Resistance, Junction-to-Ambient (Note 1)	$R_{\theta JA}$	50	$^\circ\text{C/W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	2.5	W
Continuous Drain Current @ 25°C	I_D	5.9	A
Continuous Drain Current @ 70°C	I_D	4.7	A
Pulsed Drain Current (Note 4)	I_{DM}	25	A
Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	100	$^\circ\text{C/W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	1.25	W
Continuous Drain Current @ 25°C	I_D	4.2	A
Continuous Drain Current @ 70°C	I_D	3.3	A
Pulsed Drain Current (Note 4)	I_{DM}	20	A
Thermal Resistance, Junction-to-Ambient (Note 3)	$R_{\theta JA}$	162	$^\circ\text{C/W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	0.77	W
Continuous Drain Current @ 25°C	I_D	3.3	A
Continuous Drain Current @ 70°C	I_D	2.6	A
Pulsed Drain Current (Note 4)	I_{DM}	15	A
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to $+150$	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy - Starting $T_J = 25^\circ\text{C}$ ($V_{DD} = 20\text{ Vdc}$, $V_{GS} = 5.0\text{ Vdc}$, Peak $I_L = 7.5\text{ Apk}$, $L = 6\text{ mH}$, $R_G = 25\ \Omega$)	E_{AS}	169	mJ
Maximum Lead Temperature for Soldering Purposes, $1/8''$ from case for 10 seconds	T_L	260	$^\circ\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Mounted onto a 2" square FR-4 Board (1" sq. 2 oz Cu 0.06" thick single sided), $t \leq 10$ seconds.
2. Mounted onto a 2" square FR-4 Board (1" sq. 2 oz Cu 0.06" thick single sided), $t =$ steady state.
3. Minimum FR-4 or G-10 PCB, $t =$ Steady State.
4. Pulse Test: Pulse Width = 300 μs , Duty Cycle = 2%.

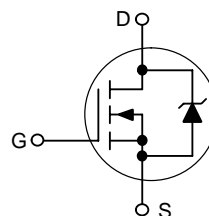


ON Semiconductor®

<http://onsemi.com>

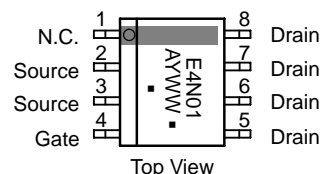
4.2 AMPERES, 20 VOLTS
0.045 Ω @ $V_{GS} = 4.5\text{ V}$

Single N-Channel



SO-8
 CASE 751
 STYLE 13

MARKING DIAGRAM AND PIN ASSIGNMENT



E4N01 = Device Code
 A = Assembly Location
 Y = Year
 WW = Work Week
 ■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NTMS4N01R2	SO-8	2500 / Tape & Reel
NTMS4N01R2G	SO-8 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NTMS4N01R2

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted) (Note 5)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-to-Source Breakdown Voltage ($V_{GS} = 0\text{ Vdc}$, $I_D = 250\ \mu\text{Adc}$)	$V_{(BR)DSS}$	20	-	-	Vdc
Temperature Coefficient (Positive)		-	20	-	$\text{mV}/^\circ\text{C}$
Zero Gate Voltage Drain Current ($V_{DS} = 12\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$, $T_J = 25^\circ\text{C}$) ($V_{DS} = 12\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$, $T_J = 125^\circ\text{C}$) ($V_{DS} = 20\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$, $T_J = 25^\circ\text{C}$)	I_{DSS}	-	-	1.0 10 -	μAdc
Gate-Body Leakage Current ($V_{GS} = +10\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	-	-	100	nAdc
Gate-Body Leakage Current ($V_{GS} = -10\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	-	-	-100	nAdc

ON CHARACTERISTICS

Gate Threshold Voltage ($V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{Adc}$)	$V_{GS(th)}$	0.6	0.95	1.2	Vdc
Temperature Coefficient (Negative)		-	-3.0	-	$\text{mV}/^\circ\text{C}$
Static Drain-to-Source On-State Resistance ($V_{GS} = 4.5\text{ Vdc}$, $I_D = 4.2\text{ Adc}$) ($V_{GS} = 2.7\text{ Vdc}$, $I_D = 2.1\text{ Adc}$) ($V_{GS} = 2.5\text{ Vdc}$, $I_D = 2.0\text{ Adc}$)	$R_{DS(on)}$	-	0.030 0.035 0.037	0.04 0.05 -	Ω
Forward Transconductance ($V_{DS} = 2.5\text{ Vdc}$, $I_D = 2.0\text{ Adc}$)	g_{FS}	-	10	-	Mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	$(V_{DS} = 10\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$, $f = 1.0\text{ MHz}$)	C_{iss}	-	870	1200	pF
Output Capacitance		C_{oss}	-	260	400	
Reverse Transfer Capacitance		C_{rss}	-	60	100	

SWITCHING CHARACTERISTICS (Notes 6 & 7)

Turn-On Delay Time	$(V_{DD} = 12\text{ Vdc}$, $I_D = 4.2\text{ Adc}$, $V_{GS} = 4.5\text{ Vdc}$, $R_G = 2.3\ \Omega$)	$t_{d(on)}$	-	13	25	ns
Rise Time		t_r	-	35	65	
Turn-Off Delay Time		$t_{d(off)}$	-	45	75	
Fall Time		t_f	-	50	90	
Total Gate Charge	$(V_{DS} = 12\text{ Vdc}$, $V_{GS} = 4.5\text{ Vdc}$, $I_D = 4.2\text{ Adc}$)	Q_{tot}	-	11	16	nC
Gate-Source Charge		Q_{gs}	-	2.0	-	
Gate-Drain Charge		Q_{gd}	-	3.0	-	

BODY-DRAIN DIODE RATINGS (Note 6)

Diode Forward On-Voltage ($I_S = 4.2\text{ Adc}$, $V_{GS} = 0\text{ Vdc}$) ($I_S = 4.2\text{ Adc}$, $V_{GS} = 0\text{ Vdc}$, $T_J = 125^\circ\text{C}$)	V_{SD}	-	0.85 0.70	1.1 -	Vdc
Reverse Recovery Time ($I_S = 4.2\text{ Adc}$, $V_{GS} = 0\text{ Vdc}$, $di_S/dt = 100\text{ A}/\mu\text{s}$)	t_{rr}	-	20	-	ns
	t_a	-	12	-	
	t_b	-	8.0	-	
Reverse Recovery Stored Charge	Q_{RR}	-	0.01	-	μC

5. Handling precautions to protect against electrostatic discharge is mandatory.

 6. Indicates Pulse Test: Pulse Width = 300 μs max, Duty Cycle = 2%.

7. Switching characteristics are independent of operating junction temperature.

NTMS4N01R2

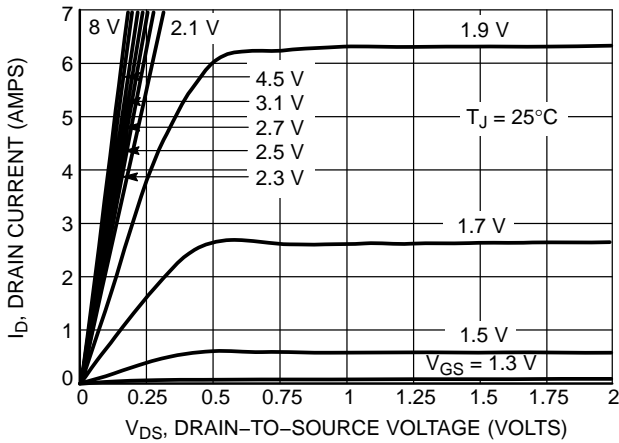


Figure 1. On-Region Characteristics

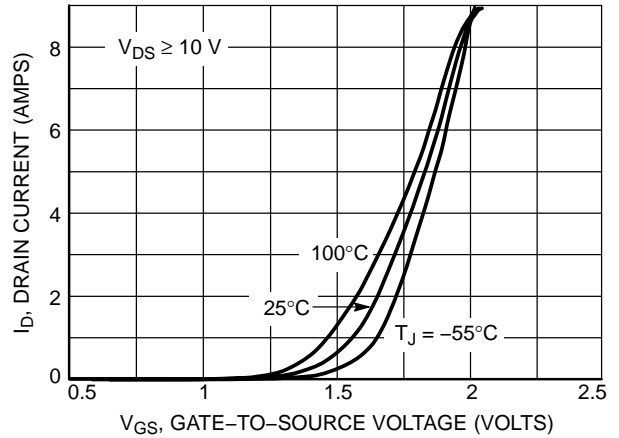


Figure 2. Transfer Characteristics

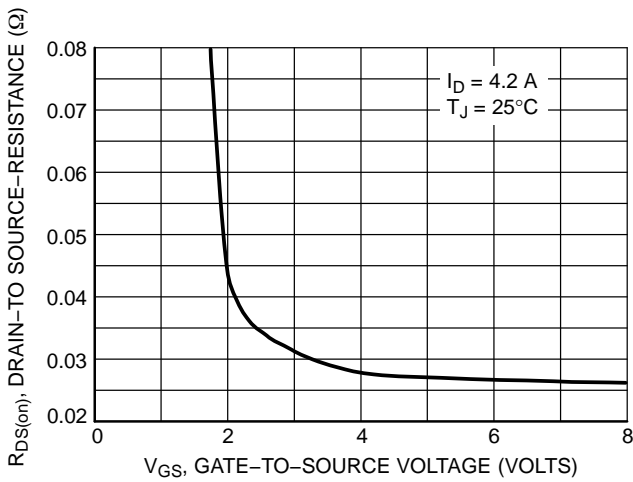


Figure 3. On-Resistance versus Gate-to-Source Voltage

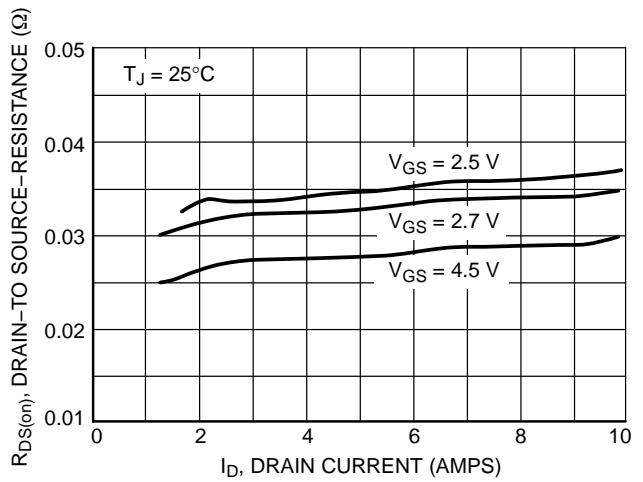


Figure 4. On-Resistance versus Drain Current and Gate Voltage

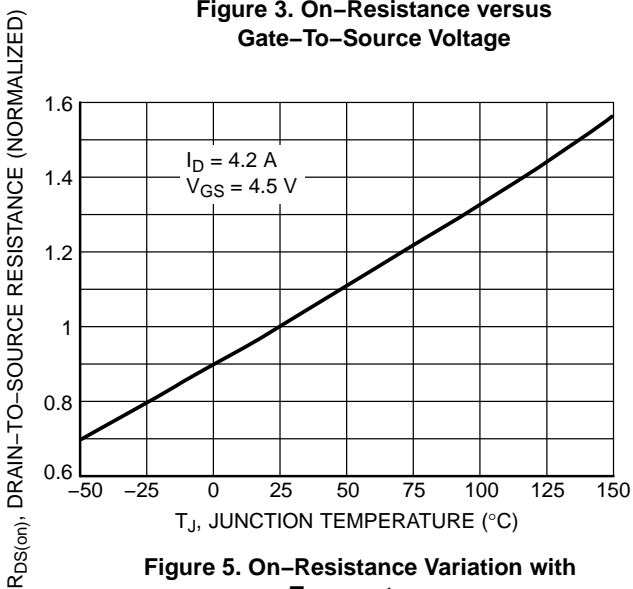


Figure 5. On-Resistance Variation with Temperature

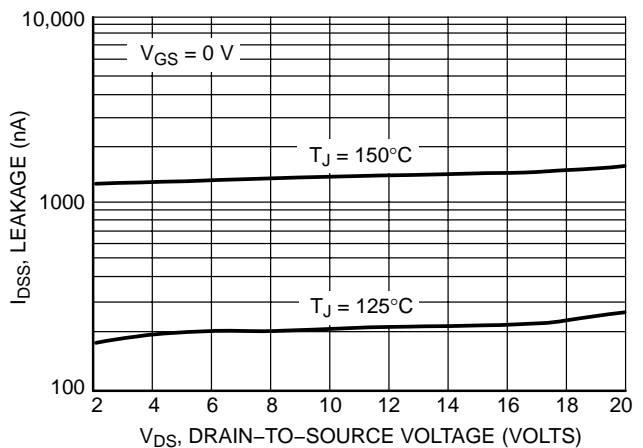


Figure 6. Drain-to-Source Leakage Current versus Voltage

NTMS4N01R2

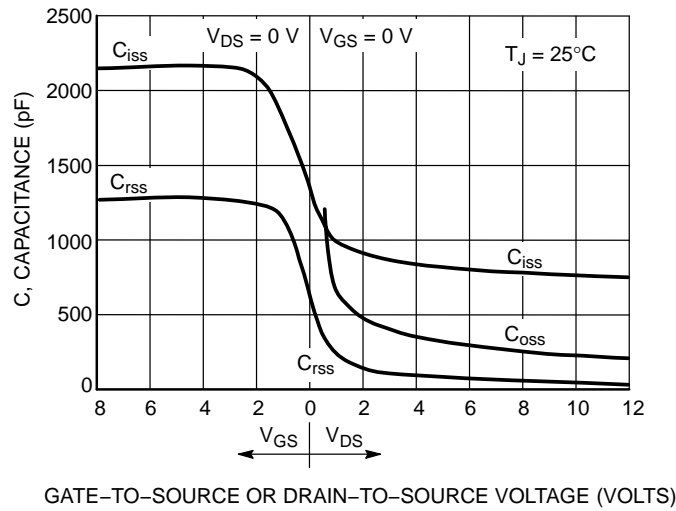


Figure 7. Capacitance Variation

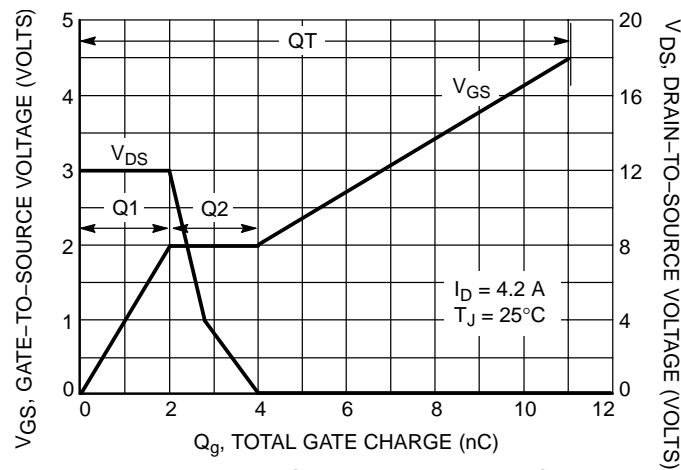


Figure 8. Gate-To-Source and Drain-To-Source Voltage versus Total Charge

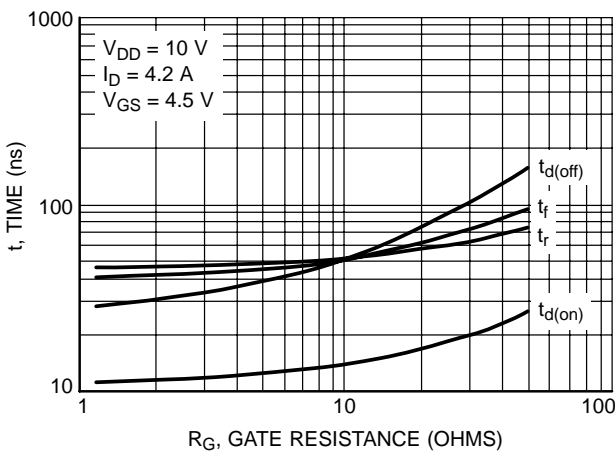


Figure 9. Resistive Switching Time Variation versus Gate Resistance

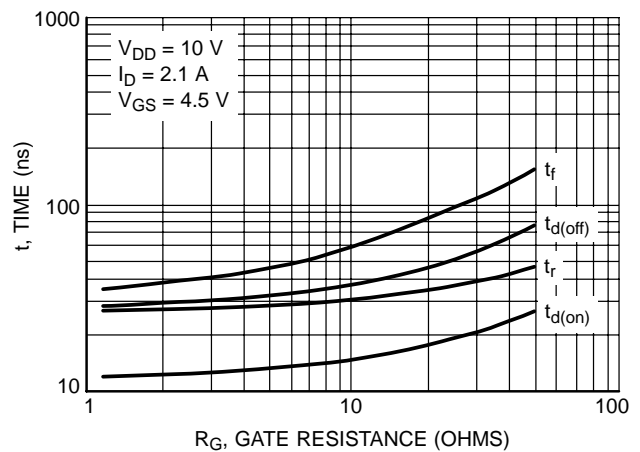


Figure 10. Resistive Switching Time Variation versus Gate Resistance

NTMS4N01R2

DRAIN-TO-SOURCE DIODE CHARACTERISTICS

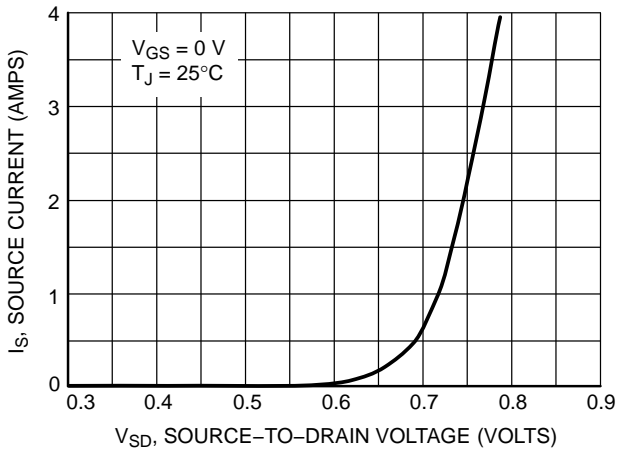


Figure 11. Diode Forward Voltage versus Current

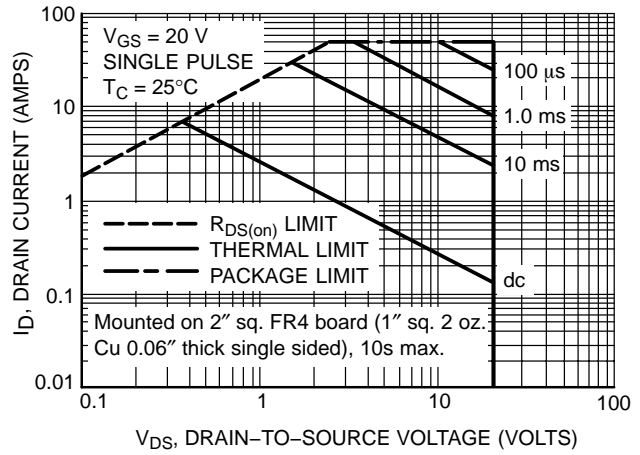


Figure 12. Maximum Rated Forward Biased Safe Operating Area

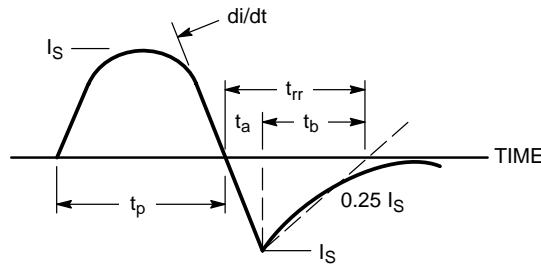


Figure 13. Diode Reverse Recovery Waveform

TYPICAL ELECTRICAL CHARACTERISTICS

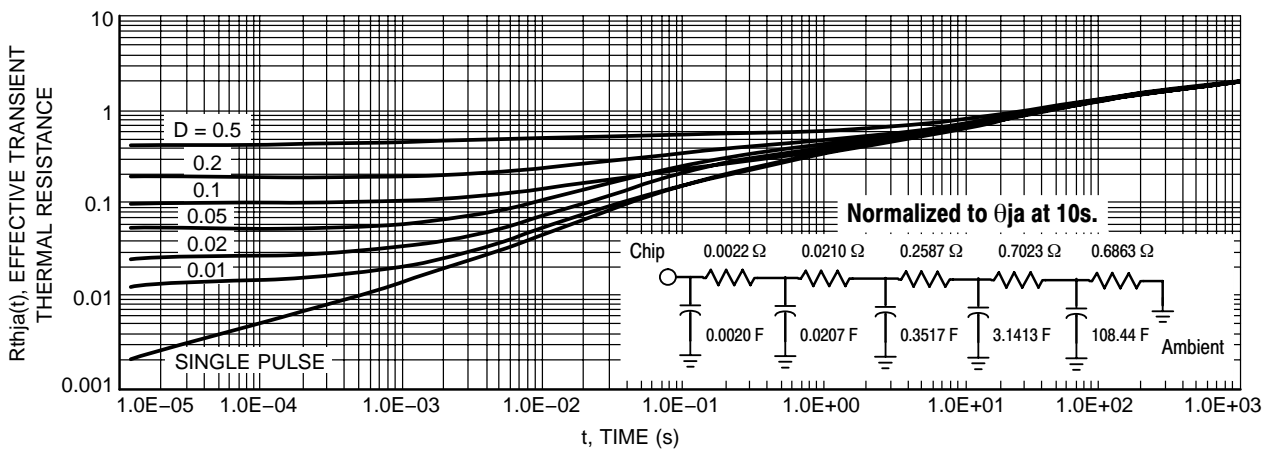
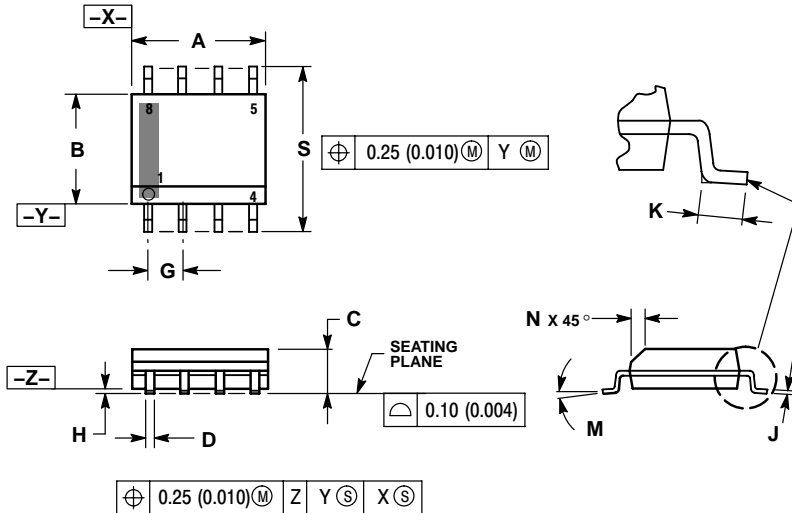


Figure 14. Thermal Response

NTMS4N01R2

PACKAGE DIMENSIONS

SOIC-8 NB
CASE 751-07
ISSUE AG



NOTES:

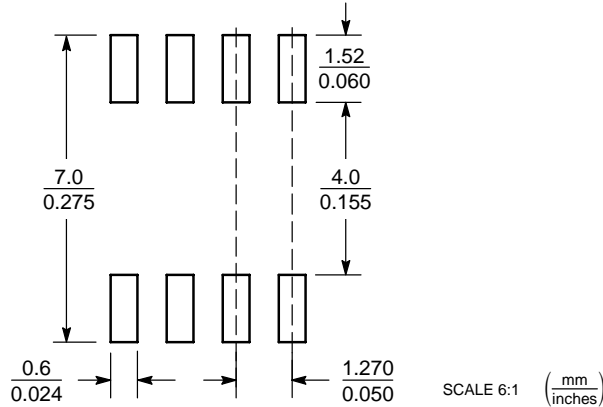
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0° 8°		0° 8°	
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

STYLE 13:

- PIN 1: N.C.
 2. SOURCE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
 P.O. Box 61312, Phoenix, Arizona 85082-1312 USA
 Phone: 480-829-7710 or 800-344-3860 Toll Free USA/Canada
 Fax: 480-829-7709 or 800-344-3867 Toll Free USA/Canada
 Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
 2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051
 Phone: 81-3-5773-3850

ON Semiconductor Website: <http://onsemi.com>

Order Literature: <http://www.onsemi.com/litorder>

For additional information, please contact your local Sales Representative.