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ON Semiconductor
NSBA114TDXV6T1G

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MUN5115DW1, NSBA114TDXV6, NSBA114TDP6

Dual PNP Bias Resistor Transistors
R1 = 10 kΩ, R2 = ∞ kΩ

PNP Transistors with Monolithic Bias Resistor Network

This series of digital transistors is designed to replace a single device and its external resistor bias network. The Bias Resistor Transistor (BRT) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. The BRT eliminates these individual components by integrating them into a single device. The use of a BRT can reduce both system cost and board space.

Features

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- S and NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS
(T_A = 25°C, common for Q_1 and Q_2, unless otherwise noted)

Rating	Symbol	Max	Unit
Collector-Base Voltage	V_{CBO}	50	Vdc
Collector-Emitter Voltage	V_{CEO}	50	Vdc
Collector Current – Continuous	I_C	100	mAdc
Input Forward Voltage	$V_{IN(fwd)}$	40	Vdc
Input Reverse Voltage	$V_{IN(rev)}$	5	Vdc

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

ORDERING INFORMATION

Device	Package	Shipping†
MUN5115DW1T1G, SMUN5115DW1T1G	SOT−363	3,000/Tape & Reel
NSBA114TDXV6T1G	SOT−563	4,000/Tape & Reel
NSBA114TDXV6T5G	SOT−563	8,000/Tape & Reel
NSBA114TDP6T5G	SOT−963	8,000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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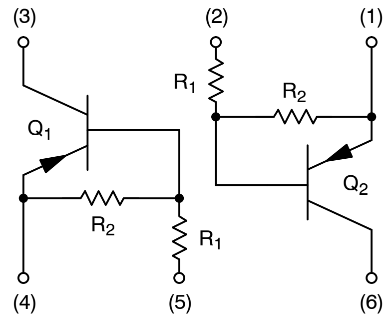
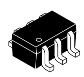
http://onsemi.com

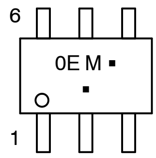
PIN CONNECTIONS

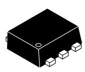


MARKING DIAGRAMS

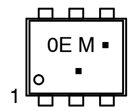


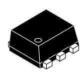
SOT−363
CASE 419B



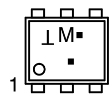


SOT−563
CASE 463A





SOT−963
CASE 527AD



0E/T	=	Specific Device Code
M	=	Date Code*
▪	=	Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation may vary depending upon manufacturing location.

THERMAL CHARACTERISTICS

Characteristic		Symbol	Max	Unit
MUN5115DW1 (SOT–363) ONE JUNCTION HEATED				
Total Device Dissipation T_A = 25°C Derate above 25°C	 (Note 1) (Note 2) (Note 1) (Note 2)	P_D	 187 256 1.5 2.0	 mW mW/°C
Thermal Resistance, Junction to Ambient	(Note 1) (Note 2)	$R_{\theta JA}$	670 490	°C/W
MUN5115DW1 (SOT–363) BOTH JUNCTION HEATED (Note 3)				
Total Device Dissipation T_A = 25°C Derate above 25°C	 (Note 1) (Note 2) (Note 1) (Note 2)	P_D	 250 385 2.0 3.0	 mW mW/°C
Thermal Resistance, Junction to Ambient	 (Note 1) (Note 2)	$R_{\theta JA}$	 493 325	°C/W
Thermal Resistance, Junction to Lead	 (Note 1) (Note 2)	$R_{\theta JL}$	 188 208	°C/W
Junction and Storage Temperature Range		T_J, T_{stg}	−55 to +150	°C
NSBA114TDXV6 (SOT–563) ONE JUNCTION HEATED				
Total Device Dissipation T_A = 25°C Derate above 25°C	 (Note 1) (Note 1)	P_D	 357 2.9	 mW mW/°C
Thermal Resistance, Junction to Ambient	 (Note 1)	$R_{\theta JA}$	 350	°C/W
NSBA114TDXV6 (SOT–563) BOTH JUNCTION HEATED (Note 3)				
Total Device Dissipation T_A = 25°C Derate above 25°C	 (Note 1) (Note 1)	P_D	 500 4.0	 mW mW/°C
Thermal Resistance, Junction to Ambient	 (Note 1)	$R_{\theta JA}$	 250	°C/W
Junction and Storage Temperature Range		T_J, T_{stg}	−55 to +150	°C
NSBA114TDP6 (SOT–963) ONE JUNCTION HEATED				
Total Device Dissipation T_A = 25°C Derate above 25°C	 (Note 4) (Note 5) (Note 4) (Note 5)	P_D	 231 269 1.9 2.2	 MW mW/°C
Thermal Resistance, Junction to Ambient	 (Note 4) (Note 5)	$R_{\theta JA}$	 540 464	°C/W
NSBA114TDP6 (SOT–963) BOTH JUNCTION HEATED (Note 3)				
Total Device Dissipation T_A = 25°C Derate above 25°C	 (Note 4) (Note 5) (Note 4) (Note 5)	P_D	 339 408 2.7 3.3	 MW mW/°C
Thermal Resistance, Junction to Ambient	 (Note 4) (Note 5)	$R_{\theta JA}$	 369 306	°C/W
Junction and Storage Temperature Range		T_J, T_{stg}	−55 to +150	°C

1. FR−4 @ Minimum Pad.
2. FR−4 @ 1.0 × 1.0 Inch Pad.
3. Both junction heated values assume total power is sum of two equally powered channels.
4. FR−4 @ 100 mm^2, 1 oz. copper traces, still air.
5. FR−4 @ 500 mm^2, 1 oz. copper traces, still air.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, common for Q_1 and Q_2, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Base Cutoff Current (V_{CB} = 50 V, I_E = 0)	I_{CBO}	–	–	100	nAdc
Collector-Emitter Cutoff Current (V_{CE} = 50 V, I_B = 0)	I_{CEO}	–	–	500	nAdc
Emitter-Base Cutoff Current (V_{EB} = 6.0 V, I_C = 0)	I_{EBO}	–	–	0.9	mAdc
Collector-Base Breakdown Voltage (I_C = 10 μA, I_E = 0)	$V_{(BR)CBO}$	50	–	–	Vdc
Collector-Emitter Breakdown Voltage (Note 6) (I_C = 2.0 mA, I_B = 0)	$V_{(BR)CEO}$	50	–	–	Vdc
ON CHARACTERISTICS					
DC Current Gain (Note 6) (I_C = 5.0 mA, V_{CE} = 10 V)	h_{FE}	160	250	–	
Collector-Emitter Saturation Voltage (Note 6) (I_C = 10 mA, I_B = 0.3 mA)	$V_{CE(sat)}$	–	–	0.25	V
Input Voltage (Off) (V_{CE} = 5.0 V, I_C = 100 μA)	$V_{i(off)}$	–	0.6	–	Vdc
Input Voltage (On) (V_{CE} = 0.2 V, I_C = 10 mA)	$V_{i(on)}$	–	1.4	–	Vdc
Output Voltage (On) (V_{CC} = 5.0 V, V_B = 2.5 V, R_L = 1.0 kΩ)	V_{OL}	–	–	0.2	Vdc
Output Voltage (Off) (V_{CC} = 5.0 V, V_B = 0.25 V, R_L = 1.0 kΩ)	V_{OH}	4.9	–	–	Vdc
Input Resistor	R1	7.0	10	13	kΩ
Resistor Ratio	R_1/R_2	–	–	–	

6. Pulsed Condition: Pulse Width = 300 ms, Duty Cycle ≤ 2%.

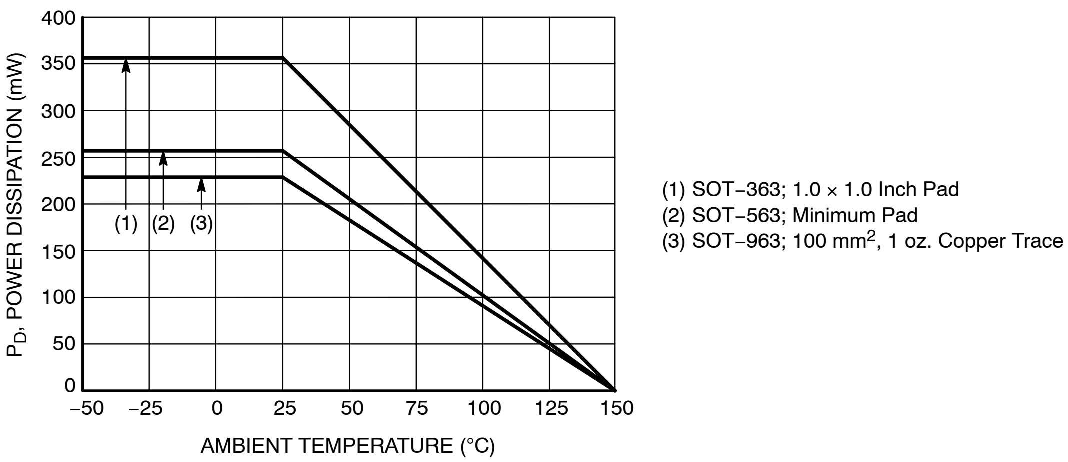


Figure 1. Derating Curve

TYPICAL CHARACTERISTICS
MUN5115DW1, NSBA114TDXV6

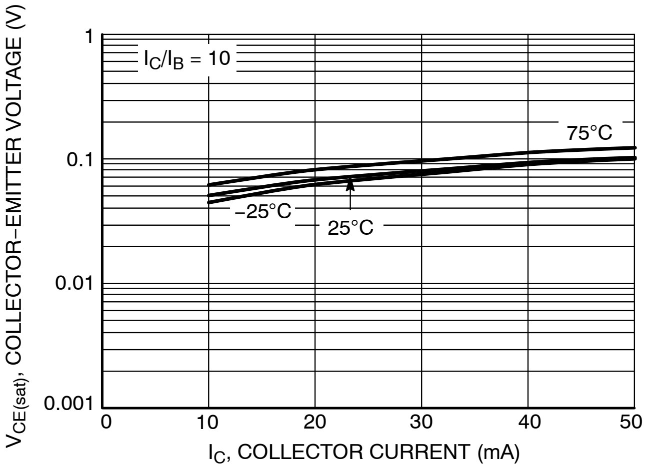


Figure 2. $V_{CE(sat)}$ vs. I_C

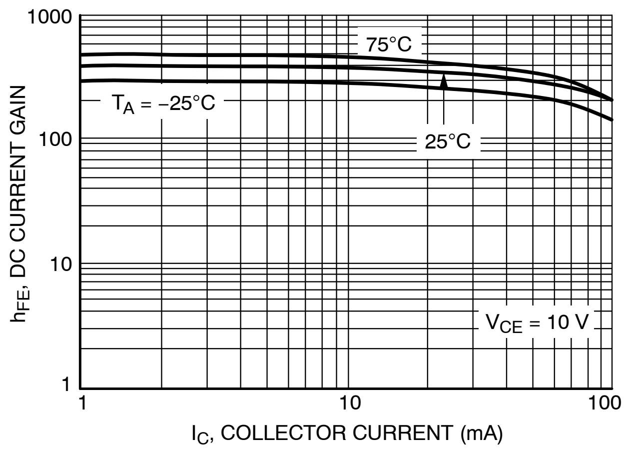


Figure 3. DC Current Gain

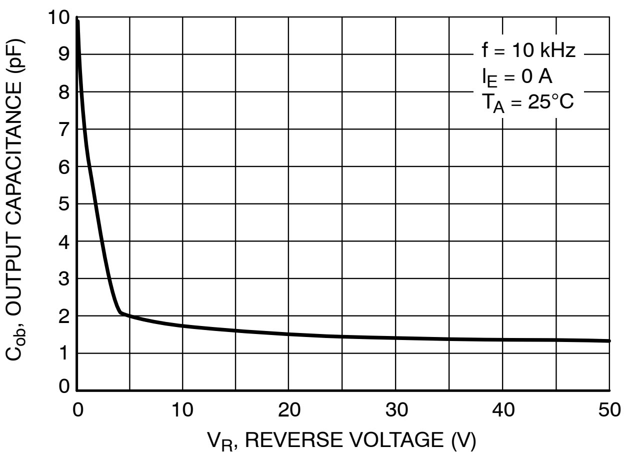


Figure 4. Output Capacitance

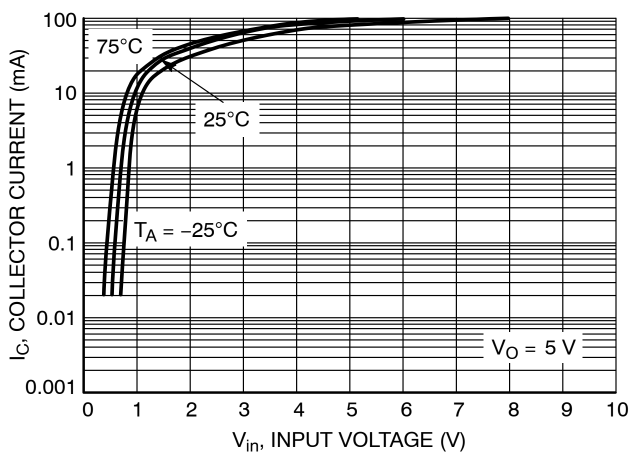


Figure 5. Output Current vs. Input Voltage

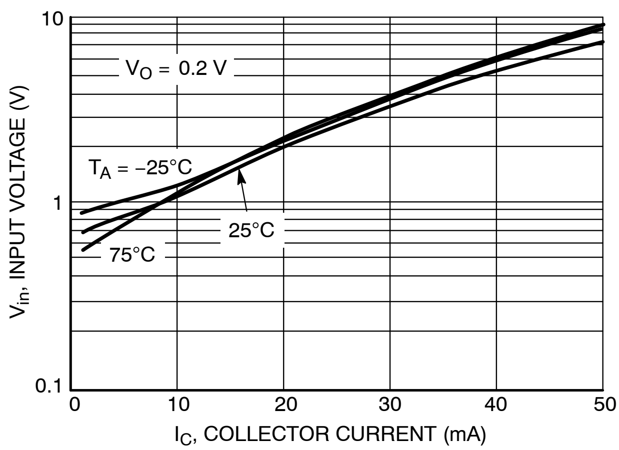


Figure 6. Input Voltage vs. Output Current

MUN5115DW1, NSBA114TDXV6, NSBA114TDP6

TYPICAL CHARACTERISTICS
NSBA114TDP6

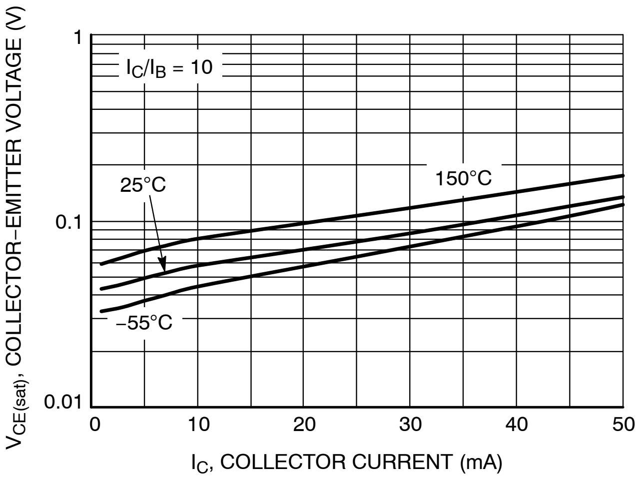


Figure 7. $V_{CE(sat)}$ vs. I_C

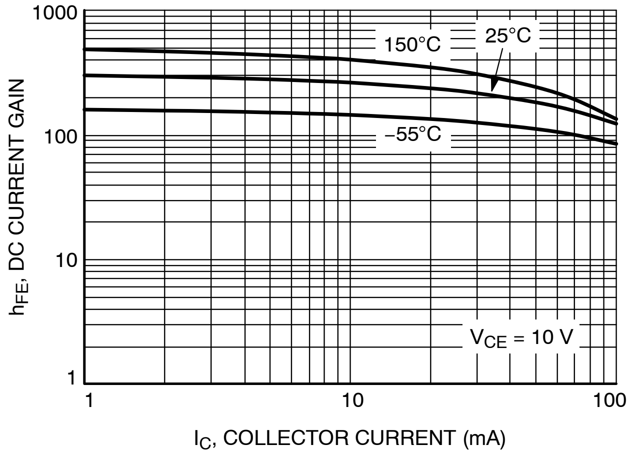


Figure 8. DC Current Gain

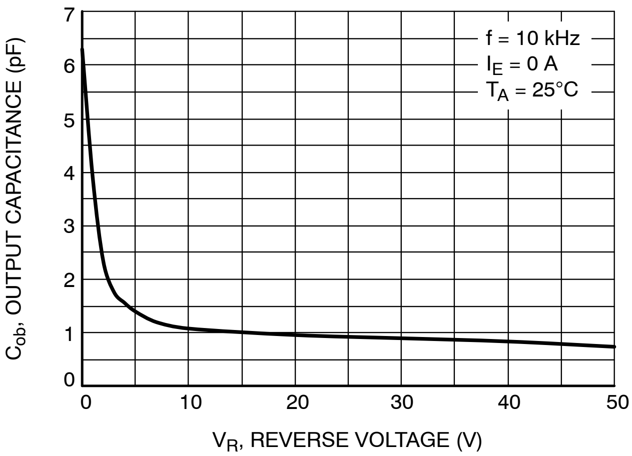


Figure 9. Output Capacitance

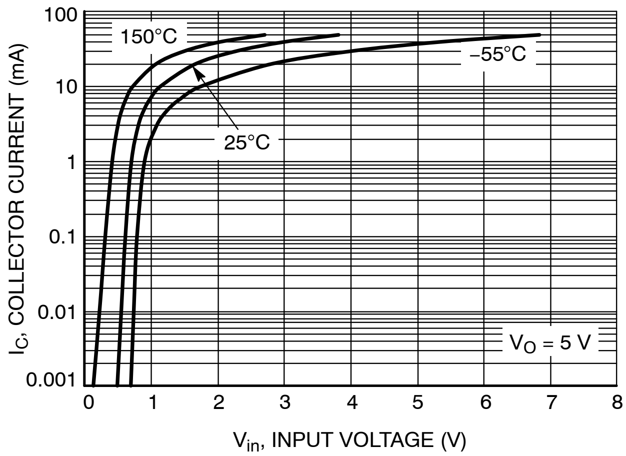


Figure 10. Output Current vs. Input Voltage

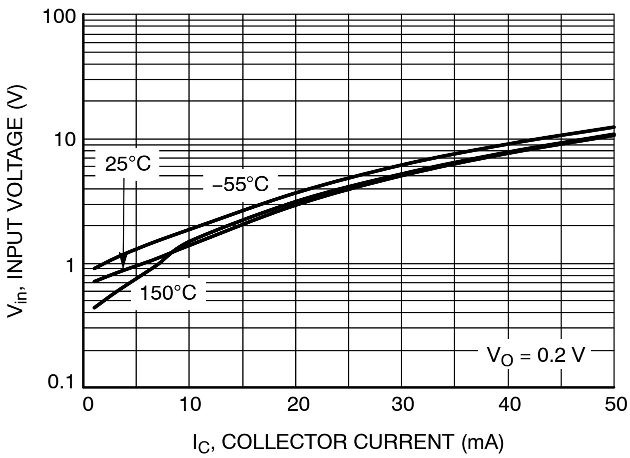
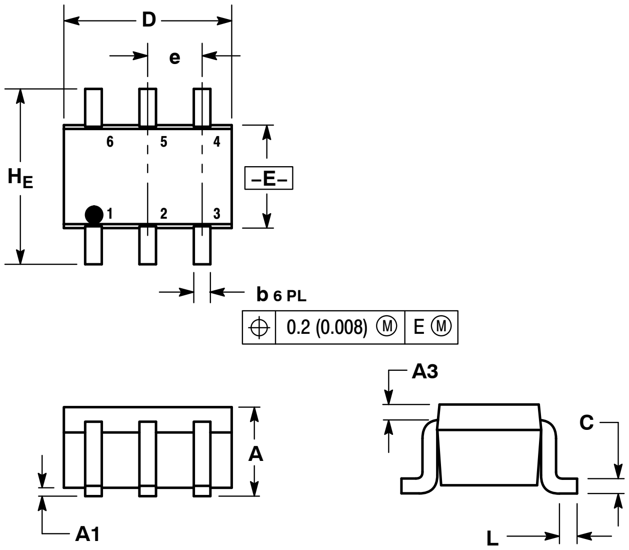


Figure 11. Input Voltage vs. Output Current

PACKAGE DIMENSIONS

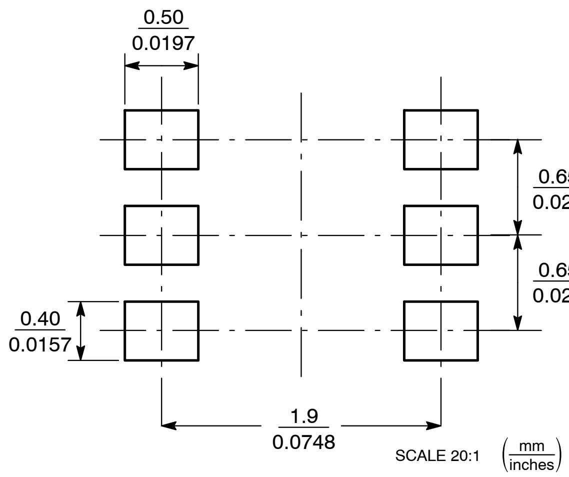
SC−88/SC70−6/SOT−363
CASE 419B−02
ISSUE W



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419B−01 OBSOLETE, NEW STANDARD 419B−02.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.95	1.10	0.031	0.037	0.043
A1	0.00	0.05	0.10	0.000	0.002	0.004
A3		0.20 REF			0.008 REF	
b	0.10	0.21	0.30	0.004	0.008	0.012
C	0.10	0.14	0.25	0.004	0.005	0.010
D	1.80	2.00	2.20	0.070	0.078	0.086
E	1.15	1.25	1.35	0.045	0.049	0.053
e		0.65 BSC			0.026 BSC	
L	0.10	0.20	0.30	0.004	0.008	0.012
H_E	2.00	2.10	2.20	0.078	0.082	0.086

SOLDERING FOOTPRINT*

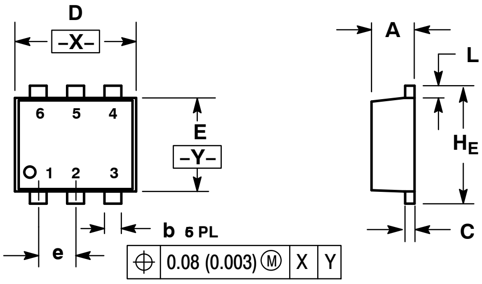


SC−88/SC70−6/SOT−363

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

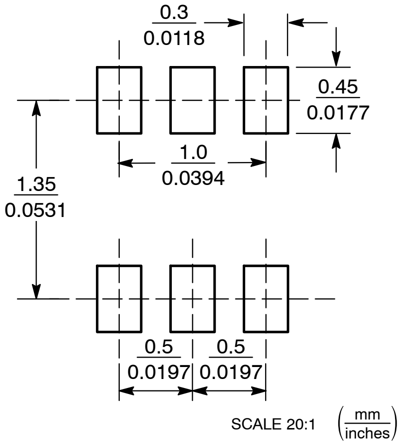
SOT−563, 6 LEAD
CASE 463A
ISSUE F



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.020	0.021	0.023
b	0.17	0.22	0.27	0.007	0.009	0.011
C	0.08	0.12	0.18	0.003	0.005	0.007
D	1.50	1.60	1.70	0.059	0.062	0.066
E	1.10	1.20	1.30	0.043	0.047	0.051
e		0.5 BSC			0.02 BSC	
L	0.10	0.20	0.30	0.004	0.008	0.012
H_E	1.50	1.60	1.70	0.059	0.062	0.066

SOLDERING FOOTPRINT*

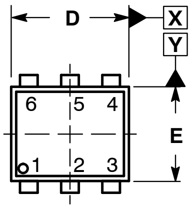


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

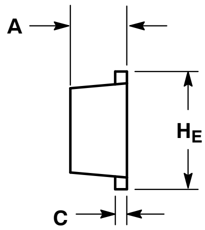
MUN5115DW1, NSBA114TDXV6, NSBA114TDP6

PACKAGE DIMENSIONS

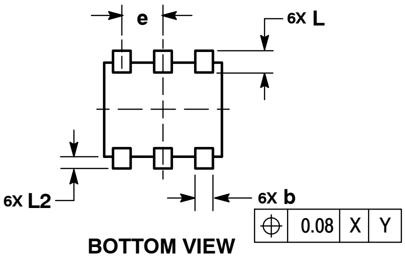
SOT−963
CASE 527AD
ISSUE E



TOP VIEW



SIDE VIEW

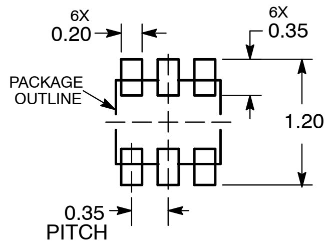


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.34	0.37	0.40
b	0.10	0.15	0.20
C	0.07	0.12	0.17
D	0.95	1.00	1.05
E	0.75	0.80	0.85
e		0.35 BSC	
H_E	0.95	1.00	1.05
L		0.19 REF	
L2	0.05	0.10	0.15

RECOMMENDED MOUNTING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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