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# MUN5115DW1, NSBA114TDXV6, NSBA114TDP6

## Dual PNP Bias Resistor Transistors R1 = 10 kΩ, R2 = ∞ kΩ

### PNP Transistors with Monolithic Bias Resistor Network

This series of digital transistors is designed to replace a single device and its external resistor bias network. The Bias Resistor Transistor (BRT) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. The BRT eliminates these individual components by integrating them into a single device. The use of a BRT can reduce both system cost and board space.

#### Features

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- S and NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

#### MAXIMUM RATINGS

(T<sub>A</sub> = 25°C, common for Q<sub>1</sub> and Q<sub>2</sub>, unless otherwise noted)

Rating	Symbol	Max	Unit
Collector-Base Voltage	V <sub>CBO</sub>	50	Vdc
Collector-Emitter Voltage	V <sub>CEO</sub>	50	Vdc
Collector Current – Continuous	I <sub>C</sub>	100	mAdc
Input Forward Voltage	V <sub>IN(fwd)</sub>	40	Vdc
Input Reverse Voltage	V <sub>IN(rev)</sub>	5	Vdc

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

#### ORDERING INFORMATION

Device	Package	Shipping†
MUN5115DW1T1G, SMUN5115DW1T1G	SOT-363	3,000/Tape & Reel
NSBA114TDXV6T1G	SOT-563	4,000/Tape & Reel
NSBA114TDXV6T5G	SOT-563	8,000/Tape & Reel
NSBA114TDP6T5G	SOT-963	8,000/Tape & Reel

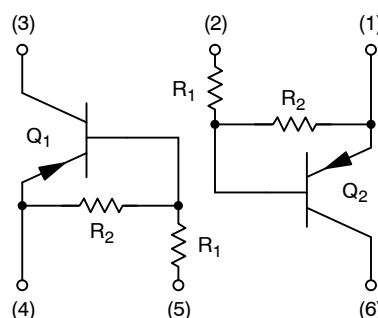
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



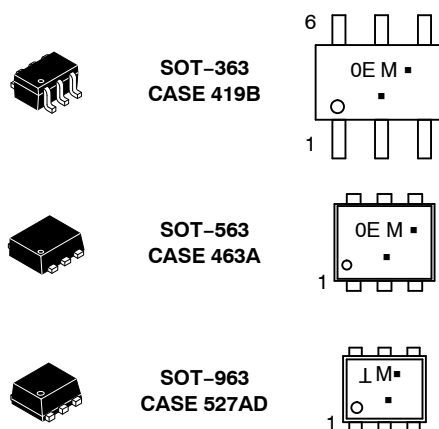
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http://onsemi.com

#### PIN CONNECTIONS



#### MARKING DIAGRAMS



0E/T = Specific Device Code

M = Date Code\*

▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*Date Code orientation may vary depending upon manufacturing location.

**MUN5115DW1, NSBA114TDXV6, NSBA114TDP6**
**THERMAL CHARACTERISTICS**

Characteristic	Symbol	Max	Unit
<b>MUN5115DW1 (SOT-363) ONE JUNCTION HEATED</b>			
Total Device Dissipation $T_A = 25^\circ\text{C}$	$P_D$	187	mW
Derate above $25^\circ\text{C}$		256	$\text{mW}/^\circ\text{C}$
		1.5	
		2.0	
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	670	$^\circ\text{C}/\text{W}$
		490	
<b>MUN5115DW1 (SOT-363) BOTH JUNCTION HEATED (Note 3)</b>			
Total Device Dissipation $T_A = 25^\circ\text{C}$	$P_D$	250	mW
Derate above $25^\circ\text{C}$		385	$\text{mW}/^\circ\text{C}$
		2.0	
		3.0	
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	493	$^\circ\text{C}/\text{W}$
		325	
Thermal Resistance, Junction to Lead	$R_{\theta JL}$	188	$^\circ\text{C}/\text{W}$
		208	
Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$
<b>NSBA114TDXV6 (SOT-563) ONE JUNCTION HEATED</b>			
Total Device Dissipation $T_A = 25^\circ\text{C}$	$P_D$	357	mW
Derate above $25^\circ\text{C}$		2.9	$\text{mW}/^\circ\text{C}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	350	$^\circ\text{C}/\text{W}$
<b>NSBA114TDXV6 (SOT-563) BOTH JUNCTION HEATED (Note 3)</b>			
Total Device Dissipation $T_A = 25^\circ\text{C}$	$P_D$	500	mW
Derate above $25^\circ\text{C}$		4.0	$\text{mW}/^\circ\text{C}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	250	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$
<b>NSBA114TDP6 (SOT-963) ONE JUNCTION HEATED</b>			
Total Device Dissipation $T_A = 25^\circ\text{C}$	$P_D$	231	MW
Derate above $25^\circ\text{C}$		269	$\text{mW}/^\circ\text{C}$
		1.9	
		2.2	
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	540	$^\circ\text{C}/\text{W}$
		464	
<b>NSBA114TDP6 (SOT-963) BOTH JUNCTION HEATED (Note 3)</b>			
Total Device Dissipation $T_A = 25^\circ\text{C}$	$P_D$	339	MW
Derate above $25^\circ\text{C}$		408	$\text{mW}/^\circ\text{C}$
		2.7	
		3.3	
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	369	$^\circ\text{C}/\text{W}$
		306	
Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$

1. FR-4 @ Minimum Pad.

 2. FR-4 @  $1.0 \times 1.0$  Inch Pad.

3. Both junction heated values assume total power is sum of two equally powered channels.

 4. FR-4 @  $100 \text{ mm}^2$ , 1 oz. copper traces, still air.

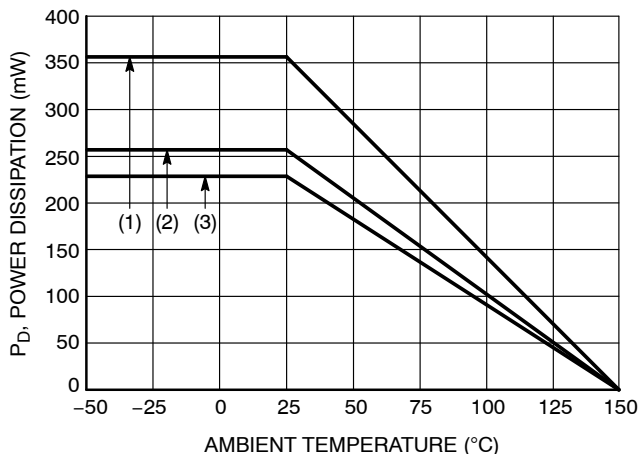
 5. FR-4 @  $500 \text{ mm}^2$ , 1 oz. copper traces, still air.

### MUN5115DW1, NSBA114TDXV6, NSBA114TDP6

**ELECTRICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$ , common for  $Q_1$  and  $Q_2$ , unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Collector-Base Cutoff Current ( $V_{CB} = 50\text{ V}$ , $I_E = 0$ )	$I_{CBO}$	-	-	100	nA <sub>dc</sub>
Collector-Emitter Cutoff Current ( $V_{CE} = 50\text{ V}$ , $I_B = 0$ )	$I_{CEO}$	-	-	500	nA <sub>dc</sub>
Emitter-Base Cutoff Current ( $V_{EB} = 6.0\text{ V}$ , $I_C = 0$ )	$I_{EBO}$	-	-	0.9	mA <sub>dc</sub>
Collector-Base Breakdown Voltage ( $I_C = 10\ \mu\text{A}$ , $I_E = 0$ )	$V_{(BR)CBO}$	50	-	-	V <sub>dc</sub>
Collector-Emitter Breakdown Voltage (Note 6) ( $I_C = 2.0\text{ mA}$ , $I_B = 0$ )	$V_{(BR)CEO}$	50	-	-	V <sub>dc</sub>
<b>ON CHARACTERISTICS</b>					
DC Current Gain (Note 6) ( $I_C = 5.0\text{ mA}$ , $V_{CE} = 10\text{ V}$ )	$h_{FE}$	160	250	-	
Collector-Emitter Saturation Voltage (Note 6) ( $I_C = 10\text{ mA}$ , $I_B = 0.3\text{ mA}$ )	$V_{CE(sat)}$	-	-	0.25	V
Input Voltage (Off) ( $V_{CE} = 5.0\text{ V}$ , $I_C = 100\ \mu\text{A}$ )	$V_{i(off)}$	-	0.6	-	V <sub>dc</sub>
Input Voltage (On) ( $V_{CE} = 0.2\text{ V}$ , $I_C = 10\text{ mA}$ )	$V_{i(on)}$	-	1.4	-	V <sub>dc</sub>
Output Voltage (On) ( $V_{CC} = 5.0\text{ V}$ , $V_B = 2.5\text{ V}$ , $R_L = 1.0\text{ k}\Omega$ )	$V_{OL}$	-	-	0.2	V <sub>dc</sub>
Output Voltage (Off) ( $V_{CC} = 5.0\text{ V}$ , $V_B = 0.25\text{ V}$ , $R_L = 1.0\text{ k}\Omega$ )	$V_{OH}$	4.9	-	-	V <sub>dc</sub>
Input Resistor	$R_1$	7.0	10	13	k $\Omega$
Resistor Ratio	$R_1/R_2$	-	-	-	

6. Pulsed Condition: Pulse Width = 300 ms, Duty Cycle  $\leq$  2%.

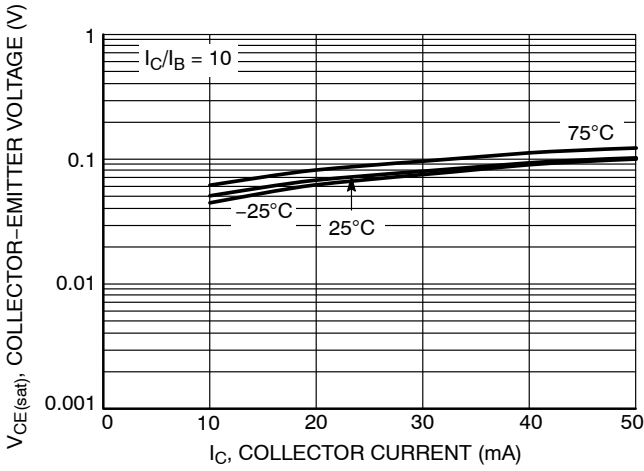


- (1) SOT-363; 1.0 x 1.0 Inch Pad
- (2) SOT-563; Minimum Pad
- (3) SOT-963; 100 mm<sup>2</sup>, 1 oz. Copper Trace

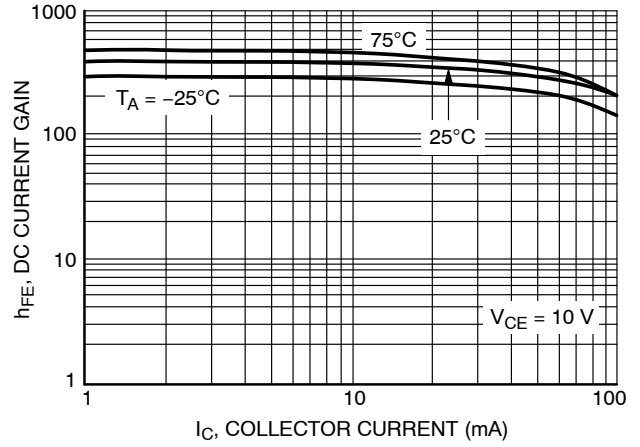
Figure 1. Derating Curve

**MUN5115DW1, NSBA114TDXV6, NSBA114TDP6**

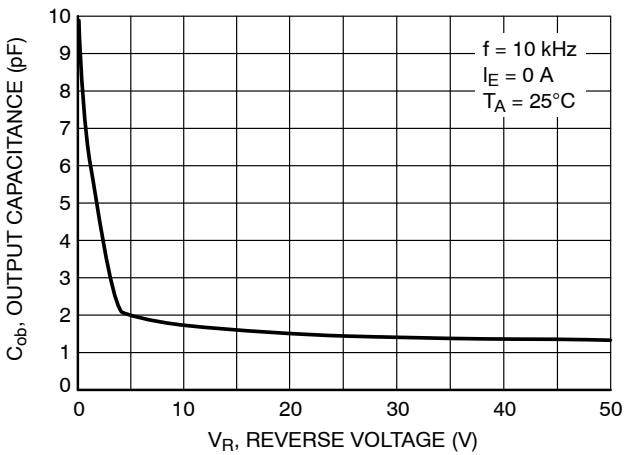
**TYPICAL CHARACTERISTICS  
 MUN5115DW1, NSBA114TDXV6**



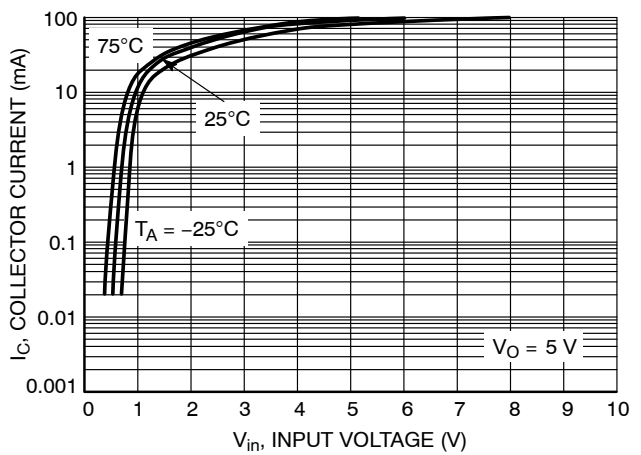
**Figure 2.  $V_{CE(sat)}$  vs.  $I_C$**



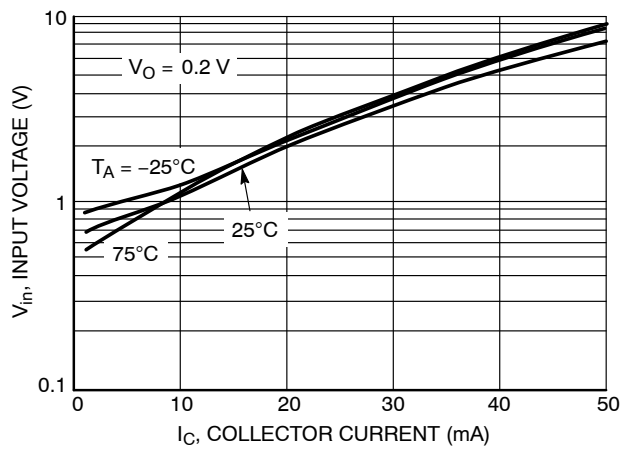
**Figure 3. DC Current Gain**



**Figure 4. Output Capacitance**



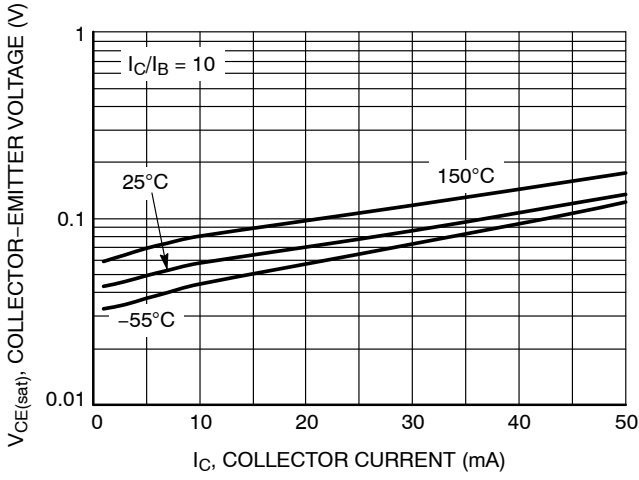
**Figure 5. Output Current vs. Input Voltage**



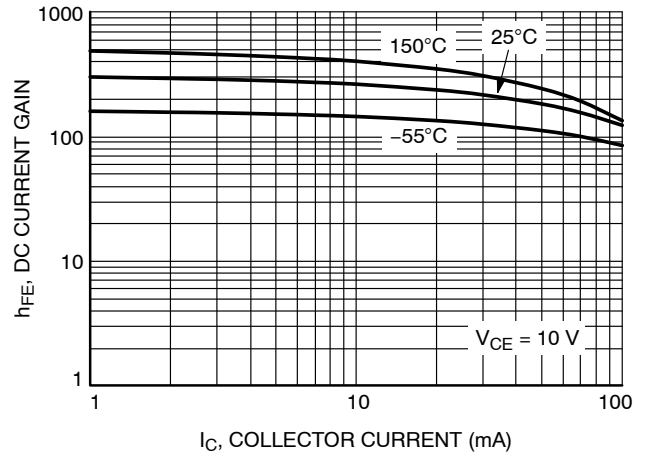
**Figure 6. Input Voltage vs. Output Current**

**MUN5115DW1, NSBA114TDXV6, NSBA114TDP6**

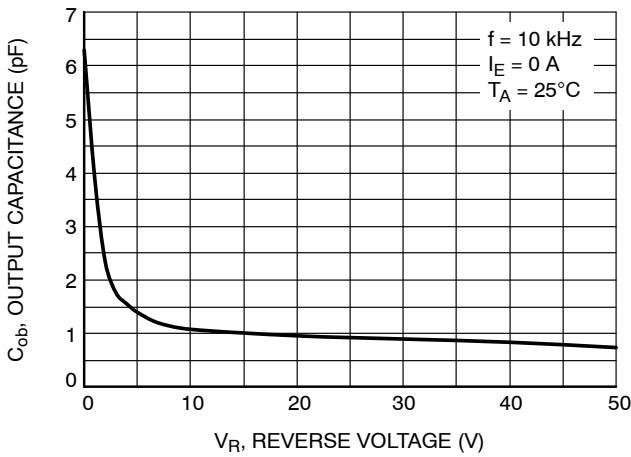
**TYPICAL CHARACTERISTICS  
 NSBA114TDP6**



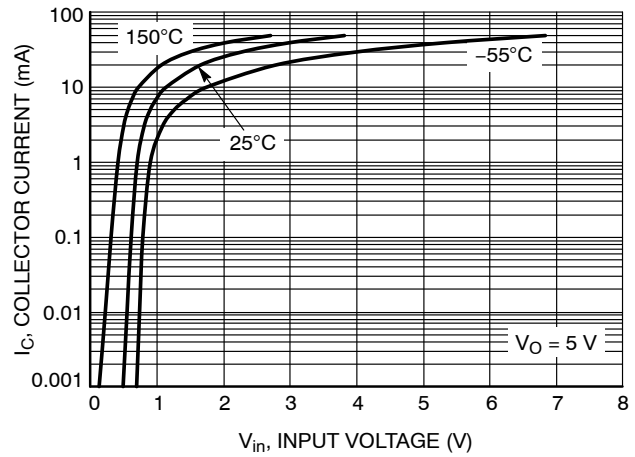
**Figure 7.  $V_{CE(sat)}$  vs.  $I_C$**



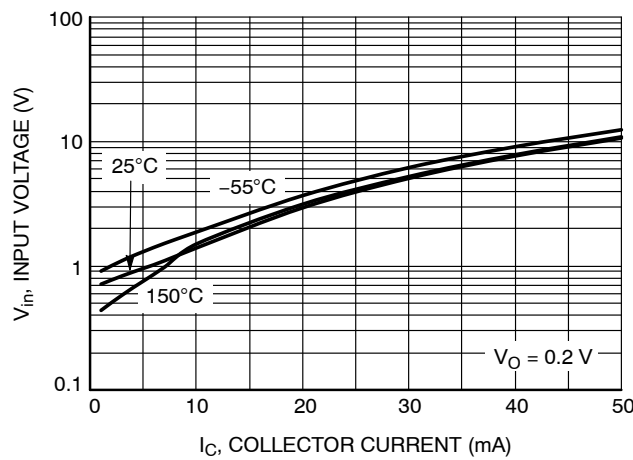
**Figure 8. DC Current Gain**



**Figure 9. Output Capacitance**



**Figure 10. Output Current vs. Input Voltage**



**Figure 11. Input Voltage vs. Output Current**

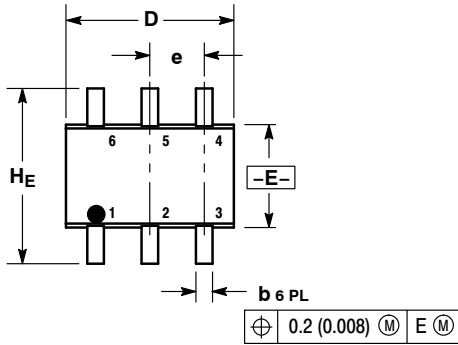
**MUN5115DW1, NSBA114TDXV6, NSBA114TDP6**

**PACKAGE DIMENSIONS**

**SC-88/SC70-6/SOT-363**

CASE 419B-02

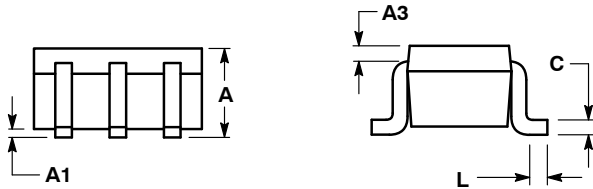
ISSUE W



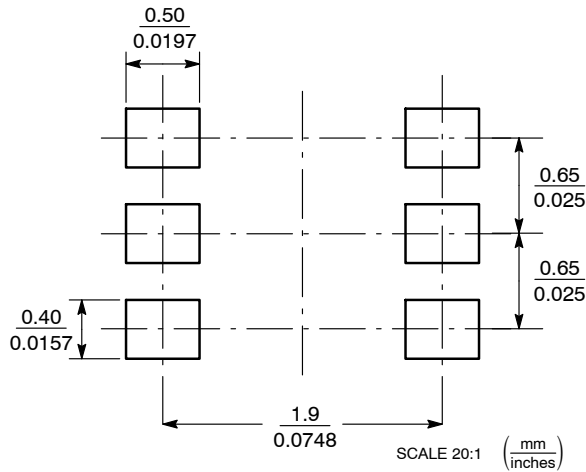
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419B-01 OBSOLETE, NEW STANDARD 419B-02.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.95	1.10	0.031	0.037	0.043
A1	0.00	0.05	0.10	0.000	0.002	0.004
A3	0.20 REF			0.008 REF		
b	0.10	0.21	0.30	0.004	0.008	0.012
C	0.10	0.14	0.25	0.004	0.005	0.010
D	1.80	2.00	2.20	0.070	0.078	0.086
E	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65 BSC			0.026 BSC		
L	0.10	0.20	0.30	0.004	0.008	0.012
HE	2.00	2.10	2.20	0.078	0.082	0.086



**SOLDERING FOOTPRINT\***



**SC-88/SC70-6/SOT-363**

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

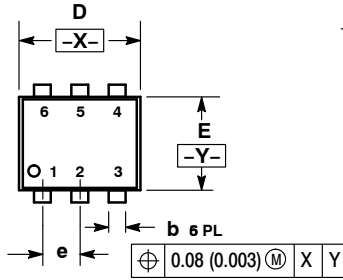
**MUN5115DW1, NSBA114TDXV6, NSBA114TDP6**

**PACKAGE DIMENSIONS**

**SOT-563, 6 LEAD**

CASE 463A

ISSUE F

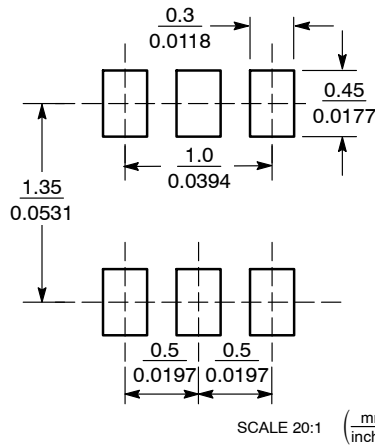


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.020	0.021	0.023
b	0.17	0.22	0.27	0.007	0.009	0.011
C	0.08	0.12	0.18	0.003	0.005	0.007
D	1.50	1.60	1.70	0.059	0.062	0.066
E	1.10	1.20	1.30	0.043	0.047	0.051
e	0.5 BSC			0.02 BSC		
L	0.10	0.20	0.30	0.004	0.008	0.012
H <sub>E</sub>	1.50	1.60	1.70	0.059	0.062	0.066

**SOLDERING FOOTPRINT\***



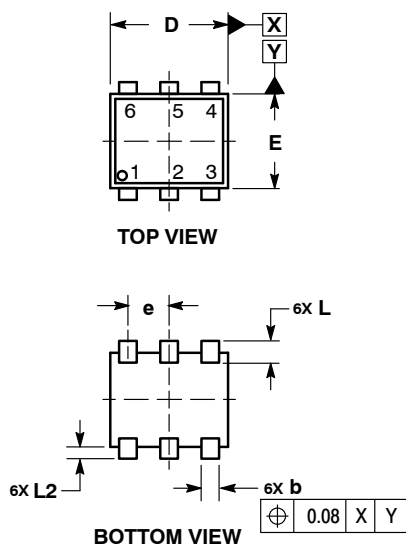
\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



## MUN5115DW1, NSBA114TDXV6, NSBA114TDP6

### PACKAGE DIMENSIONS

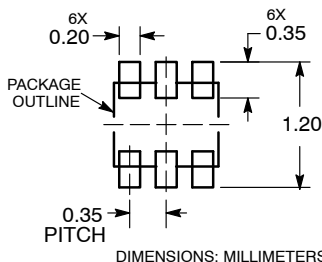
#### SOT-963 CASE 527AD ISSUE E




- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETERS
  3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
  4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.34	0.37	0.40
b	0.10	0.15	0.20
C	0.07	0.12	0.17
D	0.95	1.00	1.05
E	0.75	0.80	0.85
e	0.35 BSC		
H <sub>E</sub>	0.95	1.00	1.05
L	0.19 REF		
L <sub>2</sub>	0.05	0.10	0.15

#### RECOMMENDED MOUNTING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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