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June 1998

## FDR4420A

### Single N-Channel, Logic Level, PowerTrench™ MOSFET

#### General Description

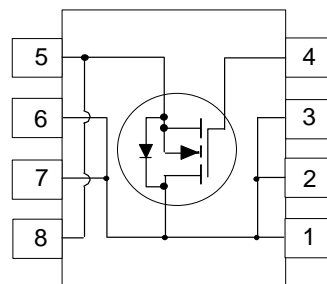
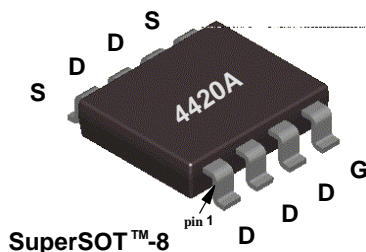
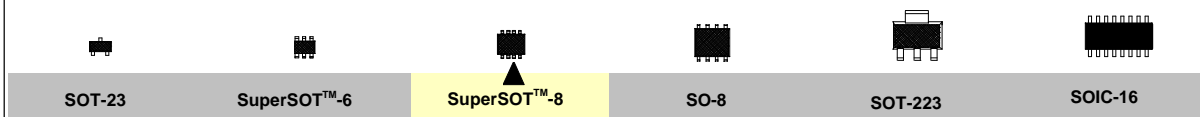
The SuperSOT-8 family of N-Channel Logic Level MOSFETs have been designed to provide a low profile, small footprint alternative to industry standard SO-8 little foot type product.

These MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench process that has been tailored to minimize the on-state resistance and yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applications where small package size is required without compromising power handling and fast switching.

#### Features

- 11 A, 30 V.  $R_{DS(ON)} = 0.009 \Omega$  @  $V_{GS} = 10$  V,  
 $R_{DS(ON)} = 0.013 \Omega$  @  $V_{GS} = 4.5$  V.
- Fast switching speed.
- Low gate charge.
- Small footprint 38% smaller than a standard SO-8.
- Low profile package(1mm thick).
- Power handling capability similar to SO-8.



#### Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FDR4420A	Units
$V_{DSS}$	Drain-Source Voltage	30	V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Drain Current - Continuous (Note 1a)	11	A
	- Pulsed	40	
$P_D$	Maximum Power Dissipation (Note 1a)	1.8	W
	(Note 1b)	1	
	(Note 1c)	0.9	
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to 150	$^\circ\text{C}$

#### THERMAL CHARACTERISTICS

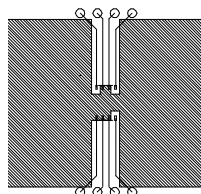
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	70	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	20	$^\circ\text{C/W}$

# **Electrical Characteristics** ( $T_A = 25^{\circ}\text{C}$ unless otherwise noted)

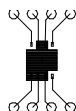
Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	30			V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	$I_D = 250\text{ }\mu\text{A}$ , Referenced to $25\text{ }^{\circ}\text{C}$		20		mV / $^{\circ}\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
		$T_J = 55^{\circ}\text{C}$			10	$\mu\text{A}$
$I_{GSS}$	Gate - Body Leakage Current	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA
$I_{GSS}$	Gate - Body Leakage, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$			-100	nA
ON CHARACTERISTICS (Note 2)						
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Temp.Coefficient	$I_D = 250\text{ }\mu\text{A}$ , Referenced to $25\text{ }^{\circ}\text{C}$		-6		mV / $^{\circ}\text{C}$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1	1.4	3	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 11\text{ A}$		0.0075	0.009	$\Omega$
		$T_J = 125^{\circ}\text{C}$		0.0125	0.016	
		$V_{GS} = 4.5\text{ V}, I_D = 9\text{ A}$		0.01	0.013	
$I_{D(ON)}$	On-State Drain Current	$V_{GS} = 10\text{ V}, V_{DS} = 5\text{ V}$	30			A
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{ V}, I_D = 11\text{ A}$		25		S
DYNAMIC CHARACTERISTICS						
$C_{iss}$	Input Capacitance	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		2560		pF
$C_{oss}$	Output Capacitance			560		pF
$C_{rss}$	Reverse Transfer Capacitance			280		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	$V_{DD} = 10\text{ V}, I_D = 1\text{ A},$ $V_{GS} = 10\text{V}, R_{GEN} = 1\text{ }\Omega$		11	20	ns
$t_r$	Turn - On Rise Time			15	27	ns
$t_{D(off)}$	Turn - Off Delay Time			25	40	ns
$t_f$	Turn - Off Fall Time			21	34	ns
$Q_g$	Total Gate Charge	$V_{DS} = 15\text{ V}, I_D = 9.3\text{ A},$ $V_{GS} = 5\text{ V}$		23	33	nC
$Q_{gs}$	Gate-Source Charge			7		nC
$Q_{gd}$	Gate-Drain Charge			11		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
$I_S$	Maximum Continuous Drain-Source Diode Forward Current				1.5	A
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 1.5\text{ A}$ (Note 2)		0.7	1.2	V

Notes:

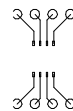
1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JA}$  is guaranteed by design while  $R_{\theta JC}$  is determined by the user's board design.  $R_{\theta JA}$  shown below for single device operation on FR-4 board in still air.



a.  $70^{\circ}\text{C/W}$  on a  $1\text{ in}^2$  pad of 2oz copper.



b.  $125^{\circ}\text{C/W}$  on a  $0.026\text{ in}^2$  of pad of 2oz copper.



c.  $135^{\circ}\text{C/W}$  on a  $0.005\text{ in}^2$  of pad of 2oz copper.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

## Typical Electrical Characteristics

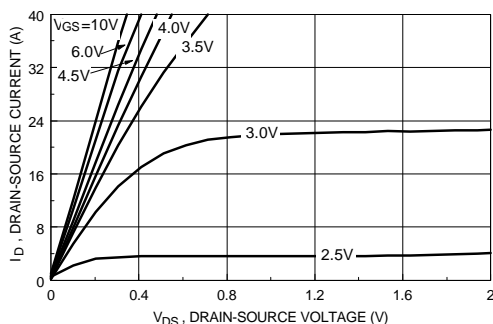


Figure 1. On-Region Characteristics.

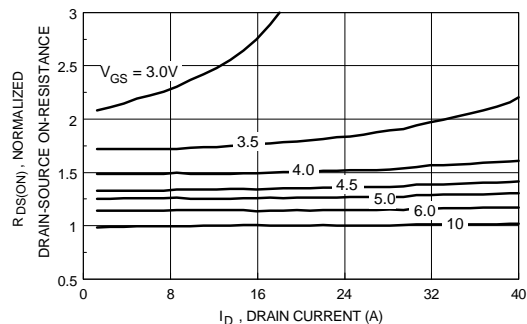


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

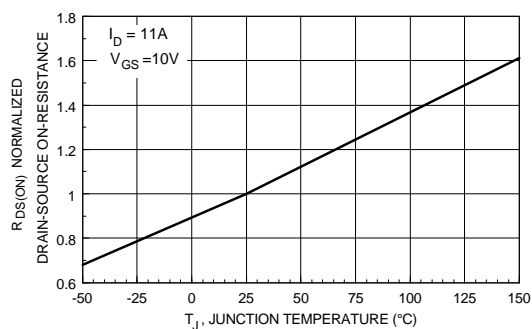


Figure 3. On-Resistance Variation with Temperature.

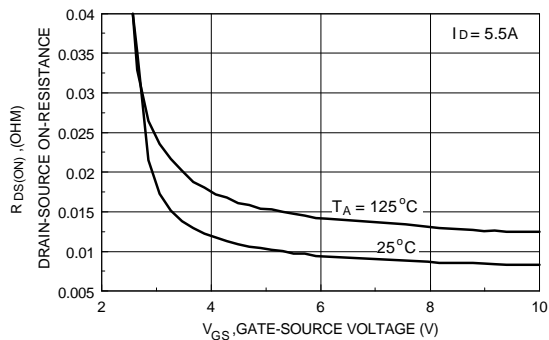


Figure 4. On Resistance Variation with Gate-To-Source Voltage.

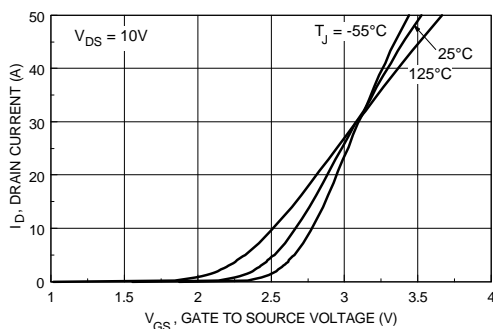


Figure 5. Transfer Characteristics.

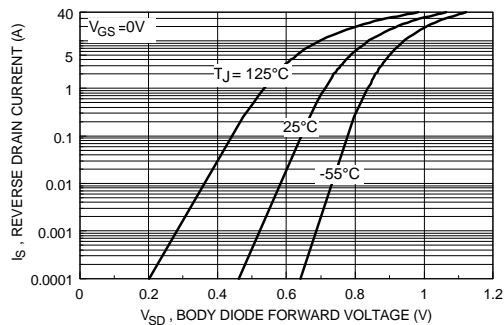


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

## Typical Electrical Characteristics (continued)

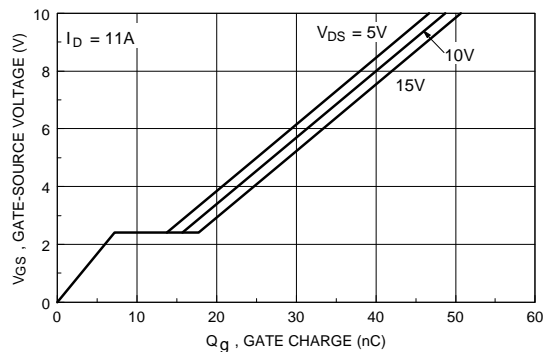


Figure 7. Gate Charge Characteristics.

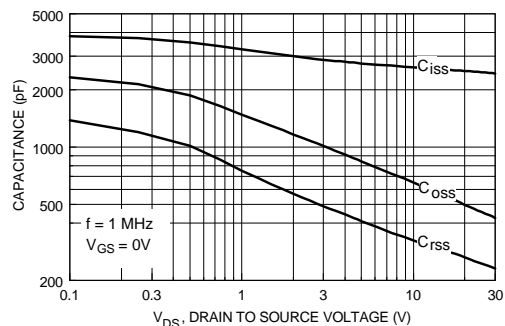


Figure 8. Capacitance Characteristics.

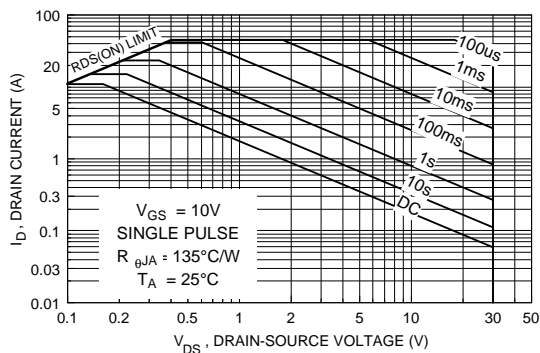


Figure 9. Maximum Safe Operating Area.

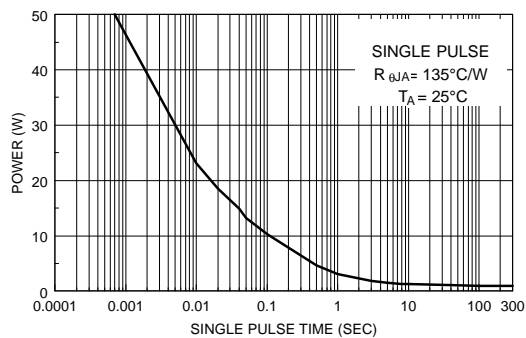


Figure 10. Single Pulse Maximum Power Dissipation.

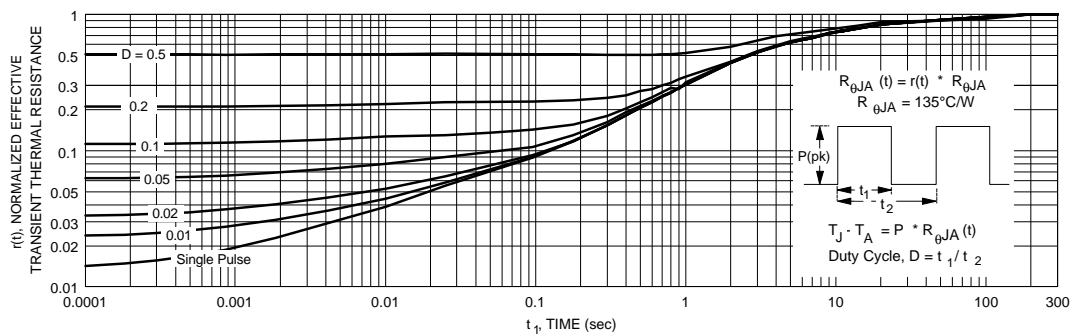


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in note 1c.  
Transient thermal response will change depending on the circuit board design.

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DOMET <sup>TM</sup>	HiSeC <sup>TM</sup>	PowerTrench <sup>®</sup>	SuperSOT <sup>TM</sup> -8	
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