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Advance Information

MPC8240RXXPNS
Rev. 0, 11/2003

MPC8240 Part Number Specification for the XPC8240RXXnnnx Series

Part Numbers Affected:

XPC8240RZU250E
XPC8240RVV250E

This document describes part-number-specific changes to recommended operating conditions and revised electrical specifications, as applicable, from those described in the general *MPC8240 Integrated Processor Hardware Specifications* (Order No. MPC8240EC).

Specifications provided in this document supersede those in the *MPC8240 Integrated Processor Hardware Specifications*, Revision 1.0 or later, for the part numbers listed in Table A only. Specifications not addressed herein are unchanged. Because this document is frequently updated, refer to http://www.freescale.com or to a local Freescale sales office for the latest version.

Note that headings and table numbers in this document are not consecutively numbered. They correspond to the heading or table affected in the general hardware specification.

The part numbers addressed in this document are listed in Table A. For more detailed ordering information, see Section 1.9, “Ordering Information.”

Table A. Part Number Addressed by This Data Sheet

M Part Number	Operating Conditions			Significant Differences from Hardware Specification
	CPU Frequency	V_{DD}	T_J (°C)	
XPC8240RVV250x XPC8240RZU250x	250 MHz	2.625 ±125 mV	0 to 105	Modified voltage specifications to achieve 250 MHz

Note: The X prefix in a Freescale part number designates a “Pilot Production Prototype” as defined by Freescale SOP 3-13. These are part of a limited production volume of prototypes manufactured, tested, and Q.A.-inspected on qualified technology to simulate normal production. These parts have only preliminary reliability and characterization data. Before pilot production prototypes may be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur while shipping pilot production prototypes.

1.2 Features

This section summarizes changes to the features of the MPC8240 described in the *MPC8240 Integrated Processor Hardware Specifications*.

- Power management

— 2.625-V processor core

1.3 General Parameters

This section summarizes changes to the general parameters of the MPC8240 described in the *MPC8240 Integrated Processor Hardware Specifications*.

- Core power supply 2.625 V ±125 mV DC nominal

1.4.1. DC Electrical Characteristics

Table 2 provides the recommended operating conditions for the MPC8240 part numbers described herein.

Table 2. Recommended Operating Conditions

Characteristic		Symbol	Recommended Value	Unit	Notes
Supply voltage		V_{DD}	2.625 ±5%	V	4, 6
Supply voltage for PCI and standard bus standards		OV_{DD}	3.3 ±0.3	V	6
Supply voltages for memory bus drivers		GV_{DD}	3.3 ±5%	V	8
PLL supply voltage—CPU core logic		AV_{DD}	2.625 ±5%	V	4, 6
PLL supply voltage—peripheral logic		$AV_{DD}2$	2.6255 ±5%	V	4, 7
DLL supply voltage		LAV_{DD}	2.625 ±5%	V	4, 7
PCI reference		LV_{DD}	5.0 ±5%	V	9, 10
			3.3 ±0.3	V	9, 10
Input voltage	LV_{DD} input-tolerant signals	V_{in}	0 to 3.6 or 5.75	V	2, 3
	All other inputs		0 to 3.6	V	5

Table 2. Recommended Operating Conditions (continued)

Characteristic	Symbol	Recommended Value	Unit	Notes
Die-junction temperature	T_j	0 to 105	°C	

Notes:

1. These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.
2. These signals are designed to withstand LV_{DD} + 0.5 V DC when LV_{DD} is connected to a 3.3- or 5.0-V DC power supply.
3. LV_{DD} input tolerant signals: PCI interface, EPIC control, and OSC_IN signals.
4. See Section 1.9, “Ordering Information,” for details on a modified voltage (V_{DD}) version device.

Cautions:

5. Input voltage (V_{in}) must not be greater than the supply voltage (V_{DD}/AV_{DD}/AV_{DD}2/LAV_{DD}) by more than 2.5 V at all times, including during power-on reset.
6. OV_{DD} must not exceed V_{DD}/AV_{DD}/AV_{DD}2/LAV_{DD} by more than 1.8 V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
7. V_{DD}/AV_{DD}/AV_{DD}2/LAV_{DD} must not exceed OV_{DD} by more than 0.6 V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
8. GV_{DD} must not exceed V_{DD}/AV_{DD}/AV_{DD}2/LAV_{DD} by more than 1.8 V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
9. LV_{DD} must not exceed V_{DD}/AV_{DD}/AV_{DD}2/LAV_{DD} by more than 5.4 V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
10. LV_{DD} must not exceed OV_{DD} by more than 3.6 V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

1.4.1.5 Power Characteristics

Table 5 provides power consumption data for the MPC8240. Power consumption on the PLL supply pins (AV_{DD} and AV_{DD}2) and the DLL supply pin (LAVDD) less than 15 mW. This parameter is guaranteed by design and is not tested.

Table 5. Preliminary Power Consumption

Mode	PCI Bus Clock/Memory Bus Clock CPU Clock Frequency (MHz)						Unit	Notes
	33/66/233	33/83/250	33/100/200	33/100/250	66/100/200	66/100/250		
Typical	3.4	3.6	3.2	3.7	3.2	3.8	W	1, 5
Maximum—FP	3.8	4.1	3.6	4.2	3.6	4.3	W	1, 2
Maximum—INT	3.4	3.7	3.3	3.8	3.4	3.8	W	1, 3
Doze	2.2	2.4	2.2	2.6	2.2	2.6	W	1, 4, 6
Nap	700	800	900	900	900	900	mW	1, 4, 6
Sleep	500	500	500	500	800	800	mW	1, 4, 6
I/O Power Supplies								
Mode	**Minimum**			**Maximum**			**Unit**	**Notes**
Typical—OV_{DD}	200			600			mW	7, 8

Table 5. Preliminary Power Consumption (continued)

Mode	PCI Bus Clock/Memory Bus Clock CPU Clock Frequency (MHz)						Unit	Notes
	33/66/233	33/83/250	33/100/200	33/100/250	66/100/200	66/100/250		
Typical—GV_{DD}	300			900			mW	7, 9

Notes:

1. The values include V_{DD}, AV_{DD}, $AV_{DD}2$, and LAV_{DD} but do not include I/O supply power; see Section 1.7.2, "Power Supply Sizing," in the *MPC8240 Integrated Processor Hardware Specifications* for information on OV_{DD} and GV_{DD} supply power. One DIMM is used for memory loading.
2. Maximum—FP power is measured at V_{DD} = 2.625 V with dynamic power management enabled while running an entirely cache-resident, looping, floating point multiplication instruction.
3. Maximum—INT power is measured at V_{DD} = 2.625 V with dynamic power management enabled while running entirely cache-resident, looping, integer instructions.
4. Power saving mode maximums are measured at V_{DD} = 2.625 V while the device is in doze, nap, or sleep mode.
5. Typical power is measured at V_{DD} = AV_{DD} = 2.625 V, OV_{DD} = 3.3 V where a nominal FP value, a nominal INT value, and a value where there is a continuous flush of cache lines with alternating ones and zeros on 64-bit boundaries to local memory are averaged.
6. Power saving mode data measured with only two PCI_CLKs and two SDRAM_CLKs enabled.
7. The typical minimum I/O power values were results of the MPC8240 performing cache resident integer operations at the slowest frequency combination of 33:66:166 (PCI:Mem:CPU) MHz.
8. The typical maximum OV_{DD} value resulted from the MPC8240 operating at the fastest frequency combination of 66:100:250 (PCI:Mem:CPU) MHz and performing continuous flushes of cache lines with alternating ones and zeros to PCI memory.
9. The typical maximum GV_{DD} value resulted from the MPC8240 operating at the fastest frequency combination of 66:100:250 (PCI:Mem:CPU) MHz and performing continuous flushes of cache lines with alternating ones and zeros on 64-bit boundaries to local memory.

1.5 PLL Configurations

The MPC8240 internal PLLs are configured by the PLL_CFG[0:4] signals. For a given PCI_SYNC_IN (PCI bus) frequency, the PLL configuration signals set both the peripheral logic/memory bus PLL (VCO) frequency of operation for the PCI-to-memory frequency multiplying and the MPC603e CPU PLL (VCO) frequency of operation for memory-to-CPU frequency multiplying. The PLL configurations for the MPC8240 is shown in Table 18.

Table 18. MPC8240 Microprocessor PLL Configurations

Ref. No.	PLL_CFG [0:4] [2]	CPU [1] HID1[0:4]	250-MHz Part [8, 9]			Ratios [3, 4]	
			PCI Clock Input (PCI_SYNC_IN) Range (MHz)	Peripheral Logic/Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI to Mem (Mem VCO) Multiplier	Mem to CPU (CPU VCO) Multiplier
0	00000	00110	25–33	75–100	188–250	3 (6)	2.5 (5)
1	00001	11000	25–27	75–83	225–250	3 (6)	3 (6)
2	00010	00101	50–56 [5]	50–56	100–112	1 (4)	2 (8)
3	00011	00101	Bypass			Bypass	2 (8)
4	00100	00101	25–28 [5]	50–56	100–113	2 (8)	2 (8)

Table 18. MPC8240 Microprocessor PLL Configurations (continued)

Ref. No.	PLL_CFG [0:4] [2]	CPU [1] HID1[0:4]	250-MHz Part [8, 9]			Ratios [3, 4]	
			PCI Clock Input (PCI_SYNC_IN) Range (MHz)	Peripheral Logic/Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI to Mem (Mem VCO) Multiplier	Mem to CPU (CPU VCO) Multiplier
5	00101	00110	Bypass			Bypass	2.5 (5)
7	00111	11000	Bypass			Bypass	3 (6)
8	01000	11000	33 [6]–56 [5]	33–56	100–168	1 (4)	3 (6)
A	01010	00111	25–27	50–55	225–250	2 (4)	4.5 (9)
C	01100	00110	25–50	50–100	125–250	2 (4)	2.5 (5)
E	01110	11000	25–41	50–83	150–250	2 (4)	3 (6)
10	10000	00100	25–33	75–100	150–200	3 (6)	2 (4)
12	10010	00100	33–66	50–100	100–200	1.5 (3)	2 (4)
14	10100	11110	25–35	50–71	175–250	2 (4)	3.5 (7)
16	10110	11010	25–31	50–62	200–250	2 (4)	4 (8)
18	11000	11000	25–33	62–83	186–250	2.5 (5)	3 (6)
1A	11010	11010	50 [7]–62	50–62	200–250	1 (2)	4 (8)
1C	11100	11000	33 [7]–55	50–83	150–250	1.5 (3)	3 (6)
1D	11101	00110	33 [7]–66	50–100	125–250	1.5 (3)	2.5 (5)
1E	11110	01111	Not usable			Off	Off
1F	11111	11111				Off	Off

Notes:

1. The processor HID1 values only represent the multiplier of the processor's PLL (memory-to-processor multiplier); thus, multiple MPC8240 PLL_CFG[0:4] values may have the same processor HID1 value. This implies that system software cannot read the HID1 register and associate it with a unique PLL_CFG[0:4] value.
2. PLL_CFG[0:4] settings not listed (00110, 01001, 01011, 01101, 01111, 10001, 10011, 10101, 10111, 11001, and 11011) are reserved.
3. In PLL bypass mode, the PCI_SYNC_IN input signal clocks the internal processor directly, the peripheral logic PLL is disabled, and the bus mode is set for 1:1 (PCI:Mem) mode operation. This mode is intended for hardware modeling support. The AC timing specifications given in this document do not apply in PLL bypass mode.
4. In clock-off mode, no clocking occurs inside the MPC8240 regardless of the PCI_SYNC_IN input.
5. Limited due to maximum memory VCO = 225 MHz.
6. Limited due to minimum CPU VCO = 200 MHz.
7. Limited due to minimum memory VCO = 100 MHz.
8. For clarity, range values are shown rounded down to the nearest whole number (decimal place accuracy removed).
9. Note that the 250-MHz part is available only in the XPC8240RZU*nnnx* number series.

1.9 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in Section 1.9.1, "Part Numbers Fully Addressed by This Document."

1.9.1 Part Numbers Fully Addressed by This Document

Table 19 provides the Freescale part numbering nomenclature for the MPC8240. Note that the individual part numbers correspond to the maximum processor core frequency. For available frequencies, contact a local Freescale sales office. Each part number also contains a revision code that refers to the die mask revision number. The revision level can be determined by reading the Revision ID register at address offset 0x08.

Table 19. Freescale Part Numbering Nomenclature

XPC	*nnnn*	*x*	*xx*	*nnn*	*x*
Product Code	**Part Identifier**	**Process Descriptor**	**Package**	**Processor Frequency**	**Revision Level**
XPC	8240	R=2.625 V ±125 mV 0° to 105°C	ZU = TBGA V V = Lead free TBGA	250	E: 1.3; Revision ID = 0x13

1.9.2 Part Marking

Parts are marked as in the example shown in Figure 28.

Notes:
MMMMMM is the 6-digit mask number.
ATWLYYWWA is the traceability code.

Figure 28. Freescale Part Marking for TBGA Device

Document Revision History

Table B provides a revision history for this part number specification.

Table B. Document Revision History

Revision Number	Substantive Change(s)
0	Initial release. Note that this document supercedes the MPC8245RZUPNS.

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