Excellent Integrated System Limited

Stocking Distributor

Click to view price, real time Inventory, Delivery & Lifecycle Information:

Fairchild Semiconductor
74ABT16646CMTD

For any questions, you can email us directly:
sales@integrated-circuit.com

FAIRCHILD SEMICONDUCTOR™

October 1993
Revised November 1999

74ABT16646
16-Bit Transceivers and Registers with 3-STATE Outputs

General Description

The ABT16646 consists of bus transceiver circuits with 3-STATE, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a high logic level. Control $\overline{OE}$ and direction pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or the B register or in both. The select controls can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when the enable control $\overline{OE}$ is Active LOW. In the isolation mode (control $\overline{OE}$ HIGH), A data may be stored in the B register and/or B data may be stored in the A register.

Features

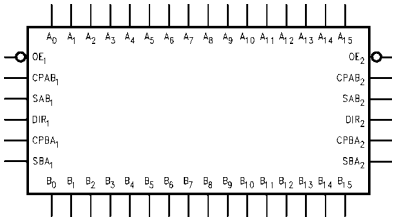
- Independent registers for A and B buses
- Multiplexed real-time and stored data
- A and B output sink capability of 64 mA, source capability of 32 mA
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability

Ordering Code:

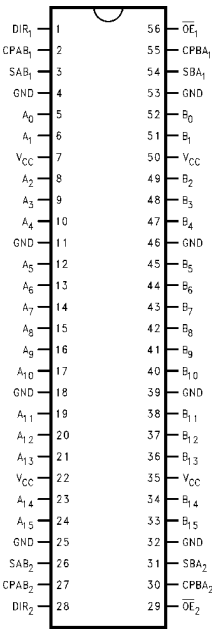
Order Number	Package Number	Package Description
74ABT16646CSSC	MS56A	56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74ABT16646CMTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description
A_0–A_{15}	Data Register A Inputs/ 3-STATE Outputs
B_0–B_{15}	Data Register B Inputs/ 3-STATE Outputs
$CPAB_n$, $CPBA_n$	Clock Pulse Inputs
SAB_n, SBA_n	Select Inputs
$\overline{OE}_n$	Output Enable Input
DIR	Direction Control Input

Function Table

Inputs						Data I/O (Note 1)		Output Operation Mode
$\overline{OE}_1$	DIR_1	$CPAB_1$	$CPBA_1$	SAB_1	SBA_1	A_{0-7}	B_{0-7}	
H	X	H or L	H or L	X	X			Isolation
H	X	↑	X	X	X	Input	Input	Clock An Data into A Register
H	X	X	↑	X	X			Clock Bn Data Into B Register
L	H	X	X	L	X			An to Bn—Real Time (Transparent Mode)
L	H	↑	X	L	X	Input	Output	Clock An Data to A Register
L	H	H or L	X	H	X			A Register to Bn (Stored Mode)
L	H	↑	X	H	X			Clock An Data into A Register and Output to Bn
L	L	X	X	X	L			Bn to An—Real Time (Transparent Mode)
L	L	X	↑	X	L	Output	Input	Clock Bn Data into B Register
L	L	X	H or L	X	H			B Register to An (Stored Mode)
L	L	X	↑	X	H			Clock Bn into B Register and Output to An

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↑ = LOW-to-HIGH Transition

Note 1: The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs. Also applies to data I/O (A and B: 8-15) and #2 control pins.

Real Time Transfer A-Bus to B-Bus

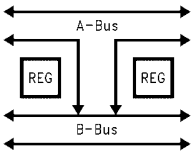


FIGURE 1.

Real Time Transfer B-Bus to A-Bus

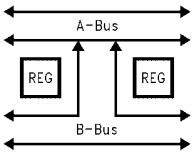


FIGURE 2.

Storage from Bus to Register

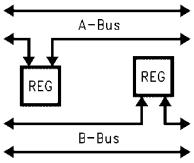


FIGURE 3.

Transfer from Register to Bus

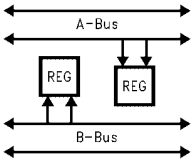
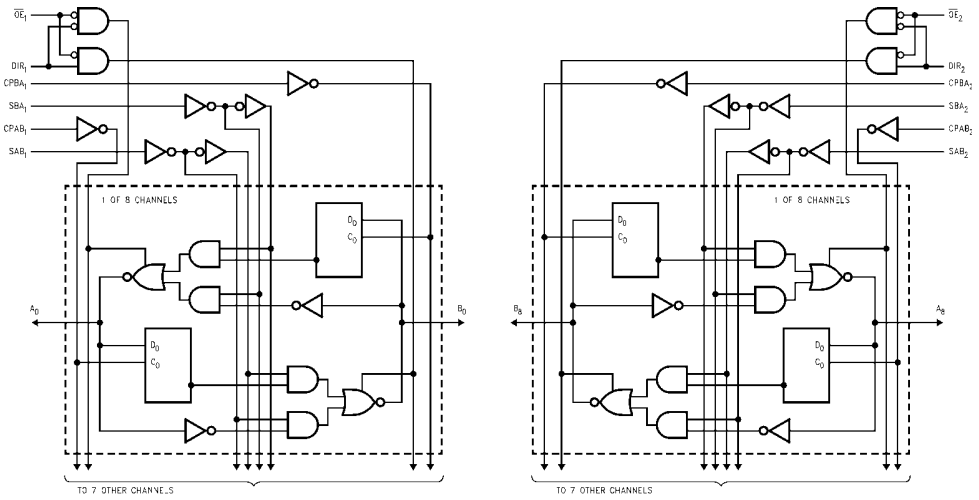


FIGURE 4.

Logic Diagram



Absolute Maximum Ratings(Note 2)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 3)	−0.5V to +7.0V
Input Current (Note 3)	−30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disable or	
Power-Off State	−0.5V to +5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V

Recommended Operating Conditions

Free Air Ambient Temperature	−40°C to +85°C
Supply Voltage	+4.5V to +5.5V
Minimum Input Edge Rate (ΔV/Δt)	
Data Input	50 mV/ns
Enable Input	20 mV/ns
Clock Input	100 mV/ns

Note 2: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 3: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA (Non I/O Pins)
V_{OH}	Output HIGH Voltage	2.5 2.0					I_{OH} = −3 mA, (A_n, B_n) I_{OH} = −32 mA, (A_n, B_n)
V_{OL}	Output LOW Voltage			0.55	V	Min	I_{OL} = 64 mA, (A_n, B_n)
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 µA, (Non-I/O Pins) All Other Pins Grounded
I_{IH}	Input HIGH Current			1 1	µA	Max	V_{IN} = 2.7V (Non-I/O Pins) (Note 5) V_{IN} = V_{CC} (Non-I/O Pins)
I_{BVI}	Input HIGH Current Breakdown Test			7	µA	Max	V_{IN} = 7.0V (Non-I/O Pins)
I_{BVIT}	Input HIGH Current Breakdown Test (I/O)			100	µA	Max	V_{IN} = 5.5V (A_n, B_n)
I_{IL}	Input LOW Current			−1 −1	µA	Max	V_{IN} = 0.5V (Non-I/O Pins) (Note 5) V_{IN} = 0.0V (Non-I/O Pins)
I_{IH} + I_{OZH}	Output Leakage Current			10	µA	0V–5.5V	V_{OUT} = 2.7V (A_n, B_n); $\overline{OE}$ = 2.0V
I_{IL} + I_{OZL}	Output Leakage Current			−10	µA	0V–5.5V	V_{OUT} = 0.5V (A_n, B_n); $\overline{OE}$ = 2.0V
I_{OS}	Output Short-Circuit Current	−100		−275	mA	Max	V_{OUT} = 0V (A_n, B_n)
I_{CEX}	Output HIGH Leakage Current			50	µA	Max	V_{OUT} = V_{CC} (A_n, B_n)
I_{ZZ}	Bus Drainage Test			100	µA	0.0V	V_{OUT} = 5.5V (A_n, B_n); All Others GND
I_{CCH}	Power Supply Current			1.0	mA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current			60	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current			1.0	mA	Max	Outputs 3-STATE; All Others GND
I_{CCT}	Additional I_{CC}/Input			2.5	mA	Max	V_I = V_{CC} − 2.1V All Other Outputs at V_{CC} or GND
I_{CCD}	Dynamic I_{CC} No Load (Note 5)			0.23	mA/ MHz	Max	Outputs OPEN $\overline{OE}$, DIR, and SEL = GND, Non-I/O = GND or V_{CC}(Note 4) One Bit toggling, 50% duty cycle

Note 4: For 8-bit toggling, I_{CCD} < 1.4 mA/MHz.

Note 5: Guaranteed but not tested.

DC Electrical Characteristics

(SSOP Package)

Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions C_L = 50 pF, R_L = 500Ω
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}		0.7	1.2	V	5.0	T_A = 25°C (Note 6)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	–1.4	–1.0		V	5.0	T_A = 25°C (Note 6)
V_{OHV}	Minimum HIGH Level Dynamic Output Voltage	2.5	3.0		V	5.0	T_A = 25° (Note 7)
V_{IHD}	Minimum HIGH Level Dynamic Input Voltage	2.2	1.6		V	5.0	T_A = 25°C (Note 8)
V_{ILD}	Maximum LOW Level Dynamic Input Voltage		1.2	0.8	V	5.0	T_A = 25°C (Note 8)

Note 6: Max number of outputs defined as (n). n – 1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.

Note 7: Max number of outputs defined as (n). n – 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.

Note 8: Max number of data inputs (n) switching. n – 1 inputs switching 0V to 3V. Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}). Guaranteed, but not tested.

AC Electrical Characteristics

(SSOP Package)

Symbol	Parameter	T_A = +25°C, V_{CC} = +5.0V, C_L = 50 pF			T_A = –40°C to +85°C, V_{CC} = 4.5V–5.5V, C_L = 50 pF		Units
		Min	Typ	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		200				MHz
t_{PLH}	Propagation Delay	1.5	3.0	4.9	1.5	4.9	ns
t_{PHL}	Clock to Bus	1.5	3.4	4.9	1.5	4.9	
t_{PLH}	Propagation Delay	1.5	2.6	4.5	1.5	4.5	ns
t_{PHL}	Bus to Bus	1.5	3.0	4.5	1.5	4.5	
t_{PLH}	Propagation Delay	1.5	2.9	5.0	1.5	5.0	ns
t_{PHL}	SBA_n or SAB_n to A_n to B_n	1.5	3.2	5.0	1.5	5.0	
t_{PZH}	Enable Time	1.5	2.8	5.5	1.5	5.5	ns
t_{PZL}	$\overline{OE}_n$ to A_n or B_n	1.5	3.0	5.5	1.5	5.5	
t_{PHZ}	Disable Time	1.5	3.9	6.0	1.5	6.0	ns
t_{PLZ}	$\overline{OE}_n$ to A_n or B_n	1.5	3.2	6.0	1.5	6.0	
t_{PZH}	Enable Time	1.5	3.5	5.5	1.5	5.5	ns
t_{PZL}	DIR_n to A_n or B_n	1.5	3.2	5.5	1.5	5.5	
t_{PHZ}	Disable Time	1.5	3.8	6.5	1.5	6.5	ns
t_{PLZ}	DIR_n to A_n or B_n	1.5	3.2	6.5	1.5	6.5	

AC Operating Requirements

Symbol	Parameter	T_A = +25°C, V_{CC} = +5.0V, C_L = 50 pF		T_A = –40°C to +85°C, V_{CC} = 4.5V–5.5V, C_L = 50 pF		Units
		Min	Max	Min	Max	
t_S(H)	Setup Time, HIGH	2.0		2.0		ns
t_S(L)	or LOW Bus to Clock					
t_H(H)	Hold Time, HIGH	1.0		1.0		ns
t_H(L)	or LOW Bus to Clock					
t_W(H)	Pulse Width,	3.0		3.0		ns
t_W(L)	HIGH or LOW					

Extended AC Electrical Characteristics

(SSOP Package)

Symbol	Parameter	$T_A = -40°C$ to $+85°C$ $V_{CC} = 4.5V–5.5V$ $C_L = 50$ pF 8 Outputs Switching (Note 9)		$T_A = -40°C$ to $+85°C$ $V_{CC} = 4.5V–5.5V$ $C_L = 250$ pF 1 Output Switching (Note 10)		$T_A = -40°C$ to $+85°C$ $V_{CC} = 4.5V–5.5V$ $C_L = 250$ pF 8 Outputs Switching (Note 11)		Units
		Min	Max	Min	Max	Min	Max	
t_{PLH}	Propagation Delay	1.5	5.8	2.0	7.5	2.5	10.0	ns
t_{PHL}	Clock to Bus	1.5	5.8	2.0	7.5	2.5	10.0	
t_{PLH}	Propagation Delay	1.5	6.5	2.0	7.0	2.5	9.5	ns
t_{PHL}	Bus to Bus	1.5	6.5	2.0	7.0	2.5	9.5	
t_{PLH}	Progagation Delay	1.5	6.0	2.0	7.5	2.5	10.0	ns
t_{PHL}	SBA_n or SAB_n to A_n or B_n	1.5	6.0	2.0	7.5	2.5	10.0	
t_{PZH}	Output Enable Time	1.5	6.0	2.0	8.0	2.5	10.5	ns
t_{PZL}	$\overline{OE}_n$ to A_n or B_n	1.5	6.0	2.0	8.0	2.5	10.5	
t_{PHZ}	Output Disable Time	1.5	6.0	(Note 12)		(Note 12)		ns
t_{PLZ}	$\overline{OE}_n$ to A_n or B_n	1.5	6.0					
t_{PZH}	Output Enable Time	1.5	6.5	2.0	8.0	2.5	10.5	ns
t_{PZL}	DIR to A_n or B_n	1.5	6.5	2.0	8.0	2.5	10.5	
t_{PHZ}	Output Disable Time	1.5	6.5	(Note 12)		(Note 12)		ns
t_{PLZ}	DIR to A_n or B_n	1.5	6.5					

Note 9: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).

Note 10: This specification is guaranteed but not tested. The limits represent propagation delay with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Note 11: This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.) with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Note 12: The 3-STATE delays are dominated by the RC network (500Ω, 250 pF) on the output and has been excluded from the datasheet.

Skew

(SOIC Package)

Symbol	Parameter	$T_A = -40°C$ to $+85°C$ $V_{CC} = 4.5V–5.5V$ $C_L = 50$ pF 16 Outputs Switching (Note 13) Max	$T_A = -40°C$ to $+85°C$ $V_{CC} = 4.5V–5.5V$ $C_L = 250$ pF 16 Outputs Switching (Note 14) Max	Units
t_{OSHL} (Note 15)	Pin to Pin Skew HL Transitions	2.0	2.5	ns
t_{OSLH} (Note 15)	Pin to Pin Skew LH Transitions	2.0	2.5	ns
t_{PS} (Note 16)	Duty Cycle LH–HL Skew	2.0	2.5	
t_{OST} (Note 15)	Pin to Pin Skew LH/HL Transitions	2.8	3.0	ns
t_{PV} (Note 17)	Device to Device Skew LH/HL Transitions	3.5	4.0	ns

Note 13: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).

Note 14: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Note 15: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW (t_{OST}). This specification is guaranteed but not tested.

Note 16: This describes the difference between the delay of the LOW-to-HIGH and the HIGH-to-LOW transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested.

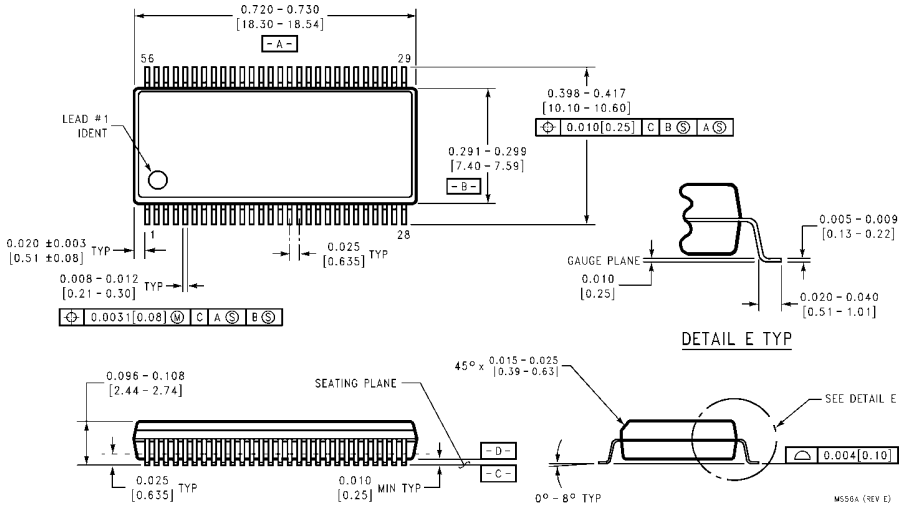
Note 17: Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device. This specification is guaranteed but not tested.

Capacitance

Symbol	Parameter	Typ	Units	Conditions $T_A = 25°C$
C_{IN}	Input Capacitance	5	pF	$V_{CC} = 0V$ (non I/O pins)
$C_{I/O}$ (Note 18)	Output Capacitance	11	pF	$V_{CC} = 5.0V$ (A_n, B_n)

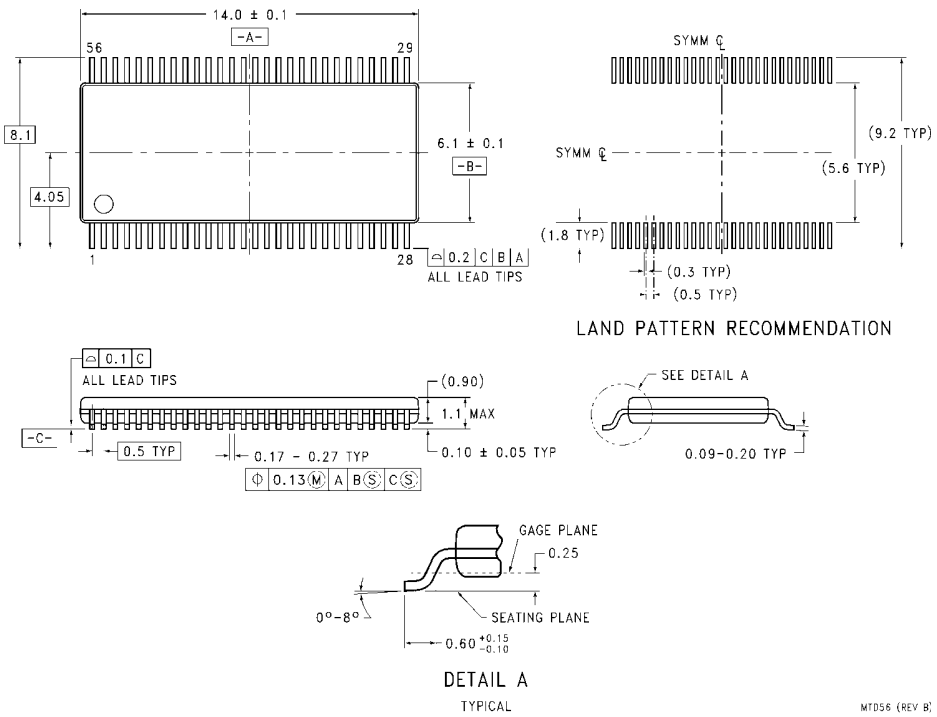
Note 18: $C_{I/O}$ is measured at frequency, f = 1 MHz, per MIL-STD-883, Method 3012.

Physical Dimensions inches (millimeters) unless otherwise noted



56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
Package Number MS56A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD56

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com