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November 2001
 Revised November 2001

74ALVC162827

Low Voltage 20-Bit Buffer/Line Driver with 3.6V Tolerant Inputs and Outputs and 26Ω Series Resistors in the Outputs

General Description

The ALVC162827 contains twenty non-inverting buffers with 3-STATE outputs to be employed as a memory and address driver, clock driver, or bus oriented transmitter/receiver. The device is byte controlled. Each byte has NOR output enables for maximum control flexibility.

The 74ALVC162827 is designed for low voltage (1.65V to 3.6V) V_{CC} applications with I/O capability up to 3.6V. The ALVC162827 is also designed with 26Ω resistors in the outputs.

The 74ALVC162827 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

Features

- 1.65V to 3.6V V_{CC} supply operation
- 3.6V tolerant inputs and outputs
- 26Ω series resistors in outputs
- t_{PD}
 - 3.9 ns max for 3.0V to 3.6V V_{CC}
 - 4.6 ns max for 2.3V to 2.7V V_{CC}
 - 8.2 ns max for 1.65V to 1.95V V_{CC}
- Power-off high impedance inputs and outputs
- Supports live insertion and withdrawal (Note 1)
- Uses patented noise/EMI reduction circuitry
- Latchup conforms to JEDEC JED78
- ESD performance:
 - Human body model > 2000V
 - Machine model > 200V

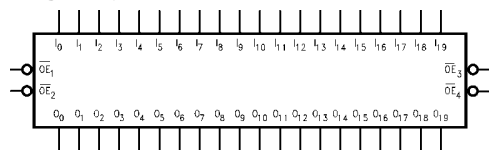
Note 1: To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Ordering Code:

Order Number	Package Number	Package Description
74ALVC162827T	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix "X" to the ordering code.

Logic Symbol

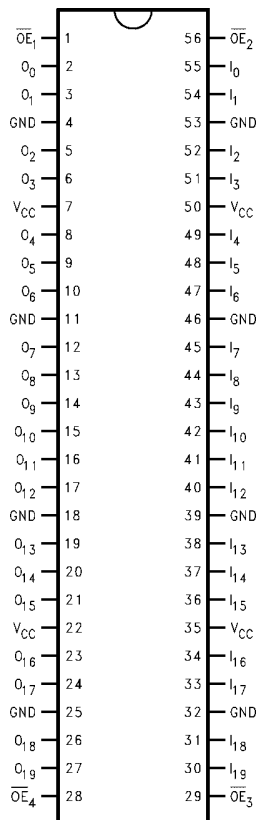


Pin Descriptions

Pin Names	Description
\overline{OE}_n	Output Enable Input (Active LOW)
I_0 - I_{19}	Inputs
O_0 - O_{19}	Outputs

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Connection Diagram



Truth Tables

Inputs			Outputs
\overline{OE}_1	\overline{OE}_2	I_0-I_9	O_0-O_9
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

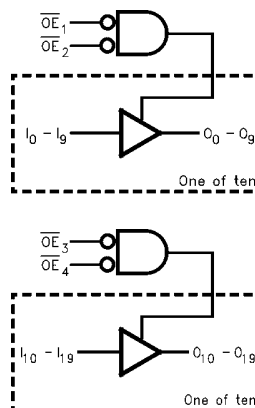
Inputs			Outputs
\overline{OE}_3	\overline{OE}_4	$I_{10}-I_{19}$	$O_{10}-O_{19}$
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial (HIGH or LOW, inputs may not float)
 Z = High Impedance

Functional Description

The 74ALVC162827 contains twenty non-inverting buffers with 3-STATE outputs. The device is byte controlled with each byte functioning identically, but independent of each other. The control pins may be shorted together to obtain full 20-bit operation. The 3-STATE outputs are controlled by Output Enable (\overline{OE}_i) inputs. When \overline{OE}_1 and \overline{OE}_2 are LOW, O_0-O_{10} are in the 2-state mode. When either \overline{OE}_1 or \overline{OE}_2 are HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the inputs. The same applies for byte two with \overline{OE}_3 and \overline{OE}_4 .

Logic Diagrams



Absolute Maximum Ratings (Note 2)		Recommended Operating Conditions (Note 4)	
Supply Voltage (V_{CC})	-0.5V to +4.6V	Power Supply	
DC Input Voltage (V_I)	-0.5V to 4.6V	Operating	1.65V to 3.6V
Output Voltage (V_O) (Note 3)	-0.5V to $V_{CC} + 0.5V$	Input Voltage	0V to V_{CC}
DC Input Diode Current (I_{IK})		Output Voltage (V_O)	0V to V_{CC}
$V_I < 0V$	-50 mA	Free Air Operating Temperature (T_A)	-40°C to +85°C
DC Output Diode Current (I_{OK})		Minimum Input Edge Rate ($\Delta t/\Delta V$)	
$V_O < 0V$	-50 mA	$V_{IN} = 0.8V$ to 2.0V, $V_{CC} = 3.0V$	10 ns/V
DC Output Source/Sink Current (I_{OH}/I_{OL})	±50 mA	Note 2: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.	
DC V_{CC} or GND Current per Supply Pin (I_{CC} or GND)	±100 mA	Note 3: I_O Absolute Maximum Rating must be observed.	
Storage Temperature Range (T_{STG})	-65°C to +150°C	Note 4: Floating or unused control inputs must be held HIGH or LOW.	

DC Electrical Characteristics						
Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{IH}	HIGH Level Input Voltage		1.65 - 1.95 2.3 - 2.7 2.7 - 3.6	0.65 x V_{CC} 1.7 2.0		V
V_{IL}	LOW Level Input Voltage		1.65 - 1.95 2.3 - 2.7 2.7 - 3.6		0.35 x V_{CC} 0.7 0.8	V
V_{OH}	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$	1.65 - 3.6	$V_{CC} - 0.2$		V
		$I_{OH} = -2 \text{ mA}$	1.65	1.2		
		$I_{OH} = -4 \text{ mA}$	2.3	1.9		
		$I_{OH} = -6 \text{ mA}$	2.3	1.7		
			3	2.4		
			2.7	2		
V_{OL}	LOW Level Output Voltage	$I_{OL} = 100 \mu A$	1.65 - 3.6		0.2	V
		$I_{OL} = 2 \text{ mA}$	1.65		0.45	
		$I_{OL} = 4 \text{ mA}$	2.3		0.4	
		$I_{OL} = 6 \text{ mA}$	2.3		0.55	
			3		0.55	
			2.7		0.6	
		3		0.8		
I_I	Input Leakage Current	$0 \leq V_I \leq 3.6V$	3.6		±5.0	μA
I_{OZ}	3-STATE Output Leakage	$0 \leq V_O \leq 3.6V$	3.6		±10	μA
I_{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6		40	μA
ΔI_{CC}	Increase in I_{CC} per Input	$V_{IH} = V_{CC} - 0.6V$	3 - 3.6		750	μA

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AC Electrical Characteristics										
Symbol	Parameter	T _A = -40°C to +85°C, R _L = 500Ω								Units
		C _L = 50 pF				C _L = 30 pF				
		V _{CC} = 3.3V ± 0.3V		V _{CC} = 2.7V		V _{CC} = 2.5V ± 0.2V		V _{CC} = 1.8V ± 0.15V		
		Min	Max	Min	Max	Min	Max	Min	Max	
t _{PHL} , t _{PL}	Propagation Delay Bus to Bus	1.3	3.9	1.5	4.6	1.0	4.1	1.5	8.2	ns
t _{PZL} , t _{PZH}	Output Enable Time	1.3	4.8	1.5	5.4	1.0	5.9	1.5	9.8	ns
t _{PLZ} , t _{PHZ}	Output Disable Time	1.3	4.8	1.5	5.4	1.0	4.9	1.5	8.8	ns
Capacitance										
Symbol	Parameter	Conditions	T _A = +25°C		Units					
			V _{CC}	Typical						
C _{IN}	Input Capacitance	V _I = 0V or V _{CC}	3.3	6	pF					
C _{OUT}	Output Capacitance	V _I = 0V or V _{CC}	3.3	7	pF					
C _{PD}	Power Dissipation Capacitance	Outputs Enabled	f = 10 MHz, C _L = 50 pF	3.3	20	pF				
				2.5	20					

AC Loading and Waveforms

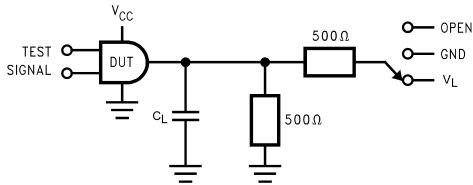


TABLE 1. Values for Figure 1

TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	V_L
t_{PZH}, t_{PHZ}	GND

FIGURE 1. AC Test Circuit

TABLE 2. Variable Matrix
(Input Characteristics: $f = 1\text{MHz}$; $t_r = t_f = 2\text{ns}$; $Z_0 = 50\Omega$)

Symbol	V_{CC}			
	$3.3V \pm 0.3V$	$2.7V$	$2.5V \pm 0.2V$	$1.8V \pm 0.15V$
V_{mi}	1.5V	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_{mo}	1.5V	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_X	$V_{OL} + 0.3V$	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$	$V_{OL} + 0.15V$
V_Y	$V_{OH} - 0.3V$	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$	$V_{OH} - 0.15V$
V_L	6V	6V	$V_{CC} * 2$	$V_{CC} * 2$

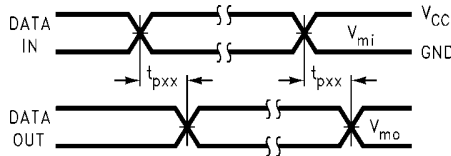


FIGURE 2. Waveform for Inverting and Non-Inverting Functions

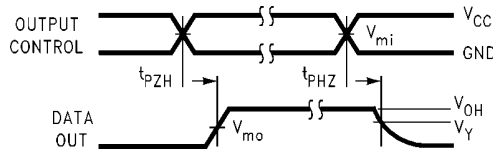


FIGURE 3. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

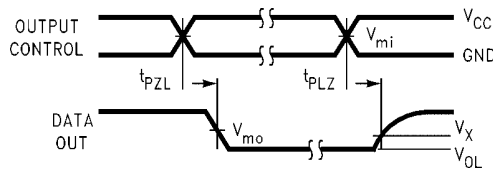


FIGURE 4. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

74ALVC162827 Low Voltage 20-Bit Buffer/Line Driver with 3.6V Tolerant Inputs and Outputs and 26Ω Series Resistors in the Outputs

Physical Dimensions inches (millimeters) unless otherwise noted

56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
 Package Number MTD56

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