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Fairchild Semiconductor
74LCX112M

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FAIRCHILD SEMICONDUCTOR™

June 1998
Revised February 2001

74LCX112
Low Voltage Dual J-K Negative Edge-Triggered Flip-Flop with 5V Tolerant Inputs

General Description

The LCX112 is a dual J-K flip-flop. Each flip-flop has independent J, K, PRESET, CLEAR, and CLOCK inputs with Q, $\overline{Q}$ outputs. These devices are edge sensitive and change state on the negative going transition of the clock pulse. Clear and preset are independent of the clock and accomplished by a low logic level on the corresponding input. LCX devices are designed for low voltage (3.3V or 2.5) operation with the added capability of interfacing to a 5V signal environment.

The 74LCX112 is fabricated with advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

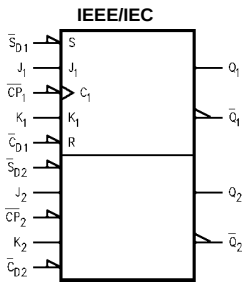
- 5V tolerant inputs
- 2.3V–3.6V V_{CC} specifications provided
- 7.5 ns t_{PD} max (V_{CC} = 3.3V), 10 µA I_{CC} max
- Power down high impedance inputs and outputs
- ±24 mA output drive (V_{CC} = 3.0V)
- Implements patented noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA
- ESD performance:
  - Human body model > 2000V
  - Machine model > 2000V

Ordering Code:

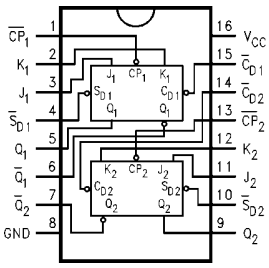
Order Number	Package Number	Package Description
74LCX112M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
74LCX112SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LCX112MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description
J_1, J_2, K_1, K_2	Data Inputs
$\overline{CP}_1$, $\overline{CP}_2$	Clock Pulse Inputs (Active Falling Edge)
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs (Active LOW)
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs (Active LOW)
Q_1, Q_2, $\overline{Q}_1$, $\overline{Q}_2$	Outputs

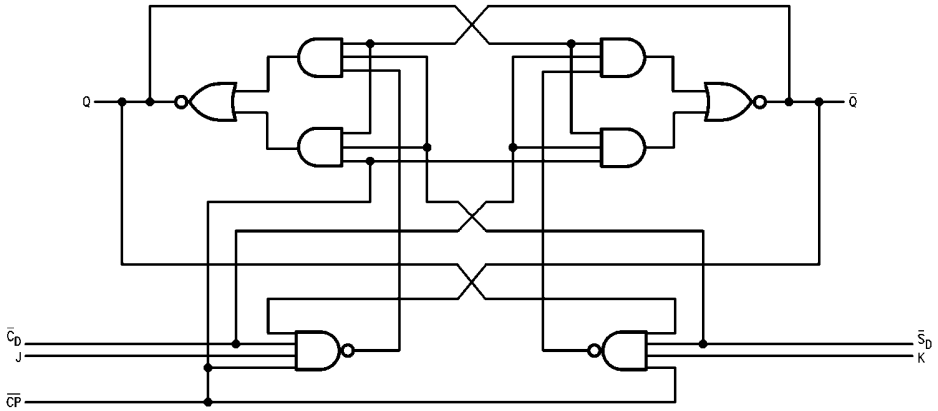
Truth Table

(Each half)

Inputs					Outputs	
$\overline{S}_D$	$\overline{C}_D$	$\overline{CP}$	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H	H
H	H	⌐	h	h	$\overline{Q}_O$	Q_O
H	H	⌐	l	h	L	H
H	H	⌐	h	l	H	L
H	H	⌐	l	l	Q_O	$\overline{Q}_O$
H	H	H	X	X	Q_O	$\overline{Q}_O$

H(h) = HIGH Voltage Level
L(l) = LOW Voltage Level
X = Immaterial
⌐ = HIGH-to-LOW Clock Transition
$Q_O(\overline{Q}_O)$ = Before HIGH-to-LOW Transition of Clock
Lower case letters indicate the state of the referenced input or output one setup time prior to the HIGH-to-LOW clock transition.

Logic Diagram



Absolute Maximum Ratings(Note 1)

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	Output in HIGH or LOW State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supple Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to 150		°C

Recommended Operating Conditions (Note 3)

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V − 3.6V		±24	mA
		V_{CC} = 2.7V − 3.0V		±12	
		V_{CC} = 2.3V − 2.7V		±8	
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum rating must be observed.

Note 3: Unused Inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.3 – 2.7	1.7		V
			2.7 – 3.6	2.0		
V_{IL}	LOW Level Input Voltage		2.3 – 2.7		0.7	V
			2.7 – 3.6		0.8	
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100µA	2.3 – 3.6	V_{CC} - 0.2	0.7	V
		I_{OH} = -8 mA	2.3	1.8		
		I_{OH} = −12 mA	2.7	2.2		
		I_{OH} = −18 mA	3.0	2.4		
		I_{OH} = −24 mA	3.0	2.2		
V_{OL}	LOW Level Output Voltage	I_{OL} = 100µA	2.3 – 3.6		0.6	V
		I_{OL} = 8mA	2.3		0.2	
		I_{OL} = 12 mA	2.7		0.4	
		I_{OL} = 16 mA	3.0		0.4	
		I_{OL} = 24 mA	3.0		0.55	
I_I	Input Leakage Current	0 ≤ I_I ≤ 5.5V	2.3 – 3.6		±5.0	µA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	µA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.3 – 3.6		10	µA
		3.6V ≤ V_I ≤ 5.5V	2.3 – 3.6		±10	µA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.3 – 3.6		500	µA

AC Electrical Characteristics

Symbol	Parameters	$T_A = 40°C$ to $85°C$, $R_L = 500\Omega$						Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		$V_{CC} = 2.5V \pm 0.2V$		
		C_L=50 pF		C_L = 50 pF		C_L=30 pF		
		Min	Max	Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	150		150		150		MHz
t_{PHL}	Propagation Delay	1.5	7.5	1.5	8.0	1.5	9.0	ns
t_{PLH}	$\overline{CP}_n$ to Q_n or $\overline{Q}_n$	1.5	7.5	1.5	8.0	1.5	9.0	
t_{PHL}	Propagation Delay	1.5	7.0	1.5	8.0	1.5	8.4	ns
t_{PLH}	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	1.5	7.0	1.7	8.0	1.5	8.4	
t_S	Setup Time	2.5		2.5		4.0		ns
t_H	Hold Time	1.5		1.5		2.0		ns
t_W	Pulse Width $\overline{CP}$	3.3		3.3		4.0		ns
t_W	Pulse Width ($\overline{C}_D$, $\overline{S}_D$)	3.3		3.3		4.0		ns
t_{REC}	Recovery Time	2.0		2.5		4.5		ns
t_{OSHL}	Output to Output Skew		1.0					ns
t_{OSLH}	(Note 4)		1.0					

Note 4: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}), or LOW-to-HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$ Typical	Units
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	C_L = 50 pF, V_{IH} = 3.3V, V_{IL} = 0V	3.3	0.8	V
		C_L = 30 pF, V_{IH} = 2.5V, V_{IL} = 0V	2.5	0.6	
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	C_L = 50 pF, V_{IH} = 3.3V, V_{IL} = 0V	3.3	−0.8	V
		C_L = 30 pF, V_{IH} = 2.5V, V_{IL} = 0V	2.5	−0.6	

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, V_I = 0V or V_{CC}	7	pF
C_{OUT}	Output Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}, f = 10 MHz	25	pF

AC Loading and Waveforms Generic for LCX Family

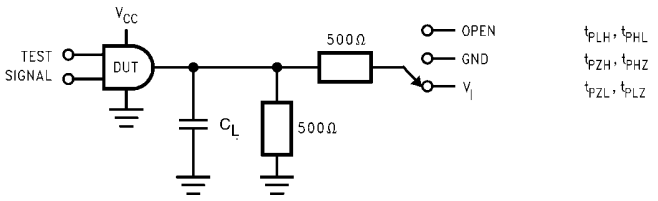
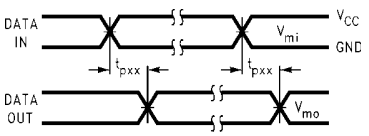
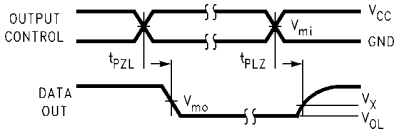


FIGURE 1. AC Test Circuit
(C_L includes probe and jig capacitance)

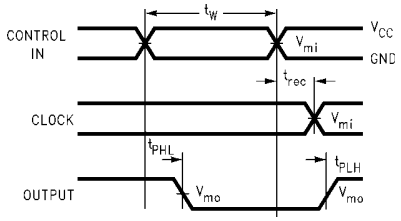
Test	Switch
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V at V_{CC} = 3.3 ± 0.3V V_{CC} x 2 at V_{CC} = 2.5 ± 0.2V
t_{PZH},t_{PHZ}	GND



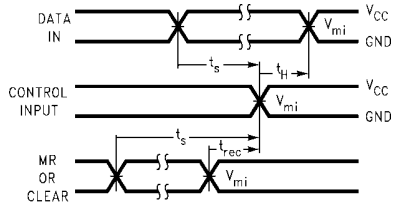
Waveform for Inverting and Non-Inverting Functions



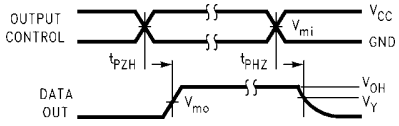
3-STATE Output Low Enable and Disable Times for Logic



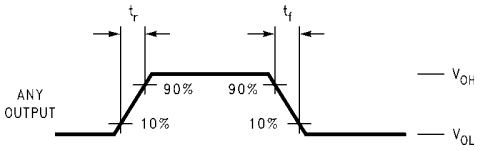
Propagation Delay, Pulse Width and t_{rec} Waveforms



Setup Time, Hold TIme and Recovery TIme for Logic



3-STATE Output High Enable and Disable TImes for Logic

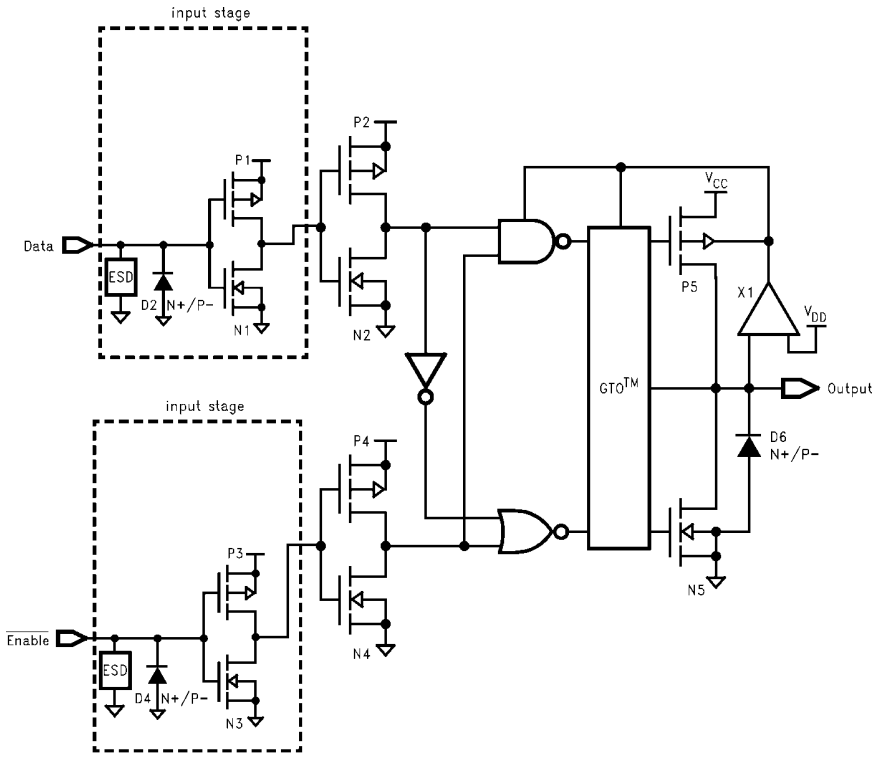


t_{rise} and t_{fall}

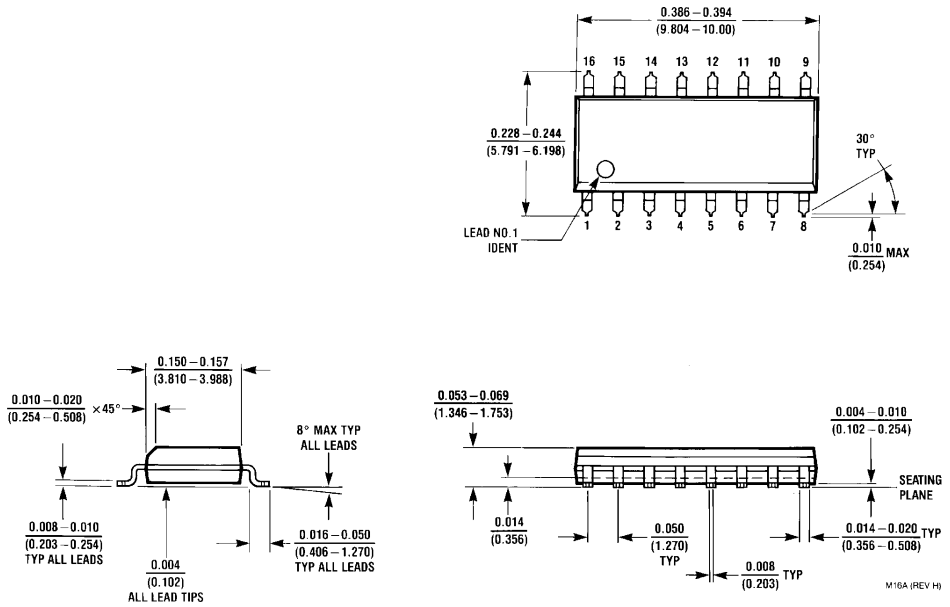
FIGURE 2. Waveforms
(Input Pulse Characteristics; f=1MHz, t_r=t_f=3ns)

Symbol	V_{CC}		
	3.3V ± 0.3V	**2.7V**	**2.5V ± 0.2V**
V_{mi}	1.5V	1.5V	V_{CC}/2
V_{mo}	1.5V	1.5V	V_{CC}/2
V_x	V_{OL} + 0.3V	V_{OL} + 0.3V	V_{OL} + 0.15V
V_y	V_{OH} − 0.3V	V_{OH} − 0.3V	V_{OH} − 0.15V

Schematic Diagram Generic for LCX Family

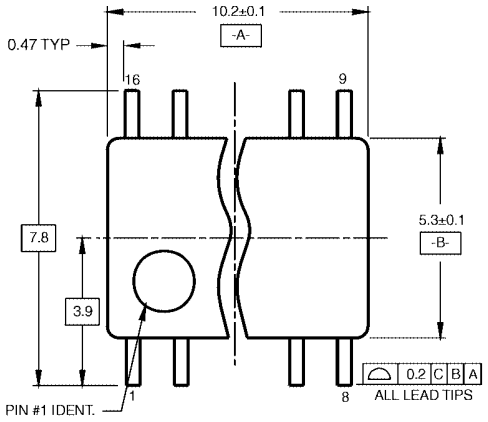


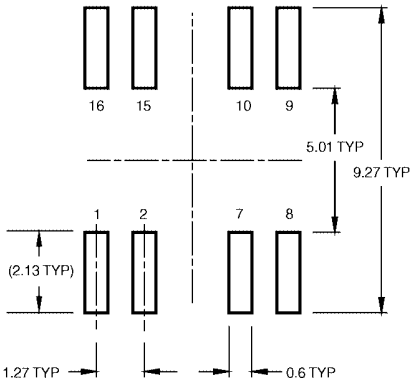
Physical Dimensions inches (millimeters) unless otherwise noted



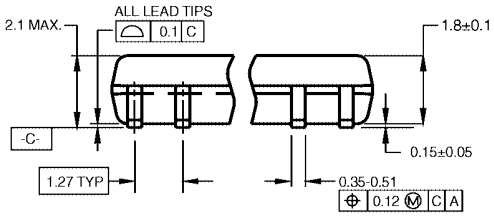
16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

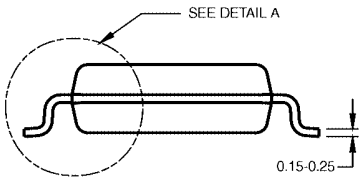


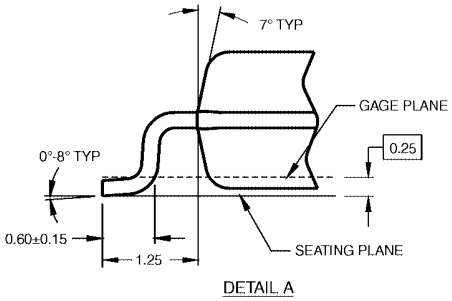


LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS





DETAIL A

NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

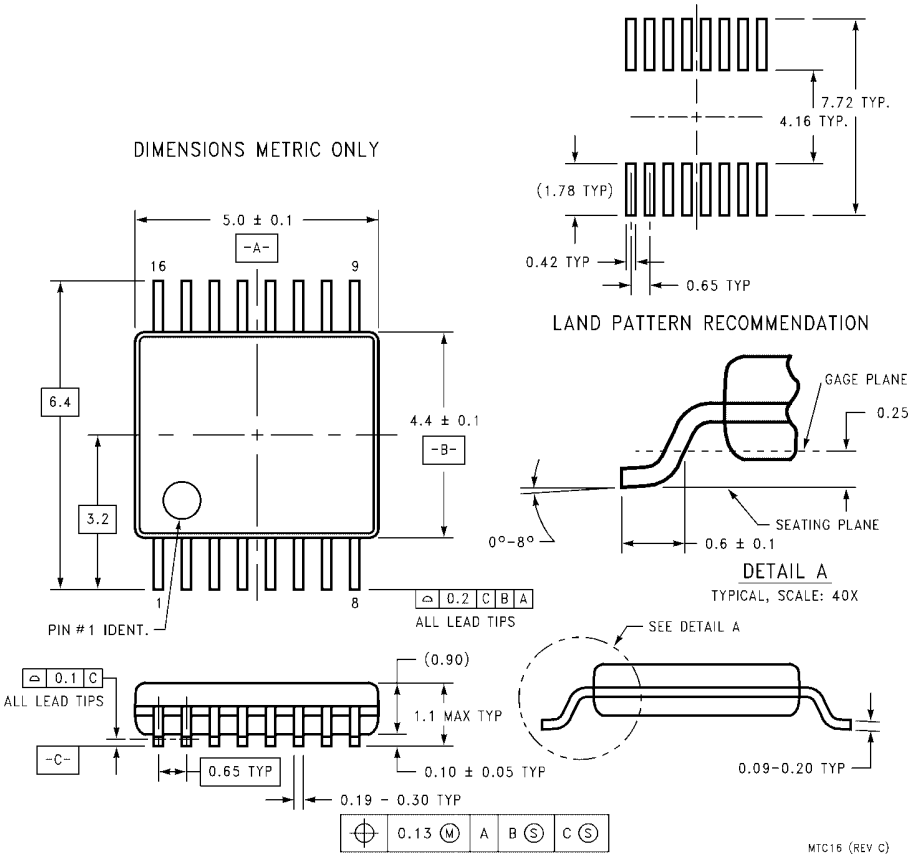
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M16DRevB1

16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC16

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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