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74ACT18823MTD

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August 1999
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74ACT18823
18-Bit D-Type Flip-Flop with 3-STATE Outputs

General Description

The ACT18823 contains eighteen non-inverting D-type flip-flops with 3-STATE outputs and is intended for bus oriented applications. The device is byte controlled. A buffered clock ($\overline{CP}$), Clear ($\overline{CLR}$), Clock Enable ($\overline{EN}$) and Output Enable ($\overline{OE}$) are common to each byte and can be shorted together for full 18-bit operation.

Features

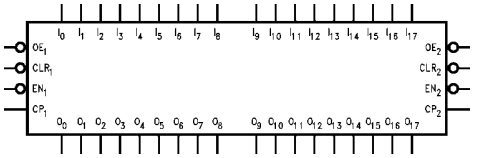
- Broadside pinout allows for easy board layout
- Separate control logic for each byte
- Extra data width for wider address/data paths or buses carrying parity
- Outputs source/sink 24 mA
- TTL-compatible inputs

Ordering Code:

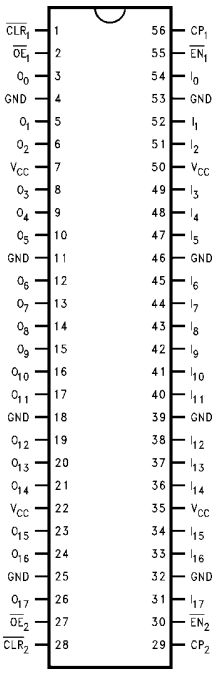
Order Number	Package Number	Package Description
74ACT18823SSC	MS56A	56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74ACT18823MTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
$\overline{CLR}_n$	Clear (Active LOW)
$\overline{EN}_n$	Clock Enable (Active LOW)
CP_n	Clock Pulse Input
I_0–I_{17}	Inputs
O_0–O_{17}	Outputs

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Functional Description

The ACT18823 consists of eighteen D-type edge-triggered flip-flops. These have 3-STATE outputs for bus systems organized with inputs and outputs on opposite sides. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation. The following description applies to each byte. The buffered clock (CP_n) and buffered Output Enable ($\overline{OE}_n$) are common to all flip-flops within that byte. The flip-flops will store the state of their individual D inputs that meet set-up and hold time requirements on the LOW-to-HIGH CP_n transition. With $\overline{OE}_n$ LOW, the contents of the flip-flops are available at the outputs. When $\overline{OE}_n$ is HIGH, the outputs go to the impedance state. Operation of the $\overline{OE}_n$ input does not affect the state of the flip-flops. In addition to the Clock and Output Enable pins, there are Clear ($\overline{CLR}_n$) and Clock Enable ($\overline{EN}_n$) pins. These devices are ideal for parity bus interfacing in high performance systems.

When $\overline{CLR}_n$ is LOW and $\overline{OE}_n$ is LOW, the outputs are LOW. When $\overline{CLR}_n$ is HIGH, data can be entered into the flip-flops. When $\overline{EN}_n$ is LOW, data on the inputs is transferred to the outputs on the LOW-to-HIGH clock transition. When the $\overline{EN}_n$ is HIGH, the outputs do not change state, regardless of the data or clock input transitions.

Function Table

(Note 1)

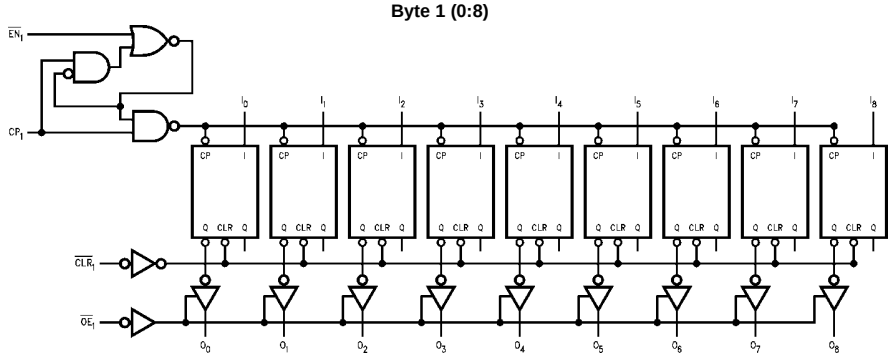
Inputs					Internal	Output	Function
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	CP	I_n	Q	O_n	
H	X	L	⌐	L	L	Z	High Z
H	X	L	⌐	H	H	Z	High Z
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	Clear
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	Hold
H	H	L	⌐	L	L	Z	Load
H	H	L	⌐	H	H	Z	Load
L	H	L	⌐	L	L	L	Load
L	H	L	⌐	H	H	H	Load

H= HIGH Voltage Level
L= LOW Voltage Level
X= Immaterial
Z= High Impedance
⌐= LOW-to-HIGH Transition
NC= No Change

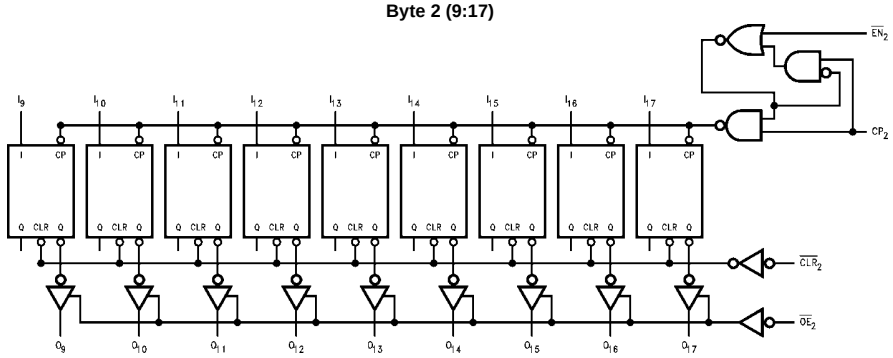
Note 1: The table represents the logic for one byte. The two bytes are independent of each other and function identically.

Logic Diagrams

Byte 1 (0:8)



Byte 2 (9:17)



Absolute Maximum Ratings(Note 2)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} +0.5V	+20 mA
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} +0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source/Sink Current (I_O)	± 50 mA
DC V_{CC} or Ground Current	
Per Output Pin	± 50 mA
Junction Temperature	
PDIP/SOIC	+140°C
Storage Temperature	−65°C to +150°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate (ΔV/Δt)	125 mV/ns
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	

Note 2: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = +25°C Typ	T_A = −40°C to +85°C Guaranteed Limits		Units	Conditions
V_{IH}	Minimum HIGH Input Voltage	4.5	1.5	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} −0.1V
		5.5	1.5	2.0	2.0		
V_{IL}	Maximum LOW Input Voltage	4.5	1.5	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} −0.1V
		5.5	1.5	0.8	0.8		
V_{OH}	Minimum HIGH Output Voltage	4.5	4.49	4.4	4.4	V	I_{OUT} = −50 μA
		5.5	5.49	5.4	5.4		
							V_{IN} = V_{IL} or V_{IH}
		4.5		3.86	3.76	V	I_{OH} = −24 mA
		5.5		4.86	4.76		I_{OH} = −24 mA (Note 3)
V_{OL}	Maximum LOW Output Voltage	4.5	0.001	0.1	0.1	V	I_{OUT} = 50 μA
		5.5	0.001	0.1	0.1		
							V_{IN} = V_{IL} or V_{IH}
		4.5		0.36	0.44	V	I_{OL} = 24 mA
		5.5		0.36	0.44		I_{OL} = 24 mA (Note 3)
I_{OZ}	Maximum 3-STATE Leakage Current	5.5		±0.5	±5.0	μA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V_I = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.5	mA	V_I = V_{CC} −2.1V
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	80.0	μA	V_{IN} = V_{CC} or GND
I_{OLD}	Minimum Dynamic Output Current (Note 4)	5.5			75	mA	V_{OLD} = 1.65V Max
I_{OHD}					−75	mA	V_{OHD} = 3.85V Min

Note 3: All outputs loaded; thresholds associated with output under test.

Note 4: Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V) (Note 5)	$T_A = +25°C$, $C_L = 50$ pF		$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	5.0	100		90		MHz
t_{PHL}	Propagation Delay	5.0	2.0	9.0	2.0	9.5	ns
t_{PLH}	CP_n to O_n		2.0	9.0	2.0	9.5	
t_{PHL}	Propagation Delay $\overline{CLR}_n$ to O_n	5.0	2.0	9.0	2.0	9.5	ns
t_{PZL}	Output Enable Time	5.0	2.0	9.0	2.0	10.0	ns
t_{PZH}			2.0	9.0	2.0	10.0	
t_{PLZ}	Output Disable Time	5.0	1.5	7.0	1.5	7.5	ns
t_{PHZ}			1.5	8.0	1.5	8.5	

Note 5: Voltage Range 5.0 is 5.0V ± 0.5V.

AC Operating Requirements

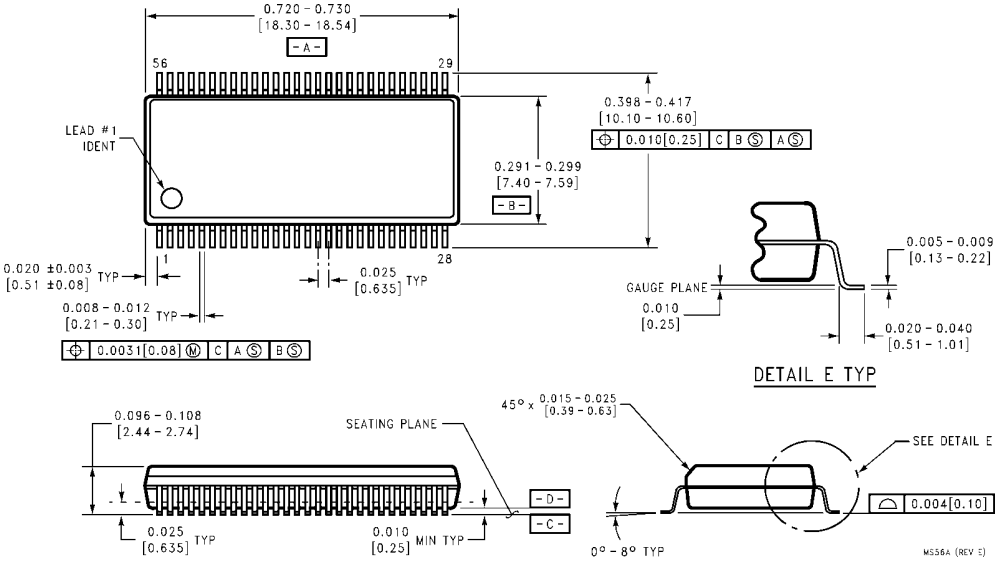
Symbol	Parameter	V_{CC} (V) (Note 6)	$T_A = +25°C$, $C_L = 50$ pF	$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units
			Guaranteed Minimum		
t_S	Setup Time, HIGH or LOW, Input to Clock	5.0	3.0	3.0	ns
t_H	Hold Time, HIGH or LOW, Input to Clock	5.0	1.5	1.5	ns
t_S	Setup Time, HIGH or LOW, Enable to Clock	5.0	3.0	3.0	ns
t_H	Hold Time, HIGH or LOW, Enable to Clock	5.0	1.5	1.5	ns
t_W	$\overline{CP}_n$ Pulse Width, HIGH or LOW	5.0	4.0	4.0	ns
t_W	$\overline{CLR}_n$ Pulse Width, HIGH or LOW	5.0	4.0	4.0	ns
t_{rec}	Recovery Time, $\overline{CLR}_n$ to CP_n	5.0	6.0	6.0	ns

Note 6: Voltage Range 5.0 is 5.0V ± 0.5V.

Capacitance

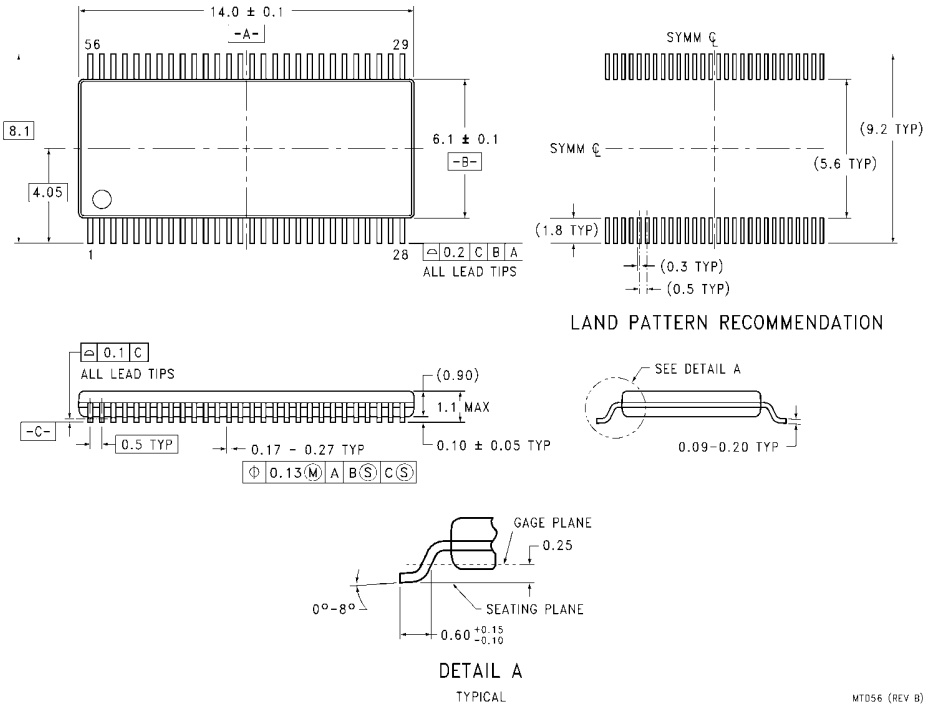
Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Pin Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	95	pF	$V_{CC} = 5.0V$

Physical Dimensions inches (millimeters) unless otherwise noted



56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
Package Number MS56A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD56