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July 2000

FDC6327C

Dual N & P-Channel 2.5V Specified PowerTrench™ MOSFET

General Description

These N & P-Channel 2.5V specified MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize on-state resistance and yet maintain low gate charge for superior switching performance.

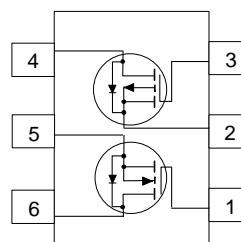
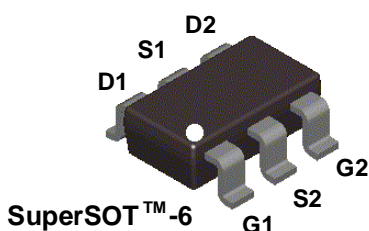
These devices have been designed to offer exceptional power dissipation in a very small footprint for applications where the bigger more expensive SO-8 and TSSOP-8 packages are impractical.

Applications

- DC/DC converter
- Load switch
- Motor driving

Features

- N-Channel 2.7A, 20V. $R_{DS(on)} = 0.08\Omega @ V_{GS} = 4.5V$
 $R_{DS(on)} = 0.12\Omega @ V_{GS} = 2.5V$
- P-Channel -1.6A, -20V. $R_{DS(on)} = 0.17\Omega @ V_{GS} = -4.5V$
 $R_{DS(on)} = 0.25\Omega @ V_{GS} = -2.5V$
- Fast switching speed.
- Low gate charge.
- High performance trench technology for extremely low $R_{DS(on)}$.
- SuperSOT™-6 package: small footprint (72% smaller than SO-8); low profile (1mm thick).



Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter	N-Channel	P-Channel	Units
V _{DSS}	Drain-Source Voltage	20	-20	V
V _{GSS}	Gate-Source Voltage	±8	±8	V
I _D	Drain Current - Continuous (Note 1a)	2.7	-1.9	A
	- Pulsed	8	-8	
P _D	Power Dissipation (Note 1a) (Note 1b) (Note 1c)	0.96		W
		0.9		
		0.7		
T _J , T _{stg}	Operating and Storage Junction Temperature Range	-55 to +150		°C

Thermal Characteristics

R _{θJA}	Thermal Resistance, Junction-to-Ambient (Note 1a)	130	°C/W
R _{θJC}	Thermal Resistance, Junction-to-Case (Note 1)	60	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape Width	Quantity
.327	FDC6327C	7"	8mm	3000

Electrical Characteristics
 $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$ $V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	N-Ch P-Ch	20 -20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C $I_D = -250\ \mu\text{A}$, Referenced to 25°C	N-Ch P-Ch		12 -19		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 16\text{ V}, V_{GS} = 0\text{ V}$ $V_{DS} = -16\text{ V}, V_{GS} = 0\text{ V}$	N-Ch P-Ch			1 -1	μA
I_{GSSF}	Gate-Body Leakage, Forward	$V_{GS} = 8\text{ V}, V_{DS} = 0\text{ V}$	All			100	nA
I_{GSSR}	Gate-Body Leakage, Reverse	$V_{GS} = -8\text{ V}, V_{DS} = 0\text{ V}$	All			-100	nA

On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$ $V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	N-Ch P-Ch	0.4 -0.4	0.9 -0.9	1.5 -1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C $I_D = -250\ \mu\text{A}$, Referenced to 25°C	N-Ch P-Ch		-2.1 2.3		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 4.5\text{ V}, I_D = 2.7\text{ A}$ $V_{GS} = 4.5\text{ V}, I_D = 2.7\text{ A}, T_J = 125^\circ\text{C}$ $V_{GS} = 2.5\text{ V}, I_D = 2.2\text{ A}$ $V_{GS} = -4.5\text{ V}, I_D = -1.6\text{ A}$ $V_{GS} = -4.5\text{ V}, I_D = -1.6\text{ A}, T_J = 125^\circ\text{C}$ $V_{GS} = -2.5\text{ V}, I_D = -1.3\text{ A}$	N-Ch N-Ch N-Ch P-Ch P-Ch P-Ch		0.069 0.094 0.093 0.141 0.203 0.205	0.08 0.13 0.12 0.17 0.27 0.25	Ω
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 4.5\text{ V}, V_{DS} = 5\text{ V}$ $V_{GS} = -4.5\text{ V}, V_{DS} = -5\text{ V}$	N-Ch P-Ch	8 -8			A
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 2.7\text{ A}$ $V_{DS} = -5\text{ V}, I_D = -1.9\text{ A}$	N-Ch P-Ch		7.7 4.5		S

Dynamic Characteristics

C_{iss}	Input Capacitance	N-Channel $V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	N-Ch P-Ch		325 315		pF
C_{oss}	Output Capacitance	P-Channel	N-Ch P-Ch		75 65		pF
C_{riss}	Reverse Transfer Capacitance	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	N-Ch P-Ch		35 24		pF

Electrical Characteristics (continued) $T_A = 25^\circ\text{C}$ unless otherwise noted

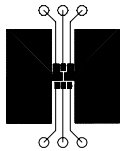
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Switching Characteristics (Note 2)							
$t_{d(on)}$	Turn-On Delay Time	N-Channel $V_{DD} = 10\text{ V}, I_D = 1\text{ A},$ $V_{GS} = 4.5\text{ V}, R_{GEN} = 6\ \Omega$	N-Ch P-Ch		5 7	15 14	ns
t_r	Turn-On Rise Time		N-Ch P-Ch		9 14	18 25	ns
$t_{d(off)}$	Turn-Off Delay Time	P-Channel $V_{DD} = -10\text{ V}, I_D = -1\text{ A},$ $V_{GS} = -4.5\text{ V}, R_{GEN} = 6\ \Omega$	N-Ch P-Ch		12 14	22 25	ns
t_f	Turn-Off Fall Time		N-Ch P-Ch		3 3	9 9	ns
Q_g	Total Gate Charge	N-Channel $V_{DS} = 10\text{ V}, I_D = 2.7\text{ A}, V_{GS} = 4.5\text{ V}$	N-Ch P-Ch		3.25 2.85	4.5 4.0	nC
Q_{gs}	Gate-Source Charge		N-Ch P-Ch		0.65 0.68		nC
Q_{gd}	Gate-Drain Charge	P-Channel $V_{DS} = -10\text{ V}, I_D = -1.9\text{ A}, V_{GS} = -4.5\text{ V}$	N-Ch P-Ch		0.90 0.65		nC

Drain-Source Diode Characteristics and Maximum Ratings

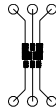
I_S	Maximum Continuous Drain-Source Diode Forward Current		N-Ch P-Ch			0.8 -0.8	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 0.8\text{ A}$ (Note 2) $V_{GS} = 0\text{ V}, I_S = -0.8\text{ A}$ (Note 2)	N-Ch P-Ch		0.76 -0.79	1.2 -1.2	V

Notes:

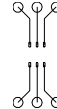
- 1: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design. Both devices are assumed to be operating and sharing the dissipated heat energy equally.



a) 130 °C/W when mounted on a 0.125 in² pad of 2 oz. copper.



b) 140 °C/W when mounted on a 0.005 in² pad of 2 oz. copper.



c) 180 °C/W when mounted on a 0.0015 in² pad of 2 oz. copper.

Scale 1 : 1 on letter size paper

- 2: Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$

Typical Characteristics: N-Channel

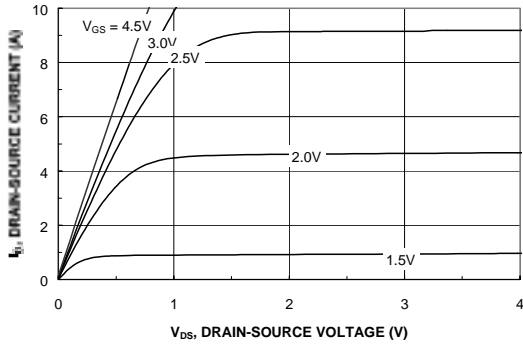


Figure 1. On-Region Characteristics.

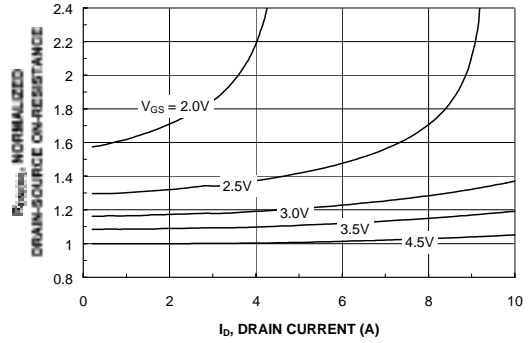


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

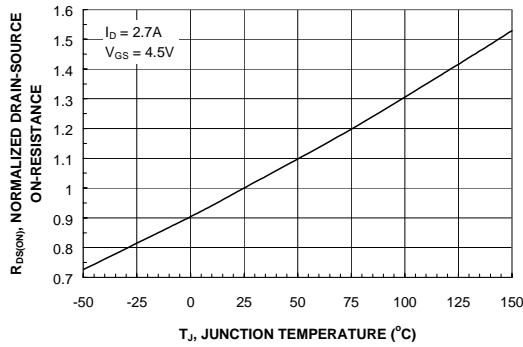


Figure 3. On-Resistance Variation with Temperature.

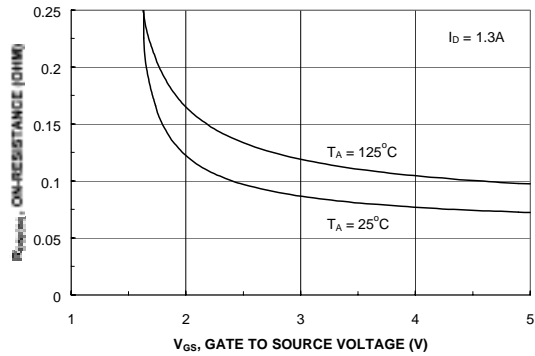


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

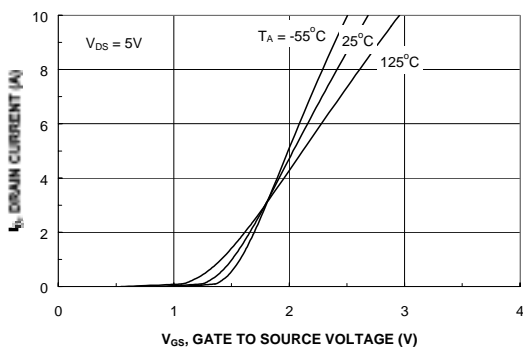


Figure 5. Transfer Characteristics.

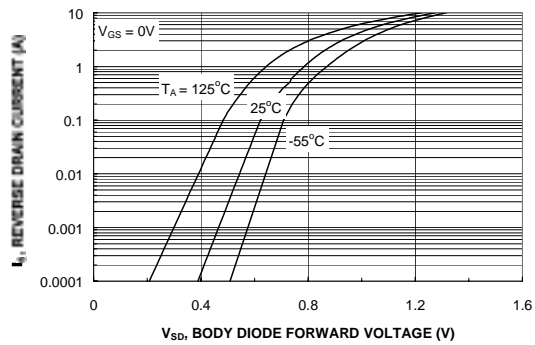


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: N-Channel (continued)

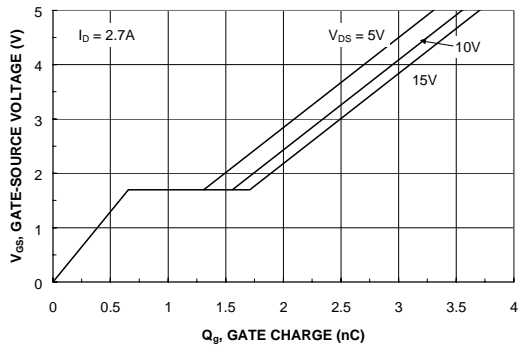


Figure 7. Gate-Charge Characteristics.

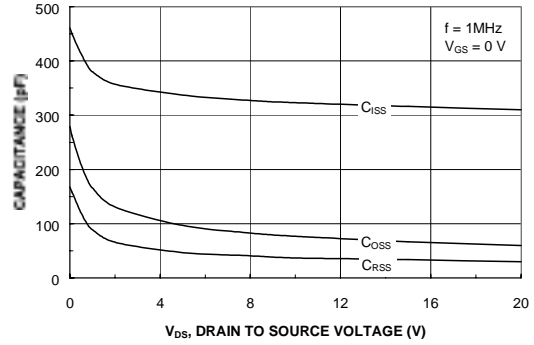


Figure 8. Capacitance Characteristics.

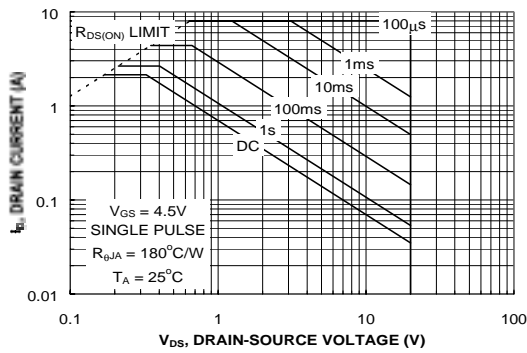


Figure 9. Maximum Safe Operating Area.

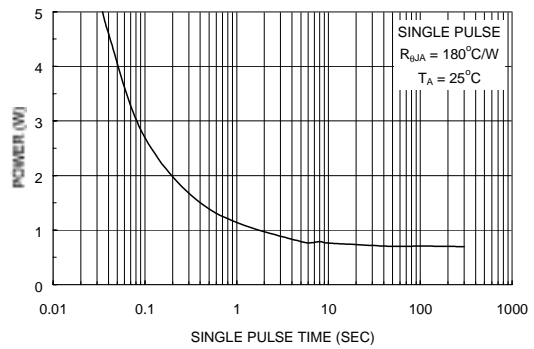


Figure 10. Single Pulse Maximum Power Dissipation.

Typical Characteristics: P-Channel

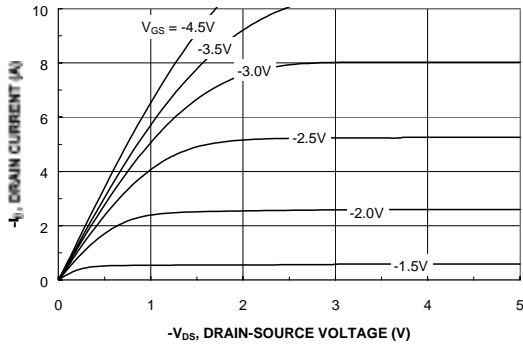


Figure 11. On-Region Characteristics.

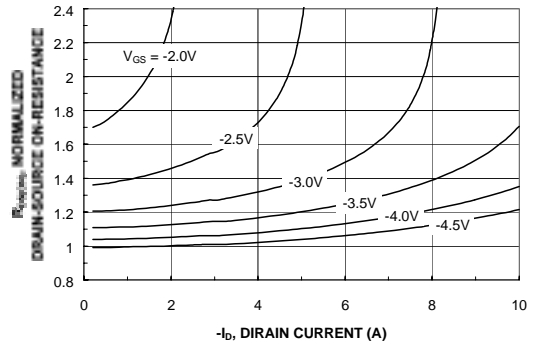


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.

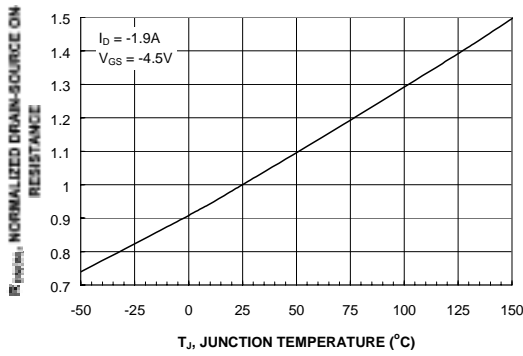


Figure 13. On-Resistance Variation with Temperature.

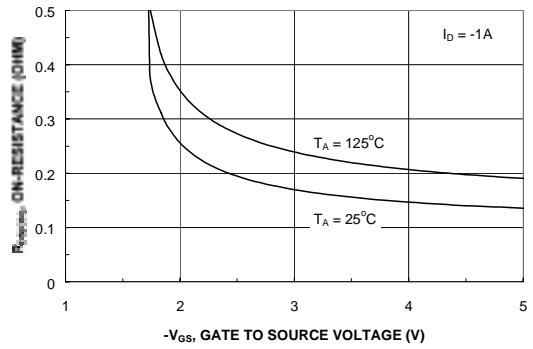


Figure 14. On-Resistance Variation with Gate-to-Source Voltage.

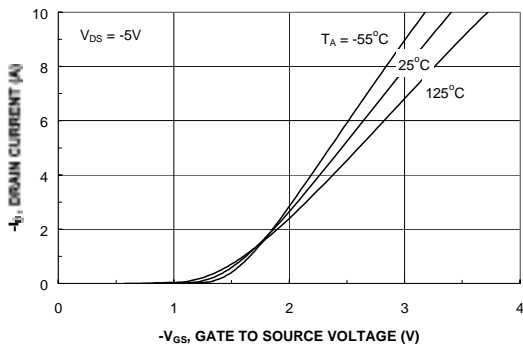


Figure 15. Transfer Characteristics.

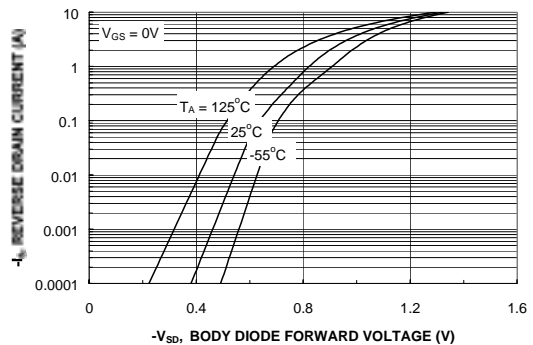


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: P-Channel (continued)

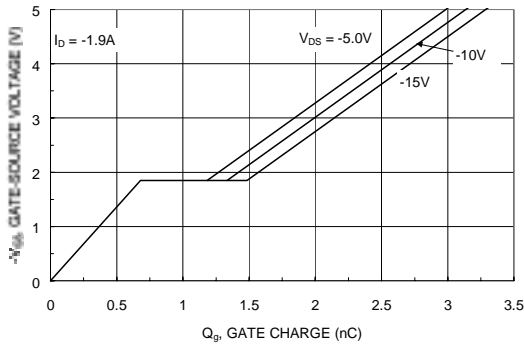


Figure 17. Gate-Charge Characteristics.

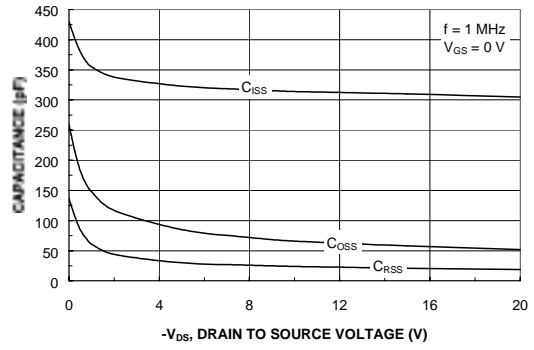


Figure 18. Capacitance Characteristics.

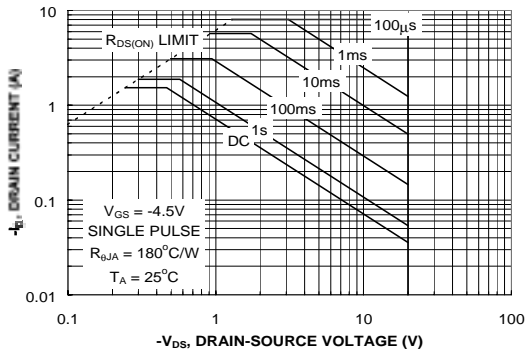


Figure 19. Maximum Safe Operating Area.

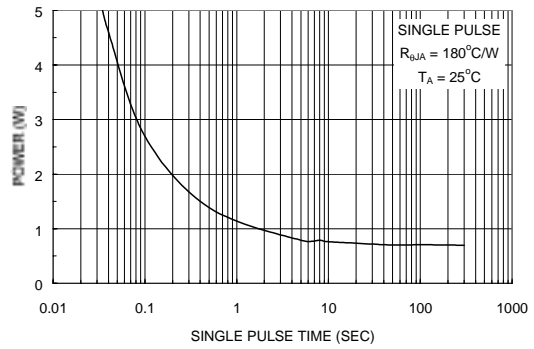


Figure 20. Single Pulse Maximum Power Dissipation.

Typical Characteristics: N & P-Channel (continued)

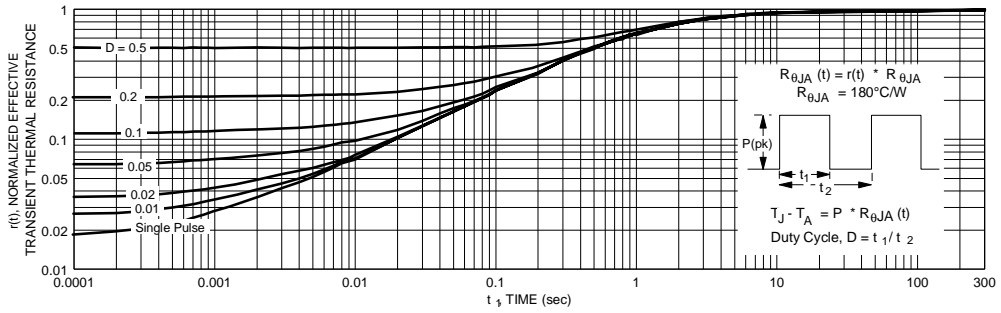


Figure 21. Transient Thermal Response Curve.

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E ² CMOS™	MICROWIRE™	SuperSOT™-6	
EnSigna™	OPTOLOGIC™	SuperSOT™-8	
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