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Fairchild Semiconductor FDD6670AS

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Datasheet of FDD6670AS - MOSFET N-CH 30V 76A DPAK

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May 2005

FDD6670AS

30V N-Channel PowerTrench® SyncFET[™] General Description F

The FDD6670AS is designed to replace a single MOSFET and Schottky diode in synchronous DC:DC power supplies. This 30V MOSFET is designed to maximize power conversion efficiency, providing a low $R_{\text{DS}(\text{ON})}$ and low gate charge. The FDD6670AS includes a patented combination of a MOSFET monolithically integrated with a schottky diode. The performance of the FDD6670AS as the low-side switch in a synchronous rectifier is indistinguishable from the performance of the FDD6670A in parallel with a Schottky diode.

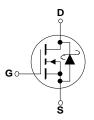
Applications

- DC/DC converter
- · Low side notebook

Features

- 76 A, 30 V $R_{DS(ON)}$ max= 8.0 m Ω @ V_{GS} = 10 V $R_{DS(ON)}$ max= 10.4 m Ω @ V_{GS} = 4.5 V
- Includes SyncFET Schottky body diode
- · Low gate charge (29nC typical)
- High performance trench technology for extremely low R_{DS(ON)}
- High power and current handling capability

G S TO-252



Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V _{DSS}	Drain-Source Voltage		30	V
V _{GSS}	Gate-Source Voltage		±20	V
I _D	Drain Current - Continuous	(Note 3)	76	А
	- Pulsed	(Note 1a)	100	
P _D	Power Dissipation	(Note 1)	70	W
		(Note 1a)	3.2	
		(Note 1b)	1.3	
T _J , T _{STG}	Operating and Storage Junction Tem	perature Range	-55 to +150	°C

Thermal Characteristics

R ₀ JC	Thermal Resistance, Junction-to-Case (Note 1)	1.8	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	40	°C/W
R _{θJA}	Thermal Resistance, Junction-to-Ambient (Note 1b)	96	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDD6670AS	FDD6670AS	13"	16mm	2500 units

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Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Drain-So	urce Avalanche Ratings (Note 2)	ı			
W _{DSS}	Drain-Source Avalanche Energy	Single Pulse, $V_{DD} = 15 \text{ V}$, $I_D = 14 \text{A}$			245	mJ
I _{AR}	Drain-Source Avalanche Current				14	Α
Off Char	acteristics			I	l l	
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_{D} = 1 \text{ mA}$	30			V
ΔBV _{DSS}	Breakdown Voltage Temperature	I _D = 10 mA, Referenced to 25°C		29		mV/°C
ΔT_J	Coefficient	,				
DSS	Zero Gate Voltage Drain Current	$V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}$			500	μΑ
		$V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 125^{\circ}\text{C}$		6.5		mA
GSS	Gate-Body Leakage	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$			±100	nA
On Chara	acteristics (Note 2)					
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 1 \text{ mA}$	1	1.8	3	V
∆V _{GS(th)}	Gate Threshold Voltage	I _D = 10 mA, Referenced to 25°C		-3.3		mV/°C
ΔT _J	Temperature Coefficient	V - 40 V L 42 9 A	1		0.0	
R _{DS(on)}	Static Drain–Source On–Resistance	$V_{GS} = 10 \text{ V}, \qquad I_{D} = 13.8 \text{ A}$ $V_{GS} = 4.5 \text{ V}, \qquad I_{D} = 11.7 \text{ A}$		6.8 8.3	8.0 10.4	mΩ
		$V_{GS} = 10 \text{ V}, I_D = 13.8 \text{A}, T_J = 125 ^{\circ}\text{C}$		9.3	11.6	
D(on)	On–State Drain Current	$V_{GS} = 10 \text{ V}, \qquad V_{DS} = 5 \text{ V}$	50			Α
g _{FS}	Forward Transconductance	V _{DS} = 15 V, I _D = 13.8 A		52		S
	Characteristics	1		•		
C _{iss}	Input Capacitance	$V_{DS} = 15 \text{ V}, \qquad V_{GS} = 0 \text{ V},$		1580		pF
C _{oss}	Output Capacitance	$V_{DS} = 15 \text{ V}, \qquad V_{GS} = 0 \text{ V},$ $f = 1.0 \text{ MHz}$		440		pF
C _{rss}	Reverse Transfer Capacitance	1 - 1.0 WHZ		170		pF
R _G	Gate Resistance	V _{GS} = 15 mV, f = 1.0 MHz		1.8		Ω
-		130 10 111, 110 1111	1]	
	g Characteristics (Note 2)	V 45 V 1 4 A	1	10	20	no
t _{d(on)}	Turn-On Delay Time	$V_{DS} = 15 \text{ V}, \qquad I_{D} = 1 \text{ A}, V_{GS} = 10 \text{ V}, \qquad R_{GEN} = 6 \Omega$		12	20 22	ns
t _r	Turn-On Rise Time	- Index of the second of the s				ns
t _{d(off)}	Turn-Off Delay Time	_		28	45	ns
t _f	Turn-Off Fall Time	V 45 V 1 4 A	-	20	36	ns
t _{d(on)}	Turn-On Delay Time	$V_{DS} = 15 \text{ V}, \qquad I_{D} = 1 \text{ A}, \ V_{GS} = 4.5 \text{ V}, \qquad R_{GEN} = 6 \Omega$		15	27	ns
t _r	Turn-On Rise Time	- Iden 1		16	29	ns
d(off)	Turn–Off Delay Time Turn–Off Fall Time	_		26 13	42 23	ns
t _f		$V_{DS} = 15 \text{ V}, I_D = 13.8 \text{ A},$	-			ns
Q _{g(TOT)}	Total Gate Charge at V _{GS} =10V Total Gate Charge at V _{GS} =5V	- 10 v, ij - 10.0 A,	-	29	40 22	nC nC
Q _{g(TOT)}	Gate—Source Charge	-	-	16 4.6		nC nC
Q _{gs}	Ŭ	_				
Q _{gd}	Gate-Drain Charge			5.5		nC
	ource Diode Characteristics	T.,	1			
V _{SD}	Drain–Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = 3.5 \text{ A} \text{(Note 2)}$ $V_{GS} = 0 \text{ V}, I_S = 7 \text{ A} \text{(Note 2)}$		0.46 0.59	0.7	V
t _{rr}	Diode Reverse Recovery Time	I _F = 3.5 A,		20		ns
Q _{rr}	Diode Reverse Recovery Charge	$d_{iF}/d_t = 300 \text{ A/}\mu\text{s}$ (Note 3)		15		nC

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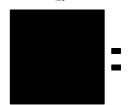
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Electrical Characteristics

T_A = 25°C unless otherwise noted

Notes

 R_{0,1A} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{0,1C} is guaranteed by design while R_{0,CA} is determined by the user's board design.



a) $R_{\theta,JA} = 40^{\circ}\text{C/W}$ when mounted on a 1in^2 pad of 2 oz copper



b) R_{BJA} = 96°C/W when mounted on a minimum pad

Scale 1:1 on letter size paper

2. Pulse Test: Pulse Width < $300\mu s$, Duty Cycle < 2.0%

3. Maximum current is calculated as: $\sqrt{\frac{P_D}{R_{DS(ON)}}}$

where P_D is maximum power dissipation at $T_C = 25^{\circ}C$ and $R_{DS(on)}$ is at $T_{J(max)}$ and $V_{GS} = 10V$. Package current limitation is 21A





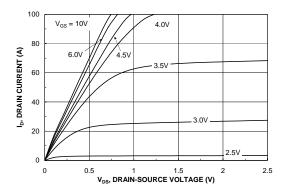


Figure 1. On-Region Characteristics.

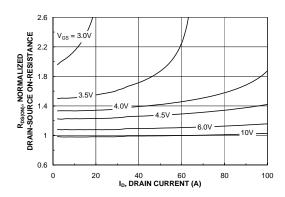


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

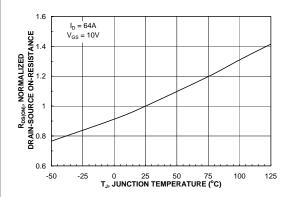


Figure 3. On-Resistance Variation with Temperature.

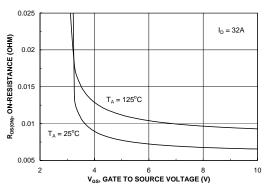


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

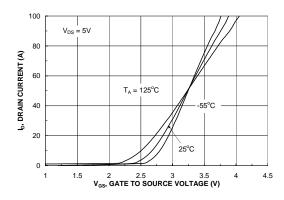


Figure 5. Transfer Characteristics.

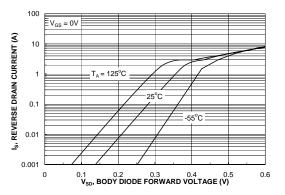
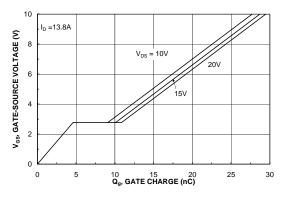


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.







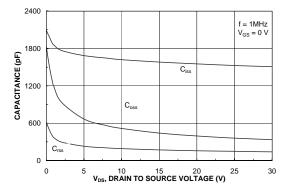
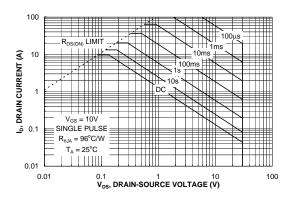


Figure 7. Gate Charge Characteristics.

Figure 8. Capacitance Characteristics.



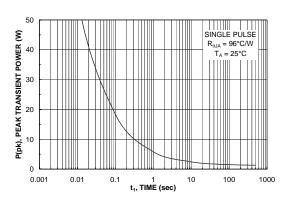


Figure 9. Maximum Safe Operating Area.

Figure 10. Single Pulse Maximum Power Dissipation.

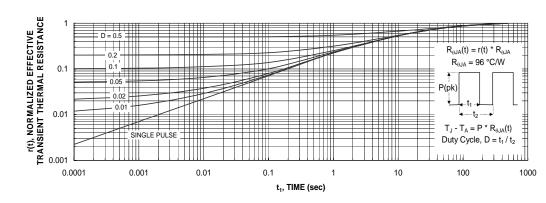


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.



Typical Characteristics (continued)

SyncFET Schottky Body Diode Characteristics

Fairchild's SyncFET process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 12 shows the reverse recovery characteristic of the FDD6670AS.

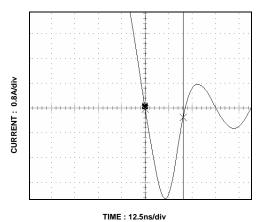


Figure 12. FDD6670AS SyncFET body diode

For comparison purposes, Figure 13 shows the reverse recovery characteristics of the body diode of an equivalent size MOSFET produced without SyncFET (FDD6670A).

reverse recovery characteristic.

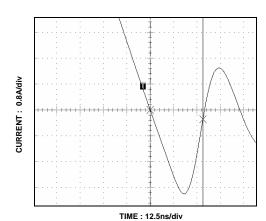


Figure 13. Non-SyncFET (FDD6670A) body diode reverse recovery characteristic.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

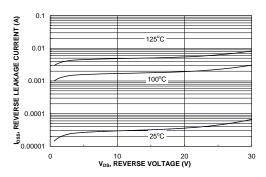


Figure 14. SyncFET body diode reverse leakage versus drain-source voltage and temperature.



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