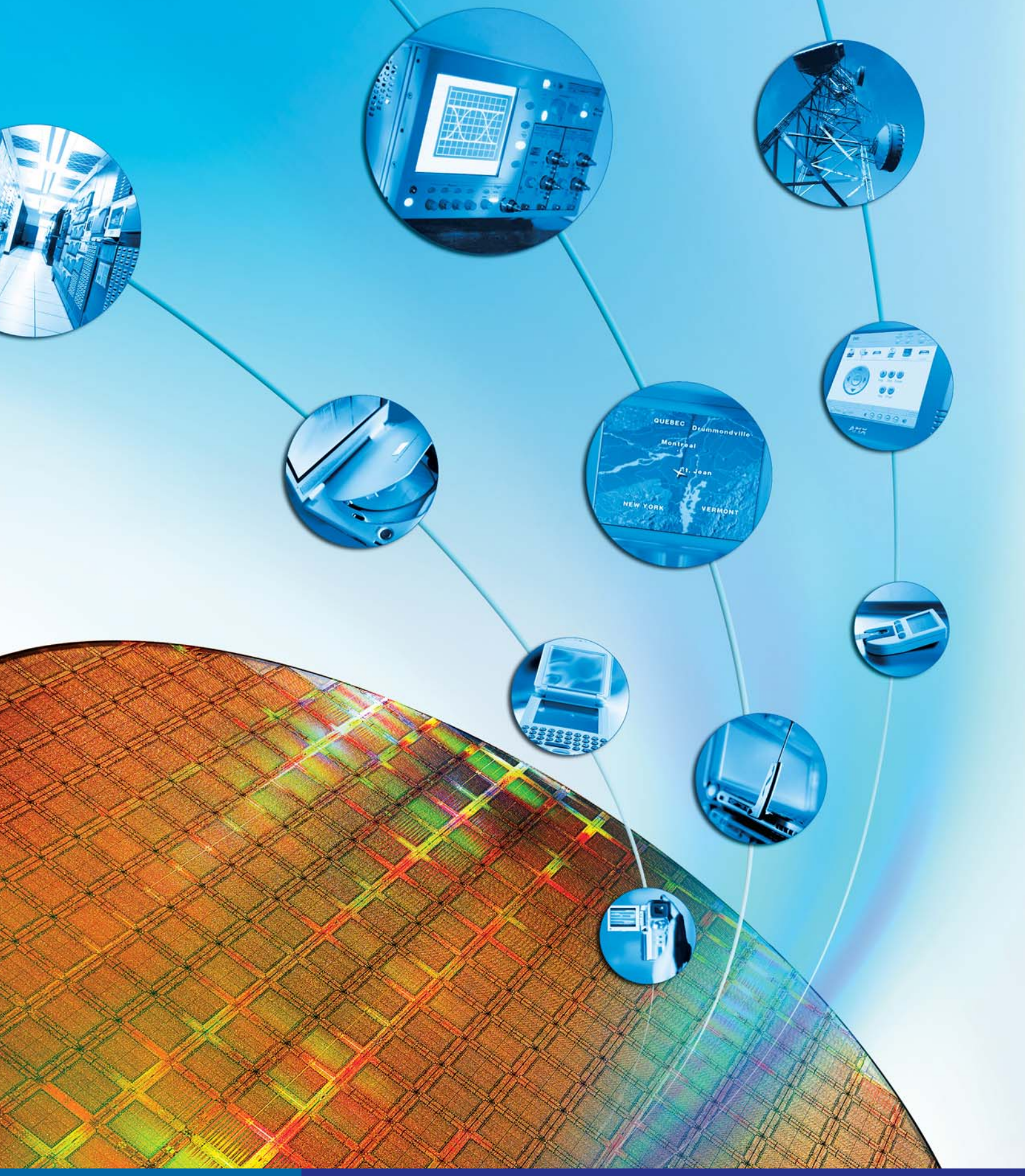


ALTERA®

Altera Product Catalog

January 2006

The Programmable Solutions Company

Altera's success is built on a commitment to innovation exemplified by the invention of the world's first reprogrammable logic device over twenty years ago. Our latest product portfolio combines the inherent value of programmable logic—flexibility and time-to-market advantages—with higher levels of performance and integration. It was specifically developed to address the wide range of today's system needs. Altera's programmable solutions include:

- The industry's most advanced FPGA, CPLD, and structured ASIC technologies
- Customizable embedded processors
- Optimized intellectual property (IP) cores
- A fully integrated software development tool
- Off-the-shelf development kits

For more information about Altera® products, please go to **www.altera.com**. If you have feedback on this catalog, please email us at **catalog@altera.com**.

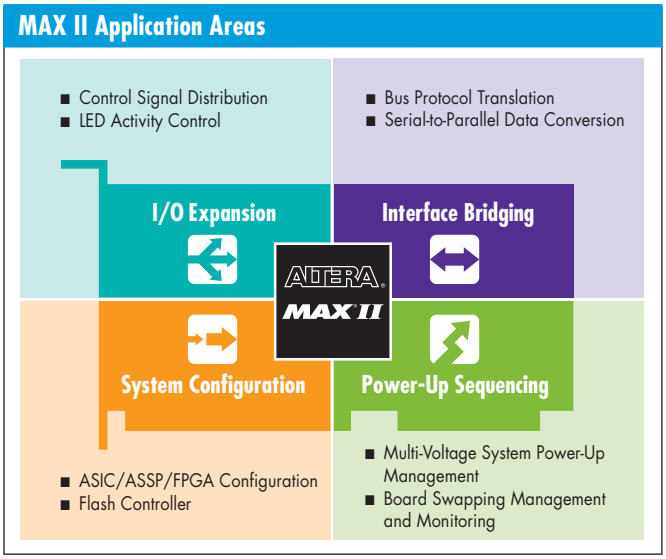
Contents

MAX CPLD Series

The industry-leading MAX® series of CPLDs are world-class, low-cost solutions for a wide variety of digital applications. Instant-on MAX CPLDs represent the ultimate in flexibility, as they can be independent programmable solutions or complement other semiconductors in a system. MAX CPLDs are non-volatile, single-chip solutions that do not require additional configuration devices. This means that they can be preprogrammed and reprogrammed using in-system programmability (ISP) and will retain the programming algorithm securely, even when the device is powered off.

Key Features

- Low cost
- Low power
- Instant-on and non-volatile
- ISP
- Free Quartus® II Web Edition software support



MAX® II

The Lowest-Cost CPLD Ever

MAX II devices are based on a ground-breaking new CPLD architecture that delivers the lowest cost per I/O pin of any CPLD family. MAX II devices deliver one-tenth the power, four times the density, and twice the performance of previous MAX devices at half the cost. This instant-on, non-volatile device family targets general-purpose control logic applications. In addition to delivering the lowest cost for traditional CPLD designs, MAX II devices drive cost and power improvements to higher densities, enabling you to use these devices in place of higher-cost or higher-power ASSPs and standard logic devices.

MAX II CPLDs optimally support four key applications: I/O expansion, interface bridging, system configuration, and power-up sequencing.

MAX II Family Features Summary	
Cost-Optimized Architecture	Delivers four times the density at half the price of competing CPLDs with the revolutionary MAX II architecture.
Low Power	Reduces power consumption and increases system reliability.
Highest-Density CPLDs	Implements more applications in a single, low-cost device.
Non-Volatile and Instant-On Functionality	Reduces system cost and board space with a single-chip solution.
User Flash Memory	Minimizes system cost and chip count by integrating discrete serial or parallel non-volatile storage onto MAX II devices.
Real-Time ISP	Reduces maintenance costs by enabling updates while the device is in operation.
MultiVolt™ Core	Operates with a 1.8-, 2.5-, or 3.3-V power supply, minimizing power rails and simplifying board design.
MultiVolt I/O Interface	Interfaces seamlessly to other devices at 1.5-, 1.8-, 2.5-, or 3.3-V logic levels.
Parallel Flash Loader	Simplifies board management by using MAX II devices to configure external non-JTAG-compliant flash devices.

MAX®

General-Purpose CPLDs

Altera's 3.3-V MAX 3000A devices are cost-optimized for high-volume applications, while the 5.0-, 3.3-, and 2.5-V MAX 7000 families offer world-class, high-performance solutions for a broad array of applications. The non-volatile, EEPROM-based MAX 3000A and MAX 7000 families provide instant-on capability and offer densities from 32 to 512 macrocells. These devices support ISP and can be easily reconfigured in the field.

MAX 3000A Family Features	
Low Price per Macrocell	Ideal for low-cost, high-volume applications.
4.5-ns Propagation Delays	Provides fast system performance.
5.0-V Tolerant I/O Pins	Inherently interfaces to 5.0-V devices.
Commercial and Industrial Temperature	Reduces overall system cost for temperature-sensitive applications.
MAX 7000 Family Features	
4.5-ns Propagation Delays	Provides fast system performance.
Support for Advanced I/O Standards	Supports GTL+ and SSTL-2/-3 I/O standards (MAX 7000B CPLDs).
Programmable Power-Saving Mode	Reduces power consumption by over 50 percent.
Commercial, Industrial, and Extended Temperature	Provides support for all environmental conditions.

MAX CPLD Series Package & I/O Matrix

36 Number indicates available user I/O pins.

Vertical migration (Same V_{CC}, GND, ISP, and input pins). User I/O may be less than labelled for vertical migration.

All MAX series devices are offered in commercial and industrial temperatures and lead-free packages.

		MAX II 3.3 V, 2.5 V, 1.8 V				MAX 3000A 3.3 V					MAX 7000AE 3.3 V				
		EPM240/G	EPM570/G	EPM1270/G	EPM2210/G	EPM3032A	EPM3064A	EPM3128A	EPM3256A	EPM3512A	EPM7032AE	EPM7064AE	EPM7128AE	EPM7256AE	EPM7512AE
Density & Speed	Macrocells[1]	192	440	980	1,700	32	64	128	256	512	32	64	128	256	512
	Logic Elements (LEs)	240	570	1,270	2,210	–	–	–	–	–	–	–	–	–	–
	Pin-to-Pin Delay (ns)	4.7, 6.2, 7.6	5.5, 7.1, 8.8	6.3, 8.2, 10.1	7.1, 9.2, 11.3	4.5, 7.5, 10	4.5, 7.5, 10	5.0, 7.5, 10	7.5, 10	7.5, 10	4.5, 7.5, 10	4.5, 7.5, 10	5.0, 7.5, 10	5.5, 7.5, 10	7.5, 10, 12
PLCC[2] (L)	44-Pin					34	34				36	36			
	84-Pin												68		
TQFP[3] (T)	44-Pin					34	34				36	36			
	100-Pin	80	76				66	80				68	84	84	
	144-Pin		116	116				96	116				100	120	120
PQFP[4] (Q)	208-Pin								158	172				164	172
BGA[5] (B)	256-Pin														212
FBGA[6] (F)	100-Pin											68	84	84	
	256-Pin		160	212	204			98	161	208			100	164	212
	324-Pin				272										

1 Typical equivalent macrocells for MAX II devices.
2 Plastic J-Lead Chip Carrier
3 Thin Quad Flat Pack
4 Plastic Quad Flat Pack
5 Ball-Grid Array (1.27 mm)
6 FineLine BGA® (1.0 mm)

MAX CPLD Series Features

		MAX II 3.3 V, 2.5 V, 1.8 V				MAX 3000A 3.3 V					MAX 7000AE 3.3 V				
		EPM240/G	EPM570/G	EPM1270/G	EPM2210/G	EPM3032A	EPM3064A	EPM3128A	EPM3256A	EPM3512A	EPM7032AE	EPM7064AE	EPM7128AE	EPM7256AE	EPM7512AE
Features	User Flash Memory (Kbit)	8				–					–				
	Boundary Scan JTAG	✓				✓					✓				
	JTAG ISP	✓				✓					✓				
	Fast Input Registers	✓				–					✓				
	Programmable Register Power-Up	✓				–					✓				
	Programmable Ground Pins	✓				–					✓				
	Open-Drain Outputs	✓				✓					✓				
	Programmable Pull-Up Resistors	✓				–					–				
	Bus Hold	✓				–					–				
	Parallel Flash Loader	✓				–					–				
	Real-Time ISP	✓				–					–				
Core Voltage & I/O Options	Core Voltage (V)	1.8				3.3					3.3				
	MultiVolt Core (V)	3.3, 2.5, 1.8				–					–				
	MultiVolt I/O (V)	3.3, 2.5, 1.8, 1.5				5.0, 3.3, 2.5					5.0, 3.3, 2.5				
	I/O Power Banks	2	2	4	4	1					1				
	Maximum I/O Pins	80	160	212	272	34	66	98	161	208	34	68	100	164	212
	Maximum Output Enables	80	160	212	272	6	6	6	6	10	6	6	6	6	10
	Transistor-to-Transistor Logic (TTL) (5.0-V Tolerance)	–	–	✓[1]	✓[1]	✓					✓				
	LVTTL/LVCMOS	✓				✓					✓				
	32-Bit, 66-MHz PCI Compliant	–	–	✓	✓	–					–				
	Schmitt Triggers	✓				–					–				
	Programmable Slew Rate	✓				✓					✓				
	Programmable Drive Strength	✓				–					–				

[1] An external series resistor must be used for 5.0-V tolerance.

FOR MORE INFORMATION

MAX II CPLDs	www.altera.com/max2
MAX 3000A CPLDs	www.altera.com/products/devices/max3k
MAX 7000 CPLDs	www.altera.com/products/devices/max7k

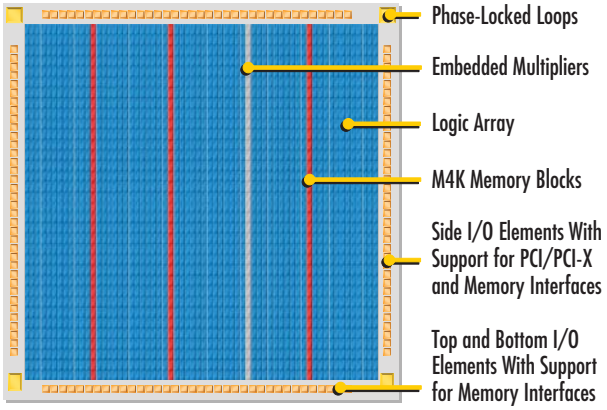
Cyclone Low-Cost FPGA Series

Altera forever changed the FPGA industry with the introduction of the Cyclone™ device family in 2002—bringing to market the first and only FPGA family designed from the ground up for the lowest cost, with each family member individually optimized for minimum die size. The Cyclone FPGA series—including the 90-nm Cyclone II and 130-nm Cyclone families—delivers a customer-defined feature set, industry-leading performance, and the lowest power consumption available. Competitive with ASICs and ASSPs, the Cyclone series gives you a high-volume solution for cost-sensitive applications.

Key Features

- The industry's lowest-cost FPGAs
- One-half the power consumption of competing FPGAs
- High-performance digital signal processing (DSP)
- Low-cost embedded processing
- Free Quartus II Web Edition software support

Cyclone II Floorplan



Cyclone II

90-nm Low-Cost FPGAs

The Cyclone II FPGA family is the second-generation family in the Cyclone series of low-cost FPGAs. Based on the 1.2-V, 90-nm, low-k dielectric process from TSMC, the Cyclone II FPGA family offers you more benefits than its predecessor, plus more density and features at dramatically lower costs. Cyclone II FPGAs include dedicated DSP circuitry for very low-cost DSP solutions. In addition, when implementing Nios® II embedded processors on Cyclone II FPGAs, you can create cost-effective processing solutions for price-sensitive and compute-intensive applications.

Cyclone II Family Features Summary	
Cost-Optimized Architecture	Offers from 4,608 to 68,416 LEs—three-and-a-half times the density of first-generation Cyclone FPGAs—and the lowest cost per LE.
Embedded Memory	Up to 1.1 Mbits of RAM via 4,608-bit memory blocks capable of 250-MHz performance that support multiple configurations, including true dual-port and single-port RAM, ROM, and first-in first-out (FIFO) buffers.
Embedded Multipliers	150 18-bit x 18-bit embedded multipliers running at 250 MHz that can implement common DSP functions such as finite impulse response (FIR) filters and fast Fourier transforms (FFTs). Each 18-bit x 18-bit multiplier can be configured as two independent 9-bit x 9-bit multipliers.
Nios II Embedded Processor Support	Nios II embedded processors offer an ideal replacement for low-cost discrete microprocessors to reduce cost and increase flexibility. Nios II soft processor support for Cyclone II FPGAs offers over 100-DMIPS performance.
Differential and Single-Ended I/O Standards Support	Support for LVTTL, LVCMOS, PCI, PCI-X, PCI Express[1], SSTL, and high-speed transceiver logic (HSTL) single-ended I/O standards. Differential signaling support for LVDS (805 Mbps receiving and 640 Mbps transmitting), mini-LVDS, reduced swing differential signaling (RSDS), LVPECL, SSTL, and HSTL system interfaces.
External Memory Interfaces	Dedicated interfaces supporting external memory devices at 167 MHz for integration with external SDR, DDR, DDR2 SDRAM, and QDRII SRAM devices. Altera offers DDR, DDR2, and QDRII memory controller MegaCore® functions free with Quartus II software subscriptions.
Clock Management Circuitry	16 low-skew, global clock networks span the entire device, fed by 16 dedicated input clock pins. Four phase-locked loops (PLLs), each with three output taps, feature programmable bandwidth, programmable duty cycle, spread-spectrum clocking, lock detection, and frequency synthesis with phase-shifting capabilities, provides complete system clock management on- and off-chip.
On-Chip Termination	Single-ended on-chip termination support for driver impedance matching and series termination eliminates the need for external resistors, improves signal integrity, and simplifies board design.
Hot-Socketing and Power Sequencing	Robust on-chip hot-socketing and power-sequencing support that ensures proper device operation independent of the power-up sequence.
Automatic SEU Detection Circuitry	Features automatic single event upset (SEU) detection circuitry utilizing 32-bit cyclic redundancy check (CRC).

[1] Requires external PHY device.

Cyclone™

130-nm Low-Cost FPGAs

Based on extensive input from hundreds of customers like you, the Cyclone FPGA family was built from the ground up for the lowest cost. Cyclone devices provide application-focused features such as embedded memory, external memory interfaces, and clock management circuitry at price points optimal for high-volume applications.

Cyclone Family Features Summary	
Cost-Optimized Architecture	Offers from 2,910 to 20,060 LEs; built for low cost.
Embedded Memory	288 Kbits of RAM through 4,608-bit memory blocks that can be configured to support a wide range of operation modes including RAM, ROM, FIFO buffers, and single-port and dual-port modes.
Nios II Embedded Processor Support	Nios II embedded processors offer an ideal replacement for low-cost discrete microprocessors to reduce cost and increase flexibility.
Single-Ended I/O Support	Supports a variety of single-ended I/O interface standards, such as the 3.3-V, 2.5-V, 1.8-V, LVTTL, LVCMOS, SSTL, and PCI standards needed for today's systems.
External Memory Interfaces	Dedicated external memory interfaces that allow you to integrate external SDR and DDR SDRAM devices into complex system designs without degrading data access performance.
Differential I/O Support	Support for 129 LVDS and RSDS channels with 640-Mbps LVDS data rates and 311-Mbps RSDS data rates.
Clock Management Circuitry	Features up to two programmable PLLs and eight global clock lines that provide robust clock management and frequency synthesis capabilities enabling on- and off-chip system clock management. PLLs offer advanced features such as frequency synthesis, programmable phase shift, programmable delays, and external clock output.
Hot Socketing and Power Sequencing	Robust on-chip hot-socketing and power-sequencing support that ensures that Cyclone devices operate no matter how the system is powered up.
Automatic Single Event Upset Detection Circuitry	Automatic single event upset detection circuitry utilizing 32-bit CRC to minimize radiation problems.

Cyclone FPGA Series Package & I/O Matrix

104 Number indicates available user I/O pins.

Vertical migration (Same V_{CC}, GND, ISP, and input pins). User I/O may be less than labelled for vertical migration.

All Cyclone series devices are offered in commercial and industrial temperatures and lead-free packages.

		Cyclone II (1.2 V) Low Cost, High Volume						Cyclone (1.5 V) Low Cost, High Volume				
		EP2C5	EP2C8	EP2C20	EP2C35	EP2C50	EP2C70	EP1C3	EP1C4	EP1C6	EP1C12	EP1C20
Thin Quad Flat Pack (T)	100-Pin TQFP							65				
	144-Pin TQFP	89	85					104		98		
Plastic Quad Flat Pack (Q)	208-Pin PQFP	142	138									
	240-Pin PQFP			142						185	173	
FineLine BGA (F)	256-Pin FBGA	158	182	152						185	185	
	324-Pin FBGA								249		249	233
	400-Pin FBGA								301			301
	484-Pin FBGA			315	322	294						
	484-Pin UFBGA[1]				322	294						
	672-Pin FBGA				475	450	422					
	896-Pin FBGA						622					

[1] Ultra FineLine BGA

Cyclone FPGA Series Features

		Cyclone II (1.2 V) Low Cost, High Volume						Cyclone (1.5 V) Low Cost, High Volume				
		EP2C5	EP2C8	EP2C20	EP2C35	EP2C50	EP2C70	EP1C3	EP1C4	EP1C6	EP1C12	EP1C20
Density & Speed	LEs	4,608	8,256	18,752	33,216	50,528	68,416	2,910	4,000	5,980	12,060	20,060
	Total RAM Bits (K)[1]	120	166	240	484	594	1,152	60	78	92	240	295
	M4K RAM Blocks (4 Kbits + 512 Parity Bits)[2]	26	36	52	105	129	250	13	17	20	52	64
	Speed Grades (Fastest to Slowest)	-6, -7, -8						-6, -7, -8				
Architectural Features	Embedded Processor Available	Nios II						Nios II				
	18-Bit x 18-Bit/9-Bit x 9-Bit Embedded Multipliers	13/26	18/36	26/52	35/70	86/172	150/300	–	–	–	–	–
	I/O Registers per I/O Element	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	True Dual-Port RAM	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Global & Regional Clock Networks	8	8	16	16	16	16	8	8	8	8	8
	PLLs/Unique Outputs	2/6	2/6	4/12	4/12	4/12	4/12	1/3	2/6	2/6	2/6	2/6
	Industrial Device Offering	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Lead-Free Device Offering	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Configuration Devices	Configuration File Size (Mbits)	1.26	1.98	3.89	6.85	9.96	14.31	0.63	0.93	1.17	2.32	3.56
	Number of EPCS1 Devices (1 Mbit)	1	–	–	–	–	–	1	1	1	–	–
	Number of EPCS4 Devices (4 Mbits)	1	1	1	–	–	–	1	1	1	1	1
	Number of EPCS16 Devices (16 Mbits)	1	1	1	1	1	1	–	–	–	–	–
	Number of EPCS64 Devices (64 Mbits)	1	1	1	1	1	1	–	–	–	–	–
	Number of EPC2 Devices (1.6 Mbits)	1	1	2	4	5	7	1	1	1	2	2
	Number of EPC4 Devices (4 Mbits)	1	1	1	–	–	–	1	1	1	1	1
	Number of EPC8 Devices (8 Mbits)	1	1	1	1	1	–	1	1	1	1	1
	Number of EPC16 Devices (16 Mbits)	1	1	1	1	1	1	1	1	1	1	1
I/O Features	I/O Voltage Levels Supported (V)	1.5, 1.8, 2.5, 3.3						1.5, 1.8, 2.5, 3.3				
	I/O Standards Supported	LVDS, RSDS, Mini-LVDS, LVPECL, Differential SSTL-18 (I & II), Differential SSTL-2 (I & II), 1.5-V Differential HSTL (I & II), 1.8-V Differential HSTL (I & II), SSTL-18 (I & II), SSTL-2 (I & II), 1.5-V HSTL (I & II), PCI, PCI-X, PCI Express[3], LVTTL, LVCMOS						LVDS, RSDS, Differential SSTL-2, SSTL-2 (I & II), SSTL-3 (I & II), PCI, LVTTL, LVCMOS				
	LVDS Maximum Data Rate (Mbps) (Receive/Transmit)	805/640	805/640	805/640	805/640	805/640	805/640	640/640	640/640	640/640	640/640	640/640
	LVDS Channels	60	79	136	209	197	265	34	129	72	103	129
	RSDS Maximum Data Rate (Mbps) (Transmit)	311	311	311	311	311	311	311	311	311	311	311
	Mini-LVDS Maximum Data Rate (Mbps) (Transmit)	311	311	311	311	311	311	–	–	–	–	–
	Series On-Chip Termination	✓	✓	✓	✓	✓	✓	–	–	–	–	–
	Programmable Drive Strength	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
External Memory Interfaces	Memory Devices Supported	QDRII, DDR2, DDR, SDR						DDR, SDR				
	MegaCore Controller With Clear Text Datapath	✓						✓				
	System Timing Analysis	✓						✓				
	Board Layout Guidelines	✓						✓				

[1] K = 1,000

[2] Kbits = 1,024 bits

[3] Requires external PHY device

FOR MORE INFORMATION

Cyclone II FPGAs	www.altera.com/cyclone2
Cyclone FPGAs	www.altera.com/cyclone
Training	www.altera.com/training

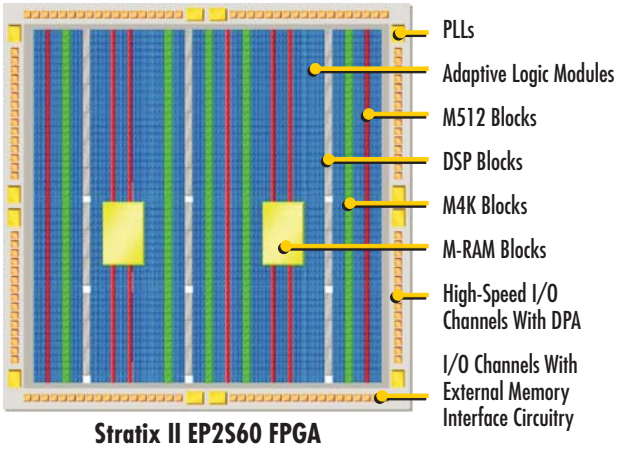
Stratix High-Density FPGA Series

The Stratix® FPGA series provides the richest feature set, highest performance, and largest FPGAs available in the industry. Stratix II FPGAs are the only FPGAs with a risk-free path to structured ASICs with reduced power and costs for volume applications. Only Altera high-density FPGAs use redundancy—a unique, patented Altera technology that dramatically increases yields and lowers device costs. The Stratix FPGA series delivers the density, performance, and features you need at both 90- and 130-nm process nodes.

Key Features

- The industry's biggest and fastest FPGAs
- Feature-rich I/O technology
- 3.1875- and 6.375-Gbps transceivers available
- Industry-leading DSP and memory capacity
- Support for Nios II soft processor
- Optimized for power
- Path to low-cost HardCopy® structured ASICs available
- Design security

Stratix II Floorplan



Stratix II EP2S60 FPGA

Stratix® II

90-nm High-Performance, High-Density FPGAs

Stratix II devices are the industry's leading high-density, high-performance FPGAs. Built on a new, innovative logic structure to maximize performance and minimize power, Stratix II devices on average deliver 50 percent faster performance than prior-generation FPGAs. Stratix II devices are the highest-density FPGAs from any vendor. They are the only FPGAs with a risk-free path to HardCopy II structured ASICs, which can further increase performance, reduce power, and minimize costs.

Stratix II Family Features Summary

Adaptive Logic Modules (ALMs)	ALMs are part of a unique, innovative logic structure that delivers faster performance, minimizes area, and reduces power consumption. ALMs expand the traditional 4-input look-up table architecture to 7 inputs, increasing performance by reducing LEs, logic levels, and associated routing. In addition, ALMs maximize DSP performance with dedicated functionality to efficiently implement adder trees and other complex arithmetic functions.
MultiTrack™ Interconnect	Connections between LEs, TriMatrix™ memory blocks, DSP blocks, and device I/O pins are provided by the MultiTrack interconnect structure with DirectDrive™ technology. The MultiTrack interconnect consists of continuous, performance-optimized routing lines of different lengths and speeds used for inter- and intra-design block connectivity. The Quartus II compiler automatically places critical design paths on faster inter-connects to maximize performance.
TriMatrix Memory	TriMatrix memory in Stratix II FPGAs provides up to 9 Mbits of memory in three block sizes: 512 bits in the M512, 4 Kbits in the M4K, and 500 Kbits in the M-RAM blocks. TriMatrix memory includes parity checking and is capable of up to 550-MHz performance.
DSP Blocks	Each DSP block includes multipliers with associated pipelining, adders, and accumulators. Stratix II FPGAs include up to 96 DSP blocks offering 384 18-bit x 18-bit multipliers that operate at up to 450 MHz. Each multiplier can be configured as 9-bit x 9-bit, 18-bit x 18-bit, or 36-bit x 36-bit multipliers.
External Memory Interface Circuitry	Fully characterized and hardware-validated circuitry provides flexible, high-performance interfaces to the latest external DRAM and SRAM memory technologies. Complete solutions, including easy-to-use IP, hard-ware development platforms, and comprehensive timing analysis, are available to minimize risk and speed time to market.
High-Speed Differential I/O Support	Optimized LVDS I/O pins provide high performance and excellent signal integrity. Wizards make differential I/O configuration straightforward and easy.
Dynamic Phase Alignment (DPA)	DPA maximizes signal integrity and simplifies PCB layout and timing management for high-speed data trans-fer. DPA eliminates channel-to-channel and channel-to-clock skew in high-speed data transmission systems.

Stratix II Family Features Summary (Continued)	
On-Chip Termination	Serial and differential on-chip termination simplifies design and reduces component count. Digital calibration circuitry provides industry-leading on-chip termination tolerance within 5 percent.
Clock Management Features	Up to 12 PLLs and up to 48 system clocks. Advanced clock management features include PLL reconfiguration, spread-spectrum clocking, frequency synthesis, programmable phase shift, programmable delay shift, external feedback, and programmable bandwidth for all on- and off-chip clocking requirements.
Design Security	Configuration bitstream encryption using 128-bit advanced encryption standard (AES); prevents IP thefts and product tampering. The non-volatile key storage makes the solution reliable, easy to use, and low cost.
Remote System Upgrades	Enables reliable and safe deployment of in-system enhancements and bug fixes.
Hot Socketing and Power Sequencing	Robust on-chip hot-socketing and power-sequencing support ensures proper device operation independent of the power-up sequence.
Automatic Single Event Upset Detection Circuitry	Features automatic single event upset detection circuitry utilizing 32-bit CRC.
Nios II Embedded Processor Support	Nios II embedded processors reduce cost, increase flexibility, and offer an ideal replacement for low-cost discrete microprocessors. Nios II soft processor support for Stratix II FPGAs offers over 200-DMIPS performance.
HardCopy II Structured ASIC Support	Reduces cost for volume applications using this pin-compatible structured ASIC.

90-nm High-Performance, High-Density FPGAs With 6.375-Gbps Transceivers

Altera's Stratix II GX devices deliver all the benefits of Stratix II devices plus up to 20 low-power, high-speed transceiver channels. The transceivers support all data rates spanning from 622 Mbps to 6.375 Gbps. They have dynamically configurable transmit pre-emphasis and receiver equalization to optimize signal integrity under adverse channel conditions. The transceivers are capable of driving FR-4 backplanes at 6.375 Gbps and have proven to be interoperable with backplanes and transceivers from multiple vendors.

In addition, the physical coding sublayer (PCS) hard IP, which is part of the transceiver block, saves valuable LE resources and simplifies protocol support. Stratix II GX devices incorporate protocol-specific PCS blocks for the following protocols: the PCI Express, Common Electrical Interface 6.375 Gbps (CEI-6G), serial digital interface (SDI), XAUI, SONET, Gigabit Ethernet, serial RapidIO™, and SerialLite II protocols. Stratix II GX devices also have 8b/10b encoder/decoders that are bypassable for proprietary protocols.

Stratix II GX Family Features Summary	
Excellent Signal Integrity 622 Mbps–6.375 Gbps	The transmitter has low jitter generation and up to 500 percent pre-emphasis. The receiver has excellent jitter tolerance and up to 17-dB equalization.
Low Power	The transceiver dissipates 225 mW per channel at 6.375 Gbps and only 125 mW per channel at 3.125 Gbps.
PCS Support (Hard IP)	The transceiver supports the following PCS blocks: PCI Express, PIPE-Compliant PCS, CEI-6G, 8b/10b encoder/decoder, XAUI state machine and channel bonding, Gigabit Ethernet state machine, SONET, and 8/10/16/20/32/40-bit interface (to FPGA).
System-Level Diagnostics	Serial loopback, reverse serial loopback, psuedo-random binary sequence (PRBS) generator checker, and register-based interface facilitates dynamic reconfiguration of pre-emphasis, equalization, and differential output voltage.

130-nm High-Performance, High-Density FPGAs

The density of Stratix devices ranges from 10,570 to 79,040 LEs, with up to 7 Mbits of embedded RAM and 88 18-bit x 18-bit multipliers. Stratix devices have up to 12 PLLs, 40 system clocks, and support for many single-ended and differential I/O electrical standards. Stratix FPGAs are based on a 1.5-V, 130-nm, all-layer-copper SRAM process. For new designs, Stratix II devices provide better performance and cost attributes than Stratix devices.

Stratix Family Features Summary	
MultiTrack Interconnect	Connections between LEs, TriMatrix memory blocks, DSP blocks, and device I/O pins are provided by the MultiTrack interconnect structure with DirectDrive technology. The MultiTrack interconnect consists of continuous, performance-optimized routing lines of different lengths and speeds used for inter- and intra-design block connectivity. The Quartus II compiler automatically places critical design paths on faster interconnects to maximize performance.
TriMatrix Memory	TriMatrix memory in Stratix FPGAs provides up to 7 Mbits of memory in three block sizes: 512 bits in the M512, 4 Kbits in the M4K, and 500 Kbits in the M-RAM blocks. TriMatrix memory includes parity checking and is capable of up to 320-MHz performance.
DSP Blocks	Each DSP block includes four 18-bit x 18-bit multipliers with associated pipelining, adders, and accumulators. Configurations can support any bit-width up to 36 bits x 36 bits. Stratix FPGAs include up to 22 DSP blocks offering 88 18-bit x 18-bit multipliers that operate at up to 275 MHz.
High-Speed Differential I/O Support	Optimized LVDS I/O pins provide high performance and excellent signal integrity. Wizards make differential I/O configuration straightforward and easy.
On-Chip Termination	Serial and differential on-chip termination simplifies design and reduces component count. Digital calibration circuitry provides industry-leading on-chip termination tolerance.
Clock Management Features	Up to 12 PLLs and up to 48 system clocks. Advanced clock management features include PLL reconfiguration, spread-spectrum clocking, frequency synthesis, programmable phase shift, programmable delay shift, external feedback, and programmable bandwidth for all on- and off-chip clocking requirements.
Remote System Upgrades	Enables reliable, safe deployment of in-system upgrades and bug fixes.
Hot Socketing and Power Sequencing	Robust on-chip hot-socketing and power-sequencing support that ensures proper device operation independent of the power-up sequence.
Automatic Single Event Upset Detection Circuitry	Features automatic single event upset detection circuitry utilizing 32-bit CRC.
Nios II Embedded Processor Support	Nios II embedded processors reduce cost, increase flexibility, and offer an ideal replacement for low-cost discrete microprocessors. Nios II soft processor support for Stratix FPGAs offers over 150-DMIPS performance.
HardCopy Structured ASIC Support	Reduces cost for volume applications using this pin-compatible structured ASIC.

130-nm High-Performance, High-Density FPGAs With 3.1875-Gbps Transceivers

Stratix GX FPGAs combine Altera's second-generation transceivers with the award-winning Stratix FPGA architecture. Stratix GX FPGAs have up to 20 transceivers operating from 500 Mbps to 3.1875 Gbps, which can easily drive 40-inch backplanes. Stratix GX devices, with their excellent built-in jitter control circuitry and tolerance, transmit pre-emphasis, receiver equalization, and 8b/10b encoder/decoder circuitry, deliver a robust transceiver solution.

Stratix GX devices also incorporate dedicated serializer/deserializer (SERDES) and DPA circuitry into 45 source-synchronous differential I/O pins, enabling the devices to operate at up to 1 Gbps. DPA automatically compensates for clock-to-channel skew on a channel-per-channel basis, thereby simplifying board layout and design. For new designs, Stratix II GX devices provide better performance and cost attributes than Stratix GX devices.

Stratix GX Family Features Summary	
500-Mbps–3.1875-Gbps Transceiver Blocks	Embedded transceiver blocks, including 8b/10b encoder/decoder circuitry, provide support for high-speed applications, such as: SerialLite II, XAUI, Gigabit Ethernet, 1G, 2G, and 10G Fibre Channel, Serial RapidIO, SONET/SDH (synchronous digital hierarchy), PCI Express, OBSAI, and SDI.
Excellent Drive Strength Capability	Transceiver capabilities, embedded programmable transmit pre-emphasis, and embedded receiver equalization combine to enable signal drive capability across a 40-inch FR4 backplane and two backplane connectors.
Low Power Consumption	450-mW power consumption per 4-channel transceiver block simplifies board design.
Source-Synchronous Differential I/O Signaling With DPA	Support for high-speed I/O standards and high-speed interfaces such as 10 Gigabit Ethernet XSBI, SFI-4, SPI-4 Phase 2 (packet over SONET (POS)-PHY Level 4), HyperTransport™ technology, and parallel RapidIO standards, at up to 1 Gbps to complement transceiver bandwidth.
DPA	Maximizes signal integrity and simplifies PCB layout and timing management for high-speed data transfer. Eliminates channel-to-channel and channel-to-clock skew in high-speed data transmission systems.
High-Performance Stratix Architecture	Highly optimized FPGA architecture provides innovative routing for block-based design and maximum system performance. Features such as TriMatrix memory, DSP blocks, and clock management circuitry enable full system implementation.

Stratix FPGA Series Package & I/O Matrices

342 Number indicates available user I/O pins.

Vertical migration (Same V_{CC}, GND, ISP, and input pins). User I/O may be less than labelled for vertical migration.

All Stratix series devices are offered in commercial and industrial temperatures and lead-free packages.

		Stratix II (1.2 V) High Density, High Performance						Stratix II GX (1.2 V) 6.375-Gbps Transceivers							
		EP2S15	EP2S30	EP2S60	EP2S90	EP2S130	EP2S180	EP2SGX30C	EP2SGX30D	EP2SGX60C	EP2SGX60D	EP2SGX60E	EP2SGX90E	EP2SGX90F	EP2SGX130G
FineLine BGA (F)	484-Pin FBGA (FlipChip)	342	342	334											
	672-Pin FBGA (FlipChip)	366	500	492											
	780-Pin FBGA				534	534		372	372	364	364				
	1,020-Pin FBGA			718	758	742	742								
	1,152-Pin FBGA											534	558		
	1,508-Pin FBGA				902	1,126	1,170							650	798
Hybrid FBGA (H)	484-Pin HFBGA				308										

356 Number indicates available user I/O pins.

Vertical migration (Same V_{CC}, GND, ISP, and input pins). User I/O may be less than labelled for vertical migration.

All Stratix series devices are offered in commercial and industrial temperatures and lead-free packages.

		Stratix (1.5 V) High Density, High Performance							Stratix GX (1.5 V) 3.1875-Gbps Transceivers						
		EP1S10	EP1S20	EP1S25	EP1S30	EP1S40	EP1S60	EP1S80	EP1SGX10C	EP1SGX10D	EP1SGX25C	EP1SGX25D	EP1SGX25F	EP1SGX40D	EP1SGX40G
Ball-Grid Array (B)	672-Pin BGA	356	426	473											
	956-Pin BGA				683	683	683	683							
FineLine BGA (F)	484-Pin FBGA (FlipChip)	335	361												
	672-Pin FBGA (Wirebond)	345	426	473											
	672-Pin FBGA (FlipChip)								330	330	426	426			
	780-Pin FBGA	426	586	697	589	615									
	1,020-Pin FBGA			706	726	773	773	773				542	542	548	548
	1,508-Pin FBGA					822	1,022	1,203							

Stratix FPGA Series Features

		Stratix II (1.2 V) HIgh Density, High Performance						Stratix II GX (1.2 V) 6.375-Gbps Transceivers							
		EP2S15	EP2S30	EP2S60	EP2S90	EP2S130	EP2S180	EP2SGX30C	EP2SGX30D	EP2SGX60C	EP2SGX60D	EP2SGX60E	EP2SGX90E	EP2SGX90F	EP2SGX130G
Density & Speed	Equivalent LEs	15,600	33,880	60,440	90,960	132,540	179,400	33,880	33,880	60,440	60,440	60,440	90,960	90,960	132,540
	ALMs	6,240	13,552	24,176	36,384	53,016	71,760	13,552	13,552	24,176	24,176	24,176	36,384	36,384	53,016
	Adaptive Look-Up Tables (ALUTs)	12,480	27,104	48,352	72,768	106,032	143,520	27,104	27,104	48,352	48,352	48,352	72,768	72,768	106,032
	Total RAM Bits (K)[1]	419	1,369	2,544	4,520	6,747	9,383	1,369	1,369	2,544	2,544	2,544	4,520	4,520	6,747
	M512 RAM Blocks (512 Bits + 64 Parity Bits)	104	202	329	488	699	930	202	202	329	329	329	488	488	699
	M4K RAM Blocks (4 Kbits + 512 Parity Bits)[2]	78	144	255	408	609	768	144	144	255	255	255	408	408	609
	M-RAM Blocks (512 Kbits + 65,536 Parity Bits)[2]	0	1	2	4	6	9	1	1	2	2	2	4	4	6
	Speed Grades (Fastest to Slowest)	-3, -4, -5	-3, -4, -5	-3, -4, -5	-3, -4, -5	-3, -4, -5	-3, -4, -5	-3, -4, -5	-3, -4, -5	-3, -4, -5	-3, -4, -5	-3, -4, -5	-3, -4, -5	-3, -4, -5	-3, -4, -5

[1] K = 1,000

[2] Kbits = 1,024 bits

Stratix FPGA Series Features (Continued)

		Stratix II (1.2 V) HIgh Density, High Performance						Stratix II GX (1.2 V) 6.375-Gbps Transceivers							
		EP2S15	EP2S30	EP2S60	EP2S90	EP2S130	EP2S180	EP2SGX30C	EP2SGX30D	EP2SGX60C	EP2SGX60D	EP2SGX60E	EP2SGX90E	EP2SGX90F	EP2SGX130G
Architectural Features	Embedded Processor Available	Nios II						Nios II							
	DSP Blocks	12	16	36	48	63	96	16	16	36	36	36	48	48	63
	18-Bit x 18-Bit/9-Bit x 9-Bit Embedded Multipliers	48/96	64/128	144/288	192/384	252/504	384/768	64/128	64/128	144/288	144/288	144/288	19/384	19/384	252/504
	I/O Registers per I/O Element	6	6	6	6	6	6	6	6	6	6	6	6	6	6
	True Dual-Port RAM	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Global & Regional Clock Networks	48	48	48	48	48	48	48	48	48	48	48	48	48	48
	PLLs/Unique Outputs	6/28	6/28	12/56	12/56	12/56	12/56	4/18	4/18	8/36	8/36	8/36	8/36	8/36	8/36
	Design Security	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	HardCopy II Device Support	–	✓	✓	✓	✓	✓	–	–	–	–	–	–	–	–
Configuration Devices	Configuration File Size (Mbits)	5	10	17	28	40	53	10	10	17	17	17	28	28	40
	Number of EPCS4 Devices (4 Mbits)	1	–	–	–	–	–	–	–	–	–	–	–	–	–
	Number of EPCS16 Devices (16 Mbits)	1	1	1	–	–	–	1	1	1	1	1	–	–	–
	Number of EPCS64 Devices (64 Mbits)	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Number of EPC2 Devices (1.6 Mbits)	2	4	7	11	16	21	4	4	7	7	7	11	11	16
	Number of EPC4 Devices (4 Mbits)	1	–	–	–	–	–	–	–	–	–	–	–	–	–
	Number of EPC8 Devices (8 Mbits)	1	1	1	–	–	–	1	1	1	1	1	–	–	–
	Number of EPC16 Devices (16 Mbits)	1	1	1	–	–	–	1	1	1	1	1	–	–	–
I/O Features	I/O Levels Supported (V)	1.5, 1.8, 2.5, 3.3						1.5, 1.8, 2.5, 3.3							
	I/O Standards Supported	LVDS, LVPECL, HyperTransport, Differential SSTL-18, Differential SSTL-2, Differential HSTL, SSTL-18 (I & II), SSTL-2 (I & II), 1.5-V HSTL (I & II), 1.8-V HSTL (I & II), PCI, PCI-X 1.0, LVTTL, LVCMOS													
	True-LVDS™ Maximum Data Rate (Mbps)	125–1,250						125–1,250							
	True-LVDS Channels (Receive/Transmit)	38/38	58/58	80/84	114/118	152/156	152/156	29/29	29/29	42/42	42/42	42/42	59/59	59/59	78/78
	Embedded DPA Circuitry	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Series & Differential On-Chip Termination	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Programmable Drive Strength	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Transceiver (SERDES) Data Rate Range	–	–	–	–	–	–	622 Mbps–6.375 Gbps							
	Transceiver (SERDES) Channels	–	–	–	–	–	–	4	8	4	8	12	12	16	20
External Memory Interfaces	Memory Devices Supported	QDRII, DDR2, RLDRAM II, DDR, SDR						QDRII, DDR2, RLDRAM II, DDR, SDR							
	MegaCore Controller With Clear-Text Datapath	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	System Timing Analysis	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Board Layout Guidelines	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

Stratix FPGA Series Features (Continued)

		Stratix (1.5 V) High Density, High Performance							Stratix GX (1.5 V) 3.1875-Gbps Transceivers						
		EP1S10	EP1S20	EP1S25	EP1S30	EP1S40	EP1S60	EP1S80	EP1SGX10C	EP1SGX10D	EP1SGX25C	EP1SGX25D	EP1SGX25F	EP1SGX40D	EP1SGX40G
Density & Speed	LEs	10,570	18,460	25,660	32,470	41,250	57,120	79,040	10,570	10,570	25,660	25,660	25,660	41,250	41,250
	Total RAM Bits (K)[1]	920	1,669	1,944	3,317	3,423	5,215	7,427	920	920	1,944	1,944	1,944	3,423	3,423
	M512 RAM Blocks (512 Bits + 64 Parity Bits)	94	194	224	295	384	574	767	94	94	224	224	224	384	384
	M4K RAM Blocks (4 Kbits + 512 Parity Bits)[2]	60	82	138	171	183	292	364	60	60	138	138	138	183	183
	M-RAM Blocks (512 Kbits + 65,536 Parity Bits)[2]	1	2	2	4	4	6	9	1	1	2	2	2	4	4
	Speed Grades (Fastest to Slowest)	-5, -6, -7	-5, -6, -7	-5, -6, -7	-5, -6, -7	-5, -6, -7	-5, -6, -7	-5, -6, -7	-5, -6, -7	-5, -6, -7	-5, -6, -7	-5, -6, -7	-5, -6, -7	-5, -6, -7	-5, -6, -7
Architectural Features	Embedded Processor Available	Nios II							Nios II						
	DSP Blocks	6	10	10	12	14	18	22	6	6	10	10	10	14	14
	18-Bit x 18-Bit/9-Bit x 9-Bit Embedded Multipliers	24/48	40/80	40/80	48/96	56/112	72/144	88/176	24/48	24/48	40/80	40/80	40/80	56/112	56/112
	I/O Registers per I/O Element	6	6	6	6	6	6	6	6	6	6	6	6	6	6
	True Dual-Port RAM	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Global & Regional Clock Networks	36	36	36	40	40	40	40	36	36	36	36	36	40	40
	PLLs/Unique Outputs	6/32	6/32	6/32	10/40	12/52	12/52	12/52	4/26	4/26	4/26	4/26	4/26	8/42	8/42
	HardCopy Device Support	–	–	✓	✓	✓	✓	✓	–	–	–	–	–	–	–
Configuration Devices	Configuration File Size (Mbits)	3.53	5.9	7.89	10.38	12.39	17.54	23.83	3.58	3.58	7.95	7.95	7.95	12.53	12.53
	Number of EPC2 Devices (1.6 Mbits)	3	4	5	7	8	11	15	3	3	5	5	5	8	8
	Number of EPC4 Devices (4 Mbits)	1	1	–	–	–	–	–	1	1	–	–	–	–	–
	Number of EPC8 Devices (8 Mbits)	1	1	1	1	1	–	–	–	–	–	1	1	1	1
	Number of EPC16 Devices (16 Mbits)	1	1	1	1	1	1	1	1	1	1	1	1	1	1
I/O Features	I/O Voltage Levels Supported (V)	1.5, 1.8, 2.5, 3.3							1.5, 1.8, 2.5, 3.3						
	I/O Standards Supported	LVDS, LVPECL, HyperTransport, 3.3-V PCML, Differential SSTL-2, Differential HSTL, SSTL-18 (I & II), SSTL-2 (I & II), SSTL-3 (I & II), 1.5-V HSTL (I & II), 1.8-V HSTL (I & II), PCI, Compact-PCI, PCI-X 1.0, AGP (1x & 2x), GTL, GTL+, CTT, LVTTL, LVCMOS)													
	True-LVDS Maximum Data Rate (Mbps)	840							1000						
	True-LVDS Channels (Receive/ Transmit)	44/44	66/66	78/78	80/80	80/80	80/80	80/80	44/44	44/44	78/78	78/78	78/78	80/80	80/80
	Medium-Speed LVDS Channels	–	–	–	462	462	462	462	–	–	–	–	–	–	–
	Embedded DPA Circuitry	–	–	–	–	–	–	–	✓	✓	✓	✓	✓	✓	✓
	Series & Differential On-Chip Termination	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Programmable Drive Strength	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Transceiver (SERDES) Data Rate Range	–	–	–	–	–	–	–	500 Mbps–3.1875 Gbps						
	Transceiver (SERDES) Channels	–	–	–	–	–	–	–	4	8	4	8	16	8	20
External Memory Interface	Memory Devices Supported	QDRII, QDR, ZBT, DDR, SDR							QDRII, QDR, ZBT, DDR, SDR						
	MegaCore Controller With Clear-Text Datapath	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	System Timing Analysis	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Board Layout Guidelines	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

[1] K = 1,000

[2] Kbits = 1,024 bits

FOR MORE INFORMATION

Stratix II FPGAs	www.altera.com/stratix2
Stratix II GX Transceiver FPGAs	www.altera.com/stratix2gx
Stratix FPGAs	www.altera.com/stratix
Stratix GX Transceiver FPGAs	www.altera.com/stratixgx
Training	www.altera.com/training

HardCopy Structured ASIC Series

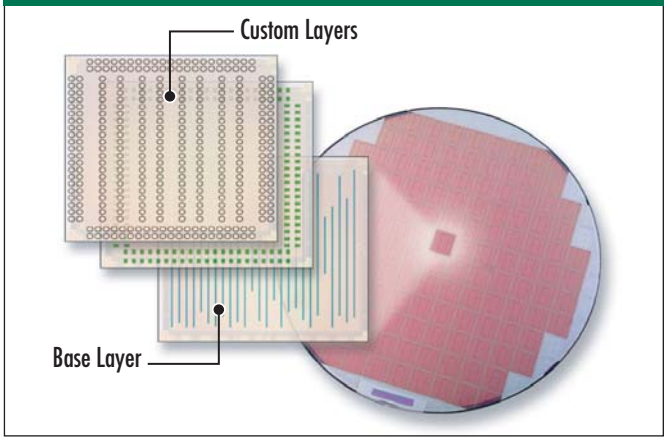
Altera's HardCopy series is the industry's most compelling structured ASIC solution. With its unique FPGA front-end design flow, you can use Altera's Stratix series of high-density, high-performance FPGAs to develop, verify, and finalize your system design before committing to silicon. The product development flexibility and time-to-market benefits of the HardCopy series are not available from other offerings in the market.

Structured ASICs bridge the gap between standard-cell ASIC technology and FPGAs, offering low unit costs combined with faster development times. Structured ASICs start with standard, pretested base layers of logic and hard IP, and the proprietary design is then implemented on the top few metal layers. HardCopy structured ASICs are the only devices to offer a seamless prototype-to-production process for guaranteed success. Use your existing design environment to use Altera's Stratix FPGAs series as your design's front end and then test it in-system. When you're done, Altera's HardCopy Design Center seamlessly migrates your design to HardCopy structured ASICs in seven to eleven weeks.

Key Features

- In-system and in-silicon high-volume design verification
- Turnkey migration from the FPGA prototype to low-cost, high-volume structured ASICs
- Drop-in replacement for the FPGA prototype
- Can be designed with standard synthesis, verification, timing analysis, and equivalency checking tools from Cadence, Mentor Graphics, Synopsys, and Synplicity in conjunction with Altera's Quartus II software
- Support for the Nios II embedded processor

Structured ASIC



HardCopy™ II

90-nm Structured ASICs With Guaranteed Success

Introduced in January 2005, the 1.2-V, 90-nm HardCopy II family builds on the success of Altera's first two generations of structured ASICs. Using Stratix II FPGAs for prototyping and testing, and then migrating to HardCopy II devices, you are guaranteed success with your high-volume production devices. HardCopy II devices offer 2.2 million ASIC gates for logic prototyping, 8.8 million bits of memory, and over 350-MHz system performance. Compared to the FPGA prototype, HardCopy II devices offer over 50 percent core power reduction at as little as one-tenth the cost. HardCopy II devices are built on a fine-grained architecture designed for low cost that is made up of an array of HCells. The HCell architecture supports seamless FPGA migration while providing the density, cost, performance, and power benefits of ASIC technology.

HardCopy II Family Features Summary

Clock Management	Up to 12 programmable PLLs, providing robust clock management and frequency synthesis capabilities for maximum system performance. The PLLs provide high-end features, including clock switchover, PLL reconfiguration, spread-spectrum clocking, frequency synthesis, programmable phase shift, programmable delay shift, external feedback, and programmable bandwidth.
Differential I/O Support	Support for high-speed differential I/O for data rates up to 1 Gbps to address the high-performance needs of emerging I/O interfaces, including support for the LVDS, LVPECL, and HyperTransport standards.
External Memory Interfaces	Advanced external memory interface support, allowing you to integrate external high-density SRAM and DRAM devices into complex system designs without degrading data-access performance.
On-Chip Termination	Series and differential on-chip termination support can simplify board layout by minimizing the number of external resistors needed on the PCB.
Single-Ended I/O Standards	High-bandwidth, single-ended I/O interface standards support (SSTL, HSTL, PCI, and PCI-X) for today's demanding system requirements.
Source-Synchronous Protocols	Support for a wide array of high-speed interface standards, including the SPI-4.2, SFI-4, 10 Gigabit Ethernet XSBI, and RapidIO standards.
TriMatrix Memory	Up to 8.8 Mbits of RAM. This advanced memory structure consists of M4K and M-RAM embedded RAM blocks that can be configured to support a wide range of features.

HardCopy™

130-nm Structured ASICs With Guaranteed Success

Altera's HardCopy Stratix family is manufactured on 1.5-V, 130-nm process technology. These devices use Stratix FPGAs for prototyping and have the same LE architecture as Stratix devices. With 300,000 to 1,000,000 ASIC gates and up to 5,600,000 bits of memory, HardCopy Stratix devices offer a 50 percent performance increase and 40 percent lower power consumption than the Stratix prototype. HardCopy Stratix devices support a wide range of high-speed interfaces—including the SPI-4 Phase 2, 10-Gigabit Ethernet XSBI, and RapidIO interfaces. HardCopy Stratix devices also support the LVDS, LVPECL, and HyperTransport high-speed I/O standards. These advanced capabilities allow designers to connect high-speed memory devices like QDR and zero-bus turnaround (ZBT) SRAMs.

HardCopy Stratix Family Features Summary	
Clock Management	Support for up to 12 programmable PLLs and 40 system clocks.
Differential I/O Support	Up to 152 high-speed differential I/O channels with 80 channels optimized for data rates up to 840 Mbps, and support for emerging I/O interfaces including the LVDS, LVPECL, PCML, and HyperTransport standards.
DSP Blocks	Up to 22 DSP blocks.
DSP Performance	Up to 463 giga multiply-accumulate operations per second (GMACS) of DSP throughput.
Embedded Test Capability	Available.
External Memory Interfaces	External memory interface to high-density SRAM and DRAM devices.
High-Speed Interfaces	Support for a wide array of high-speed interface standards, such as the SPI-4 Phase 2, SFI-4, 10G Ethernet XSBI, HyperTransport, RapidIO, and UTOPIA IV standards.
On-Chip Termination	Support for differential on-chip termination.
Single-Ended I/O Support	Support for high-bandwidth single-ended I/O interface standards, such as SSTL, HSTL, GTL, GTL+, CTT, and PCI-X.
TriMatrix Memory	Up to 5.6 Mbits of TriMatrix memory.

HardCopy Structured ASIC Series Package & I/O Matrix

951 Number indicates available user I/O pins.

All HardCopy series devices are offered in commercial and industrial temperatures and lead-free packages.

		HardCopy II (1.2 V) Structured ASIC					HardCopy Stratix (1.5 V) Structured ASIC				
		HC210W	HC210	HC220	HC230	HC240	HC1S25	HC1S30	HC1S40	HC1S60	HC1S80
FineLine BGA (F)	484-Pin FBGA (Wirebond)	300									
	484-Pin FBGA (FlipChip)		334								
	672-Pin FBGA (Wirebond)						473				
	672-Pin FBGA (FlipChip)			492							
	780-Pin FBGA			494				597	615		
	1,020-Pin FBGA				698	742				773	773
	1,508-Pin FBGA					951					

HardCopy Structured ASIC Series Features

		HardCopy II (1.2 V) Structured ASIC					HardCopy Stratix (1.5 V) Structured ASIC				
		HC210W	HC210	HC220	HC230	HC240	HC1S25	HC1S30	HC1S40	HC1S60	HC1S80
Density & Speed	ASIC Gates	1,000,000	1,000,000	1,600,000	2,200,000	2,200,000	–	–	–	–	–
	Additional Gates for DSP Blocks	0	0	300,000	700,000	1,400,000	–	–	–	–	–
	LEs	–	–	–	–	–	25,660	32,470	41,250	57,120	79,040
	Total RAM Bits	875,520	875,520	3,059,712	6,368,256	8,847,360	1,944,576	2,137,536	2,244,096	5,215,104	5,658,048
	M512 RAM Blocks (512 Bits + 64 Parity Bits)	–	–	–	–	–	224	295	384	574	767
	M4K RAM Blocks (4 Kbits + 512 Parity Bits)[1]	190	190	408	614	768	138	171	183	292	364
	M-RAM Blocks (512 Kbits + 65,536 Parity Bits)[1]	0	0	2	6	9	2	2	2	6	6
	Speed Grades (Fastest to Slowest)	–	–	–	–	–	–	–	–	–	–
Architectural Features	Embedded Processor Available	Nios II					Nios II				
	DSP Blocks	Implemented in HCell Macros					10	12	14	18	22
	18-Bit x 18-Bit/9-Bit x 9-Bit Embedded Multipliers	Implemented in HCell Macros					40/80	48/96	56/112	72/144	88/176
	I/O Registers per I/O Element	6	6	6	6	6	6	6	6	6	6
	True Dual-Port RAM	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Global & Regional Clock Networks	16/32	16/32	16/32	16/32	16/32	36	40	40	40	40
	PLLs	4	4	4	8	12	6	6	6	12	12
I/O Features	I/O Voltage Levels Supported (V)	1.5, 1.8, 2.5, 3.3					1.5, 1.8, 2.5, 3.3				
	I/O Standards Supported	LVDS, LVPECL, HyperTransport, Differential SSTL-18, Differential SSTL-2, Differential HSTL, SSTL-18 (I & II), SSTL-2 (I & II), 1.5-V HSTL (I & II), 1.8-V HSTL (I & II), PCI, PCI-X 1.0, LVTTL, LVCMOS										
	External Memory Device Interfaces	QDRII, DDR2, RLDRAM II, DDR, SDR					QDRII, QDR, ZBT, DDR, SDR				
	True-LVDS Maximum Data Rate (Mbps)	125–1,000					840				
	True-LVDS Channels (Receive/Transmit)	19/21	19/21	29/31	42/42	118/118	78/78	80/80	80/80	80/80	80/80
	Medium-Speed LVDS Data Rate (Mbps) (Receive/Transmit)	–	–	–	–	–	–	2/2	10/10	36/36	46/72
	Series & Differential On-Chip Termination	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	FPGA Prototype Options	EP2S30 EP2S60 EP2S90	EP2S30 EP2S60 EP2S90	EP2S60 EP2S90 EP2S130	EP2S90 EP2S130 EP2S180	EP2S180	EP1S25	EP1S30	EP1S40	EP1S60	EP1S80

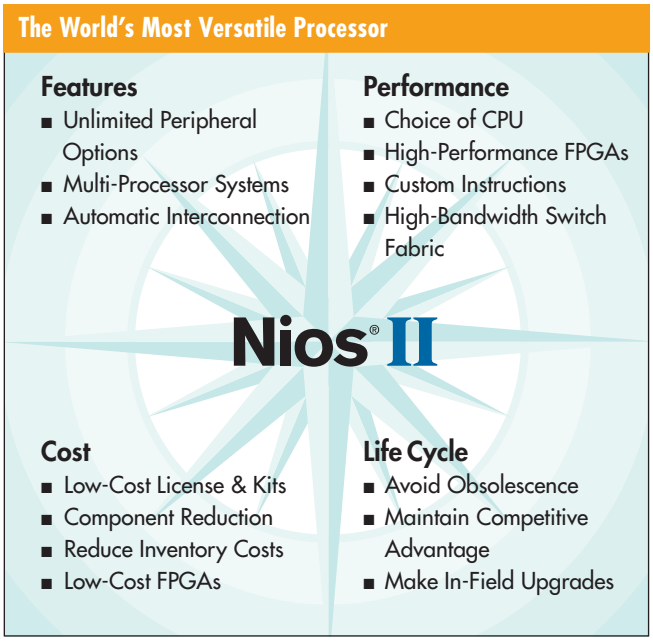
[1] Kbits = 1,024 bits

FOR MORE INFORMATION

HardCopy Structured ASIC Series	www.altera.com/hardcopy
HardCopy II Structured ASICs	www.altera.com/hardcopy2
HardCopy Stratix Structured ASICs	www.altera.com/hardcopystratix
Training	www.altera.com/training

Nios II Embedded Processors

Altera's Nios II embedded processors deliver the perfect fit every time with fully customizable features and performance, low product and implementation costs, ease of use and adaptability, and obsolescence-proof design. The three processors in the Nios II family—fast (Nios II/f), standard (Nios II/s), and economy (Nios II/e)—are each optimized for a specific price and performance range. You can easily add Nios II processors to your systems by using the SOPC Builder system development tool found within Altera's industry-leading Quartus II design software.



Nios® II

The World's Most Versatile Processor

The Nios II family of embedded 32-bit RISC processors delivers more than 200 DMIPS of performance and costs as little as 35 cents to implement in an FPGA. Because of the flexible, soft-core nature of Nios II processors, you can choose from an unlimited combination of system configurations to meet your performance, feature, and cost targets. Designing with Nios II processors lets you deploy products to market faster, extend your product's life cycle, and avoid processor obsolescence. Supported by a rich collection of tools and operating systems from Altera and Altera partners, the Nios II processor is used by more designers than any other configurable microprocessor.

To see what other Nios II users are doing with their projects, join the online community of Nios II developers at the Nios Community Forum. There you can also download code examples and other software such as the µClinux and eCos operating systems.

Nios II Family Features Summary

Feature	Nios II/f (Fast)	Nios II/s (Standard)	Nios II/e (Economy)
Description	Optimized for maximum performance	Balanced cost and performance	Optimized for minimum logic usage
Pipeline	6 Stage	5 Stage	1 Stage
Multiplier	1 Cycle	3 Cycle	Emulated in software
Branch Prediction	Dynamic	Static	None
Instruction Cache	Configurable	Configurable	None
Data Cache	Configurable	None	None
Custom Instructions	Up to 256	Up to 256	Up to 256

Nios II Integrated Development Environment

The Nios II integrated development environment (IDE) is the primary software development tool for the Nios II family of embedded processors. You can complete all software development tasks within the Nios II IDE, including project management, editing and compiling, debugging, and programming flash devices.

With a PC, an Altera FPGA, and a JTAG download cable, you have everything you need to develop and debug Nios II processor-based systems. The Nios II IDE is based on the open, extensible Eclipse IDE project and the Eclipse C/C++ Development Tools Project.

Nios II IDE Features Summary

Project Manager	
New Project Wizard	The New Project Wizard is used to automate the setup of C/C++ application projects and system library projects.
Software Project Templates	Software project templates help software engineers bring up working systems as quickly as possible. Each template is a collection of software files and project settings. You can add your own source code to the project by placing the code in the project directory or by importing the files into the project.
Software Components	Software components provide an easy way to configure your system for your specific target hardware. Software components include: ▪ Nios II run-time library, known as the hardware abstraction layer (HAL) ▪ Lightweight IP TCP/IP stack ▪ MicroC/OS-II real-time operating system (RTOS) ▪ Zip file system
Editor and Compiler	
Text Editor	The Nios II IDE text editor is a full-featured source editor that includes: ▪ Syntax highlighting in C/C++ ▪ Code assist and code completion ▪ Comprehensive search facilities ▪ File management ▪ Extensive online help topics and tutorials ▪ Import assistance ▪ Quick fix auto-corrections ▪ Integrated debugging features
C/C++ Compiler	Based on the industry-standard GNU tool chain, the Nios II IDE provides a GUI for the GNU C compiler (GCC). The Nios II IDE build environment automatically produces a makefile based on your specific system configuration. Changes you make in the Nios II IDE compiler/linker settings are automatically reflected in this auto-generated makefile.
Debugger	
Basic Debug	The Nios II IDE debugger connects to the target hardware through the JTAG debug module on the Nios II processor core. The Nios II IDE debugger contains debug features such as: ▪ Run control ▪ Call stack view ▪ Software breakpoints ▪ Disassembly code view (source, assembly, and mixed display) ▪ Debug information view ▪ Instruction set simulator (ISS) target
Advanced Debug	In addition to the basic debug features, the Nios II IDE debugger also has several advanced debugging capabilities, such as: ▪ Hardware breakpoints for debugging code in ROM or flash ▪ Data triggers ▪ Instruction trace
Debug Information View	The debug information view provides you with access to local variables, registers, memory, breakpoints, and expression evaluation functions.
Targets	The Nios II IDE debugger can connect to these targets types: ▪ Hardware (via JTAG) ▪ Instruction set simulator ▪ Hardware logic simulator
Flash Programmer	
Flash Programmer	Using the Nios II IDE flash programmer, you can program any CFI-compliant flash device connected to the FPGA. In addition to CFI flash, the Nios II IDE flash programmer can program any Altera serial configuration device connected to the FPGA. The Nios II IDE flash programmer is pre-configured to work with all of the boards available in the Nios II development kits, and can be easily ported to any custom hardware.

FOR MORE INFORMATION

Nios II Embedded Processors	www.altera.com/nios2
Nios II Development Kits	www.altera.com/nioskits
Third-Party Software Tool Support	www.altera.com/niospartners
Nios Community Forum	www.niosforum.org
Eclipse Project	www.eclipse.org

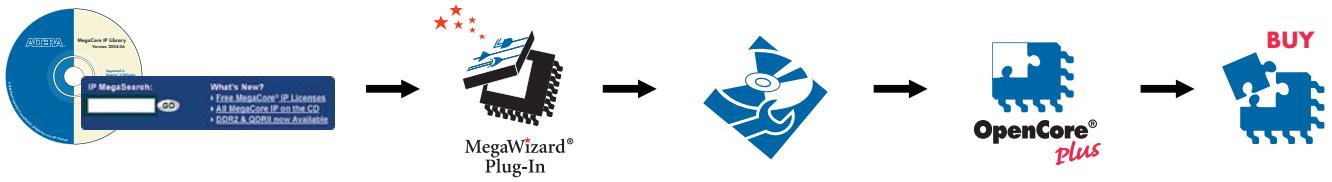
Intellectual Property Solutions

Altera's portfolio of IP solutions includes hundreds of easy-to-use IP cores. Also known as megafunctions, the IP cores are high-quality "building blocks" you can drop into your system designs instead of creating complete designs from scratch.

Altera IP MegaCore functions are easy-to-use, pre-verified, configurable, off-the-shelf IP cores. These megafunctions are optimized for the latest Altera devices and are fully supported in Quartus II design software. In addition, leading third-party IP vendors who are members of the Altera Megafunction Partners Program (AMPP℠) develop and optimize their IP products for Altera devices and license them directly to Altera customers. Many AMPP partners can provide custom integrated system-on-a-programmable-chip (SOPC) solutions. Altera also has partnerships with leading software vendors to deliver processor-based SOPC software solutions.

Discover how quickly you can use these cores to accelerate your design time, lower development costs, speed your time to market, and give your systems a competitive edge.

Altera IP Design Flow



Install From the CD or Download From the Web | Parameterize | Evaluate Using Industry-Standard EDA Tools | Evaluate in Hardware | Purchase

Designing With Altera IP Megafunctions

Install	Visit the IP MegaStore™ website to quickly find and download megafunctions from Altera's comprehensive portfolio.
Parameterize	Use Altera's powerful, user-friendly MegaWizard® Plug-In Managers to parameterize megafunctions, select the right features for your needs, estimate resources, set up third-party tools, and generate all files necessary for integrating parameterized megafunctions into your design.
Evaluate Using Industry-Standard EDA Tools	During simulation, evaluate all the features of the megafunction before you buy, including functionality, size, and speed in your system with the OpenCore® evaluation feature.
Evaluate in Hardware	Generate time-limited FPGA programming files using the OpenCore Plus hardware evaluation feature, and then use the files to verify your complete FPGA design on your own hardware—or any other available board—all before you decide to purchase an IP license.
Purchase	When you are completely satisfied with the megafunction and are ready to take your design into production, purchase the license and generate the production device programming files. Altera MegaCore licenses are for perpetual use, support multiple projects, and include upgrades and support for one year. Floating and node-locked licenses are available for all of Altera's MegaCore functions. AMPP functions are offered under a variety of different licensing terms, conditions, and pricing models. Contact the AMPP partners directly for details.

IP MegaStore Website

Visit the IP MegaStore website for a complete listing of all Altera's megafunctions for processors, interfaces, DSP, and communications. The website also includes information on evaluating and purchasing Altera and Altera's partners' IP cores, as well as available system integration and tools support.

IP MegaStore Website Overview	
IP Megafunctions	
Communications IP	IP cores ideal for telecom, datacom, and storage applications.
DSP IP	IP cores used for digital modulation, image, video, and high-speed DSP applications.
Embedded Processor IP	Versatile embedded processors with a wide range of peripherals, development kits, and software tools.
Interface and Peripheral IP	Extensive portfolio of standard memory and system interfaces.
Information and Services	
Free IP Evaluation	Information on simulating the behavior of a megafunction within your system, verifying the functionality of your design, evaluating its size and speed, generating time-limited device programming files, and verifying the design in hardware.
IP Certifications	Overview of SOPC Builder Ready, DSP Builder Ready, Atlantic™ Compliant, and I-Tested certifications.
IP Licensing	Instructions on how to request a license for an Altera software product from the Altera website and have the license file sent via email complete with installation instructions.
Documentation	Nios II embedded processor literature, MegaCore user guides and net seminars.
Partners	Complete listing of AMPP IP providers, AMPP software partners, Altera Consultants Alliance Program (ACAP®) design service providers, embedded software, and EDA partners.
System Integration and Tools Support	
Quartus II Design Software	Advanced software for CPLDs, FPGAs, and structured ASICs.
SOPC Builder	Tool that simplifies system design by automating the definition and integration phase.
DSP Builder	Interface between Quartus II software and The MathWorks MATLAB and Simulink products.
Atlantic Interface	IP core interconnect for packet-based applications.
Nios II IDE	Primary software development tool for the Nios II family of embedded processors.
Development Kits	Wide range of kits containing everything an engineer needs to create and implement a design in just a matter of hours.

IP Megafunctions

Product Name	Vendor Name	IP Certifications				Altera Device Families							
		I-Tested[1]	DSP Builder Ready[2]	SOPC Builder Ready[3]	Atlantic Compliant[4]	MAX II	Cyclone II	Cyclone	Stratix II	Stratix II GX	Stratix	Stratix GX	HardCopy II
Communications													
10-Gigabit Fibre Channel FC-1 Core	MorethanIP		✓		✓						✓	✓	
8B10B Encoder/Decoder	Altera Corporation						✓	✓	✓	✓	✓	✓	✓
AAL5	Modelware							✓	✓	✓	✓	✓	
ATM Cell Delineator	Innocor		✓				✓				✓	✓	
ATM Deformatter	Adaptive Micro-Ware, Inc.							✓	✓	✓	✓	✓	
ATM Formatter	Adaptive Micro-Ware, Inc.		✓								✓	✓	
Bit Error Rate Tester	Innocor		✓								✓	✓	
Data Encoder/Decoder	Innocor		✓								✓	✓	
Ethernet Layer 2 Switch	MorethanIP						✓		✓	✓			
FlexBUS-3 Link Layer With FIFOs Version 1.0	Modelware		✓								✓	✓	
General Framing Procedure Controller	Innocor		✓				✓				✓	✓	
HDLC Single Channel With FIFO Buffers	Mentor Graphics		✓								✓	✓	
HDLC, Bit-Oriented	Innocor		✓								✓	✓	
Multi-Channel HDLC	Modelware			✓							✓	✓	
Packet Over SONET Controller	Innocor	✓	✓				✓		✓	✓	✓	✓	
POS-PHY Level 2 Link	Altera Corporation				✓		✓	✓	✓	✓	✓	✓	✓
POS-PHY Level 2 PHY	Altera Corporation				✓		✓	✓	✓	✓	✓	✓	✓
POS-PHY Level 3 Link	Altera Corporation				✓		✓	✓	✓	✓	✓	✓	✓
POS-PHY Level 3 PHY	Altera Corporation				✓		✓	✓	✓	✓	✓	✓	✓
POS-PHY Level 4	Altera Corporation	✓			✓		✓	✓	✓	✓	✓	✓	✓
SDLC Controller	CAST, Inc.		✓					✓	✓	✓	✓	✓	
Single-Channel HDLC	Modelware		✓								✓	✓	
SONET/SDH Compiler	Altera Corporation	✓					✓	✓	✓	✓	✓	✓	✓
SONET/SDH Deframer	Aliathon							✓	✓	✓	✓	✓	
SONET/SDH Demapper	Aliathon							✓	✓	✓	✓	✓	
SONET/SDH Framer	Aliathon							✓	✓	✓	✓	✓	
SONET/SDH Mapper	Aliathon							✓	✓	✓	✓	✓	
SPI-4 Phase 1 With FIFOs Version 1.0 (FlexBUS-4)	Modelware		✓								✓	✓	
SPI-4.2 Foundation & Manager	Modelware								✓	✓	✓	✓	
T1 Deframer	Adaptive Micro-Ware, Inc.							✓	✓	✓	✓	✓	
T1 Framer	Adaptive Micro-Ware, Inc.			✓							✓	✓	
UTOPIA Level 2 Master	Altera Corporation	✓			✓		✓	✓	✓	✓	✓	✓	✓
UTOPIA Level 2 Slave	Altera Corporation	✓			✓		✓	✓	✓	✓	✓	✓	✓

[1] I-Tested: Altera awards the interoperability-tested, or I-Tested, certification to MegaCore or AMPP IP that has been verified in an Altera FPGA on an evaluation board with the ASSPs or test equipment necessary to ensure interoperability according to the necessary protocols.

[2] DSP Builder Ready: Altera awards the DSP Builder Ready certification to IP cores that have plug-and-play integration with Altera's DSP Builder software.

[3] SOPC Builder Ready: Altera awards the SOPC Builder Ready certification to IP cores that have plug-and-play integration with SOPC Builder, part of Quartus II software.

[4] Atlantic Compliant: Altera awards the Atlantic Compliant certification to IP cores that have an interface that is compliant with the Atlantic interface specification, a high-performance point-to-point interface with asynchronous cell- or packet-based transfers.

IP Megafunctions (Continued)

Product Name	Vendor Name	IP Certifications				Altera Device Families							
		I-Tested[1]	DSP Builder Ready[2]	SOPC Builder Ready[3]	Atlantic Compliant[4]	MAX II	Cyclone II	Cyclone	Stratix II	Stratix II GX	Stratix	Stratix GX	HardCopy II
Digital Signal Processing													
2D DCT IDCT	Barco Silex		✓								✓	✓	
2D Forward & Inverse Discrete Wavelet Transform (2D-DWT)	CAST, Inc.		✓								✓	✓	
Accelerated Display Graphics Engine	Bitsim						✓						
AES Cryptoprocessor	CAST, Inc.		✓								✓	✓	
C32025 Digital Signal Processor	CAST, Inc.		✓								✓	✓	
CCIR-656 Decoder	Adaptive Micro-Ware, Inc.		✓								✓	✓	
CCIR-656 Encoder	Adaptive Micro-Ware, Inc.		✓								✓	✓	
Color Space Converter	Altera Corporation		✓				✓	✓	✓	✓	✓	✓	✓
Color Space Converter	CAST, Inc.		✓								✓	✓	
DES Cryptoprocessor	CAST, Inc.		✓								✓	✓	
Digital IF Receiver	Nova Engineering, Inc.							✓			✓	✓	
Fast Black & White JPEG Decoder	Barco Silex		✓				✓				✓	✓	
Fast Color JPEG Decoder	Barco Silex		✓				✓				✓	✓	
FFT/IFFT	Altera Corporation		✓		✓		✓	✓	✓	✓	✓	✓	✓
FIR Compiler	Altera Corporation		✓		✓		✓	✓	✓	✓	✓	✓	✓
Floating-Point Arithmetic Unit	Digital Core Design		✓	✓							✓	✓	
Floating-Point Mathematics Unit	Digital Core Design			✓							✓	✓	
Floating-Point Pipelined Divider Unit	Digital Core Design		✓								✓	✓	
Floating-Point-to-Integer Pipelined Converter	Digital Core Design		✓								✓	✓	
Forward Discrete Cosine Transform	CAST, Inc.		✓								✓	✓	
Forward Discrete Wavelet Transform	Barco Silex										✓	✓	
Inverse Discrete Wavelet Transform	Barco Silex										✓	✓	
JPEG Fast Decoder	CAST, Inc.		✓								✓	✓	
JPEG Fast Encoder	CAST, Inc.		✓								✓	✓	
JPEG2000 Decoder	Barco Silex								✓	✓	✓	✓	
JPEG2000 Encoder	Barco Silex								✓	✓	✓	✓	
Low Complexity Turbo Product Code Decoder	TurboConcept		✓								✓	✓	
Numerically Controlled Oscillator Compiler	Altera Corporation		✓				✓	✓	✓	✓	✓	✓	✓
Reed-Solomon Compiler, Decoder	Altera Corporation		✓				✓	✓	✓	✓	✓	✓	✓
Reed-Solomon Compiler, Encoder	Altera Corporation		✓				✓	✓	✓	✓	✓	✓	✓
SHA-1	CAST, Inc.		✓								✓	✓	
Turbo Convolutional Decoder	TurboConcept		✓								✓	✓	
Turbo Product Code Decoder	TurboConcept		✓								✓	✓	
Vector LDPC	Flarion Technologies								✓				

[1] I-Tested: Altera awards the interoperability-tested, or I-Tested, certification to MegaCore or AMPP IP that has been verified in an Altera FPGA on an evaluation board with the ASSPs or test equipment necessary to ensure interoperability according to the necessary protocols.

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IP Megafunctions (Continued)

Product Name	Vendor Name	IP Certifications				Altera Device Families							
		I-Tested[1]	DSP Builder Ready[2]	SOPC Builder Ready[3]	Atlantic Compliant[4]	MAX II	Cyclone II	Cyclone	Stratix II	Stratix II GX	Stratix	Stratix GX	HardCopy II
Digital Signal Processing (Continued)													
Very High-Speed Turbo Product Coder Decoder	TurboConcept		✓						✓	✓	✓	✓	
Viterbi Compiler, High-Speed Parallel Decoder	Altera Corporation		✓		✓		✓	✓	✓	✓	✓	✓	✓
Viterbi Compiler, Low-Speed/Hybrid Serial Decoder	Altera Corporation		✓		✓		✓	✓	✓	✓	✓	✓	✓
Embedded Processors													
16-Bit Microprocessor, 29116A	CAST, Inc.		✓						✓	✓	✓	✓	
2901 Four-Bit Microprocessor Slice	CAST, Inc.		✓					✓	✓	✓	✓	✓	
29116A 16-Bit Microprocessor	CAST, Inc.		✓						✓	✓	✓	✓	
8-Bit Microcontroller, 8051	CAST, Inc.		✓					✓	✓	✓	✓	✓	
C68000 Microprocessor	CAST, Inc.		✓					✓	✓	✓	✓	✓	
CZ80CPU Processor	CAST, Inc.		✓					✓	✓	✓	✓	✓	
D80530 Microcontroller	CAST, Inc.		✓					✓	✓	✓	✓	✓	
DF6811CPU 8-Bit Microcontroller CPU	Digital Core Design			✓					✓	✓	✓	✓	
DFPIC1655X RISC Microcontroller	Digital Core Design		✓						✓	✓	✓	✓	
DR8051 8-Bit RISC Microcontroller	Digital Core Design		✓						✓	✓	✓	✓	
DR8052EX 8-Bit RISC Extended Microcontroller	Digital Core Design		✓						✓	✓	✓	✓	
Nios II Embedded Processor	Altera Corporation			✓			✓	✓	✓	✓	✓	✓	✓
R8051 Microcontroller	CAST, Inc.		✓					✓	✓	✓	✓	✓	
R80515 Microcontroller	CAST, Inc.		✓					✓	✓	✓	✓	✓	
Real86 16-Bit Microprocessor	Eureka Technology Inc.		✓						✓	✓	✓	✓	
Interfaces and Peripherals													
10/100 Ethernet MAC	MorethanIP			✓				✓			✓	✓	
10/100/1000 Ethernet MAC With SGMII	MorethanIP			✓			✓	✓	✓	✓	✓	✓	
10/100/1000 Ethernet MAC-Net	MorethanIP			✓				✓		✓	✓	✓	
10/100/1000-Mbps Full Duplex Ethernet MAC	MorethanIP			✓	✓		✓			✓	✓	✓	
10-Gigabit Ethernet MAC	MorethanIP			✓	✓				✓	✓	✓	✓	
10-Gigabit Ethernet Physical Coding Sublayer	MorethanIP		✓		✓				✓	✓	✓	✓	
1394A FireW ire	CAST, Inc.							✓	✓	✓	✓	✓	
32/64-Bit PCI Bus Master/Target Interface, 33/66 MHz	PLDApplications	✓	✓				✓		✓	✓	✓	✓	
32/64-Bit PCI Bus Target Interface, 33/66 MHz	PLDApplications	✓	✓				✓				✓	✓	
32-Bit PCI Bus Master/Target Interface	Eureka Technology Inc.			✓			✓		✓	✓	✓	✓	
32-Bit PCI Bus Target Interface	Eureka Technology Inc.		✓				✓	✓			✓	✓	
32-Bit PCI Host Bridge	Eureka Technology Inc.		✓								✓	✓	
49410 Microprogram Controller	CAST, Inc.		✓					✓	✓	✓	✓	✓	

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[2] DSP Builder Ready: Altera awards the DSP Builder Ready certification to IP cores that have plug-and-play integration with Altera's DSP Builder software.

[3] SOPC Builder Ready: Altera awards the SOPC Builder Ready certification to IP cores that have plug-and-play integration with SOPC Builder, part of Quartus II software.

[4] Atlantic Compliant: Altera awards the Atlantic Compliant certification to IP cores that have an interface that is compliant with the Atlantic interface specification, a high-performance point-to-point interface with asynchronous cell- or packet-based transfers.

IP Megafunctions (Continued)

Product Name	Vendor Name	IP Certifications				Altera Device Families							
		I-Tested[1]	DSP Builder Ready[2]	SOPC Builder Ready[3]	Atlantic Compliant[4]	MAX II	Cyclone II	Cyclone	Stratix II	Stratix II GX	Stratix	Stratix GX	HardCopy II
Interfaces and Peripherals (Continued)													
64-Bit PCI Bus Master/Target Interface	Eureka Technology Inc.		✓				✓				✓	✓	
64-Bit PCI Bus Target Interface	Eureka Technology Inc.		✓								✓	✓	
64-Bit PCI Host Bridge	Eureka Technology Inc.		✓				✓				✓	✓	
AHB Master	Eureka Technology Inc.			✓							✓	✓	
AHB Slave	Eureka Technology Inc.			✓							✓	✓	
AHB to PCI Host Bridge	Eureka Technology Inc.			✓							✓	✓	
AHB to SDRAM Controller	Eureka Technology Inc.		✓								✓	✓	
AMBA-AHB PCI Bridge	PLDApplications	✓	✓	✓							✓	✓	
ATA-4	Nuvation							✓			✓	✓	
ATA-5	Nuvation							✓			✓	✓	
C6845 Cathode Ray Tube (CRT) Controller	CAST, Inc.			✓							✓	✓	
C8237 Programmable DMA Controller	CAST, Inc.		✓				✓	✓	✓	✓	✓	✓	
C8279 Programmable Keyboard/Display Interface	CAST, Inc.			✓				✓	✓	✓	✓	✓	
CAN	CAST, Inc.						✓	✓	✓	✓	✓	✓	
CUSB USB Function Controller	CAST, Inc.	✓	✓				✓				✓	✓	
CUSB2	CAST, Inc.						✓	✓	✓	✓	✓	✓	
CZ80CTC Programmable Counter-Timer	CAST, Inc.		✓					✓	✓	✓	✓	✓	
CZ80PIO Programmable Parallel Input/Output Controller	CAST, Inc.		✓								✓	✓	
CZ80SIO	CAST, Inc.							✓	✓	✓	✓	✓	
D16550 UART With 16-Byte FIFO	Digital Core Design		✓	✓							✓	✓	
DDR SDRAM Controller	Altera Corporation	✓		✓			✓	✓	✓	✓	✓	✓	✓
DDR2 SDRAM Controller	Altera Corporation	✓		✓			✓	✓	✓	✓	✓	✓	✓
DI2CM I2C Bus Interface-Master	Digital Core Design			✓							✓	✓	
DI2CSB I2C Bus Interface-Slave	Digital Core Design			✓							✓	✓	
DMA Controller	Eureka Technology Inc.			✓							✓	✓	
DMA Controller for AHB	Eureka Technology Inc.			✓							✓	✓	
DSPI Serial Peripheral Interface Master/Slave	Digital Core Design			✓							✓	✓	
Dual UART for AHB	Eureka Technology Inc.			✓							✓	✓	
GEOS2+2	Nuvation						✓	✓	✓	✓	✓	✓	
GPIO8-APB	CAST, Inc.							✓	✓	✓	✓	✓	
H16450 UART	CAST, Inc.		✓								✓	✓	
H16450S UART	CAST, Inc.		✓						✓	✓	✓	✓	

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IP Megafunctions (Continued)

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Interfaces and Peripherals (Continued)													
H16550 UART	CAST, Inc.		✓								✓	✓	
H16550S UART	CAST, Inc.			✓							✓	✓	
H16750 UART	CAST, Inc.							✓	✓	✓	✓	✓	
H16750S UART	CAST, Inc.		✓								✓	✓	
H8250	CAST, Inc.			✓							✓	✓	
HyperTransport	Altera Corporation	✓			✓				✓	✓	✓	✓	
I2C Bus Controller	CAST, Inc.			✓							✓	✓	
I2C Bus Controller Slave	CAST, Inc.		✓						✓	✓	✓	✓	
Integrated PCI Core	Northwest Logic, Inc.		✓					✓			✓	✓	
ISA/PC Card/PCMCIA/Compact Flash Host Adapter	Eureka Technology Inc.			✓							✓	✓	
MAC	CAST, Inc.		✓				✓				✓	✓	
MD5	CAST, Inc.							✓	✓	✓	✓	✓	
Microprogram Controller, 2910/2910A	CAST, Inc.		✓					✓	✓	✓	✓	✓	
MODEXP1	CAST, Inc.							✓			✓	✓	
Multi-Function Memory Controller	Eureka Technology Inc.		✓								✓	✓	
Multi-Gigabit Fibre Channel Transport Core	MorethanIP				✓				✓	✓	✓	✓	
NAND Flash Memory Controller—nflashctrl	CAST, Inc.							✓	✓	✓	✓	✓	
Nios CAN	IFI		✓	✓							✓	✓	
Parallel & Serial RapidIO	Altera Corporation	✓			✓				✓	✓	✓	✓	✓
PCI Bus Arbiter	Eureka Technology Inc.		✓								✓	✓	
PCI Compiler, 32-Bit Master/Target	Altera Corporation	✓		✓		✓	✓	✓	✓	✓	✓	✓	✓
PCI Compiler, 32-Bit Target	Altera Corporation	✓		✓		✓	✓	✓	✓	✓	✓	✓	✓
PCI Compiler, 64-Bit Master/Target	Altera Corporation	✓		✓			✓	✓	✓	✓	✓	✓	✓
PCI Compiler, 64-Bit Target	Altera Corporation	✓		✓			✓	✓	✓	✓	✓	✓	✓
PCI Express	PLDApplications								✓	✓	✓	✓	
PCI Express x1 Lane	Altera Corporation	✓							✓	✓		✓	✓
PCI Express x4 Lanes	Altera Corporation	✓							✓	✓			✓
PCI Express x8 Lanes	Altera Corporation									✓			
PCI Interface	Northwest Logic, Inc.		✓					✓			✓	✓	
PCI-ISA Bridge	Eureka Technology Inc.		✓								✓	✓	
PCI-PCI Bridge	Eureka Technology Inc.		✓								✓	✓	
PCI-X Master/Target Core 32/64-Bit	PLDApplications		✓				✓		✓	✓			

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IP Megafunctions (Continued)

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Interfaces and Peripherals (Continued)													
Pipeline SDRAM Controller	Eureka Technology Inc.		✓								✓	✓	
PowerPC Bus Arbiter	Eureka Technology Inc.		✓								✓	✓	
PowerPC Bus Master	Eureka Technology Inc.		✓								✓	✓	
PowerPC Bus Slave	Eureka Technology Inc.			✓							✓	✓	
PowerPC to PCI Host Bridge	Eureka Technology Inc.		✓								✓	✓	
PowerPC/SH/1960 System Controller	Eureka Technology Inc.		✓								✓	✓	
Programmable Interrupt Controller, 8259	Innocor		✓								✓	✓	
Programmable Interrupt Controller, 8259A	CAST, Inc.		✓					✓	✓	✓	✓	✓	
Programmable Interval Timer/Counter, 8254	CAST, Inc.		✓								✓	✓	
Programmable Peripheral Interface, 8255A	CAST, Inc.		✓					✓	✓	✓	✓	✓	
QDRII SRAM Controller	Altera Corporation	✓							✓	✓	✓	✓	
RLDRAM II Controller	Altera Corporation								✓	✓			
SDR SDRAM Controller	Northwest Logic, Inc.		✓										
SDRAM Controller	Eureka Technology Inc.		✓								✓	✓	
SerialLite	Altera Corporation	✓			✓							✓	
SerialLite II	Altera Corporation				✓					✓		✓	
Smart Card Reader	CAST, Inc.							✓	✓	✓	✓	✓	
UART	Eureka Technology Inc.		✓								✓	✓	
USB Function Controller	SLS			✓				✓					

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FOR MORE INFORMATION Intellectual Property www.altera.com/ipmegastore

Quartus II Design Software

Quartus II software leads the industry in ease-of-use, performance, and productivity with the most comprehensive environment available for FPGAs, CPLDs, and structured ASICs. It is the industry's only environment to support IP-based system design, and offers complete, automated system definition and implementation without requiring lower-level HDL or schematics. This—and seamless integration with leading EDA software tools and flows—will help turn your concepts into working systems in minutes.

Quartus II Subscription & Web Edition Software

	Subscription Edition	Web Edition
Devices:	All	MAX & Cyclone Series
Features:	100%	98%
Distribution:	Altera Subscription Program	Internet & Free CD

Quartus II Design Software Features Summary

Design Flow Methodology	
Incremental Design	Improves design timing closure and reduces design compilation times up to 70 percent. Supports team-based design.
Up-Front I/O Assignment and Validation	Enables PCB layout to begin earlier.
Pin Planner	Eases the process of assigning and managing pin assignments for high-density and high-pin-count designs.
SOPC Builder	Automates adding, parameterizing, and linking IP cores—including embedded processors, coprocessors, peripherals, memories, and user-defined logic.
Off-the-Shelf IP Cores	Lets you construct your system-level design using IP cores from Altera's MegaFunction library and from Altera's third-party AMPP partners.
Parallel Development of FPGA Prototypes and Structured ASICs	Allows for FPGA prototypes and HardCopy structured ASICs to be designed in parallel using the same design software and IP.
Scripting Support	Supports command-line operation and Tcl scripting in addition to GUI design processing.
Performance and Timing Closure Methodology	
Physical Synthesis Optimization	Uses post place-and-route delay knowledge of a design to improve performance.
Design Space Explorer	Increases performance by automatically iterating through combinations of Quartus II software settings to find optimal results.
Extensive Cross-Probing	Features unmatched support for cross-probing between verification tools and design source files.
Timing Optimization Advisor	Provides design-specific advice to improve design timing performance.
Timing Closure Floorplan Editor	Enables analysis of timing data in the floorplan.
Chip Editor	Reduces verification time (while maintaining timing closure) by enabling small, post place-and-route design changes to be implemented in minutes.
Register Transfer Level (RTL) Viewer and Technology Map Viewer	Provides schematic representation that can be used to analyze a design's structure before and after its implementation.
Verification	
Advanced Multi-Clock Timing Analysis Capabilities	Provides advanced tools to analyze and optimize timing performance in designs with multiple clocks.
SignalTap® II Embedded Logic Analyzer	Supports the most channels, fastest clock speeds, largest sample depths, and most advanced triggering capabilities available in an embedded logic analyzer.
PowerPlay Technology	Provides power analysis and optimization support for power supply and thermal management planning.
SignalProbe™ Routing	Incrementally routes an internal node to an unused or reserved pin for analysis with an external scope or logic analyzer.
Third-Party Support	
EDA Partners	Offers EDA software support for synthesis, functional and timing simulation, static timing analysis, board-level simulation, signal integrity analysis, and formal verification.

Free Quartus II Web Edition Software

Altera offers free Quartus II Web Edition software for Windows-based PCs. It includes everything you need to design for Altera's latest CPLD and low-cost FPGA families. Quartus II Web Edition software also includes support for entry-level members of Altera's high-density FPGA families.

Quartus II Web Edition features include:

- Schematic- and text-based design entry
- Integrated VHDL and Verilog HDL synthesis and support for third-party synthesis software
- SOPC Builder system generation software
- Placement, routing, verification, and programming functions

Altera Design Software Subscription Program

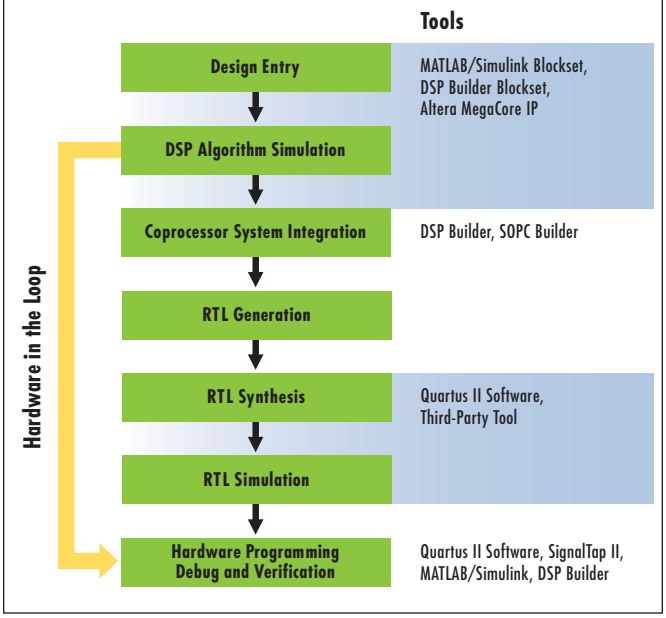
Altera's subscription program offers a comprehensive suite of premium software and IP products. Included in the subscription are:

- Quartus II Subscription Edition
  - Support for all Altera devices and software features
  - Support for Linux, Solaris, and HP-UX operating systems in addition to Windows-based PC versions
- Nios II Design Suite
- ModelSim®-Altera simulation software
- Complete IP Base Suite CD, which includes full licenses to Altera's FIR Compiler, NCO Compiler, and FFT Compiler DSP MegaCore functions, as well as the DDR, DDR2, QDRII, and RLDRAM II memory controller MegaCore functions

DSP Builder

Altera's DSP Builder enables you to perform algorithm development, simulation, and verification easily using The MathWorks MATLAB and Simulink system-level design tools, and seamlessly implement the DSP design in an FPGA using Quartus II software. Existing MATLAB functions and Simulink blocks can be combined with Altera DSP Builder blocks and Altera IP MegaCore functions to link system-level design and implementation with DSP algorithm development.

DSP Design Flow Overview



DSP Builder Features Summary	
The MathWorks MATLAB and Simulink Support	Links The Mathworks MATLAB (Signal Processing ToolBox and Filter Design Toolbox) and Simulink software with Altera Quartus II software.
SignalTap II Logic Analyzer Support	Probes signals from the Altera device on the DSP board and imports the data into the MATLAB work space to facilitate visual analysis.
SOPC Builder and Nios II Support	Includes blocks that you can use to build custom logic that works with Nios II embedded processors and other Quartus II SOPC Builder designs.
Testbench Generation	Automatically generates a VHDL testbench or Quartus II Vector File (.vec) from MATLAB and Simulink test vectors.
Simulation Support	Enables bit- and cycle-accurate design simulation.
Hardware in the Loop	Accelerates system-level co-simulation with Simulink and provides advanced debugging features.

SOPC Builder

SOPC Builder is an exclusive Quartus II software tool that enables you to build and evaluate systems at the block level easily and rapidly. SOPC Builder allows you to focus on your custom, differentiating functions by eliminating manual system integration tasks. In addition to your custom logic, you can select common functions from the Altera or Altera partner IP core libraries to include in your system. SOPC Builder automatically generates interconnect logic to make the system work optimally and creates a testbench to verify functionality to save valuable design time.

Peripheral Expansion of Stand-Alone Processors

SOPC Builder includes a component editor feature to let you easily interface to nearly any external processor or DSP device. If you create an SOPC Builder component interface to your processor, you can add additional I/O pins, prepackaged peripherals, or custom, self-made peripherals in just a few mouse clicks. SOPC Builder will build the system and output header files for your software development team. The team can access the peripherals from the external processor using their preferred integrated development environment.

Connection to ASSPs or CPUs via PCI

Many ASSPs and processors include PCI interfaces. You can easily build systems that communicate through PCI to these ASSPs or external processors if you use Altera's SOPC Builder and the SOPC Builder Ready PCI Compiler function.

SOPC Builder Features Summary	
IP Selection and Parameter Selection	Select and parameterize off-the-shelf IP from Altera and its partners or create your own custom components. Off-the-shelf IP includes the Nios II processor, memory interfaces, common embedded system peripherals, bridges and interfaces, DSP IP, and hardware accelerator peripherals.
Avalon™ Interconnect Fabric Generation	Uses an optimal interconnect fabric created specifically for the requirements of each system. Integration tasks automatically performed by SOPC Builder include: ▪ Data-path multiplexing between design blocks ▪ Address decoding ▪ Wait-state generation ▪ Dynamic bus sizing ▪ Interrupt priority assignment ▪ Clock domain crossing to connect peripherals or systems operating on different clock domains
Component Editor	Allows you to create your own custom SOPC Builder components.
IP Reuse	Reuse any custom-created IP core designed for SOPC Builder in future products.
Testbench Generation	Outputs testbench suites to test generated systems.
Header File Generation	Outputs a custom header file based on the memory map and components of the generated system.

FOR MORE INFORMATION

Quartus II Software	www.altera.com/quartus2
Quartus II Web Edition Download	www.altera.com/download
SOPC Builder	www.altera.com/sopcbuilder
DSP Builder	www.altera.com/dspbuilder
Training	www.altera.com/training

Development Kits

Altera and its partners provide you with a variety of hardware platforms to support the creation and verification of your FPGA and CPLD designs. These development kits speed system design by providing test and debug platforms for RTL generation, as well as allowing you to begin the development of application software. If you are a new user, you'll find the Altera development kits easy to master. They contain detailed walk-throughs and example designs supporting Quartus II software, IP design flow, and programming options for Altera devices. In addition, these kits provide a platform for designers to use the OpenCore Plus feature of Altera IP MegaCore functions.

The following sections briefly describe the types of Altera development kits:

- DSP Development Kits
- High-Speed Interface Development Kits
- PCI & PCI-X Development Kits
- Nios II Development Kits
- MAX CPLD Development Kits

DSP Development Kits

Altera DSP development kits are effective platforms for prototyping and debugging DSP designs for programmable logic. Jump-start your designs for complex digital communications by implementing entire modulator/demodulator subsystems in hardware within hours, using the OpenCore Plus feature of Altera's DSP MegaCore functions. DSP development kits give you everything you need right out of the box. They include an Altera device, DSP development board, Quartus II software (one-year, time-limited license), DSP Builder (Quartus II MATLAB/Simulink interface), a 30-day evaluation copy of MATLAB/Simulink, and system reference designs.

High-Speed Interface Development Kits

Altera and its partners offer cost-effective development kits to evaluate high-speed interfaces. As an example, the High-Speed Development Kit, Stratix GX Edition, provides gigabit Ethernet, 10 gigabit Ethernet, XAUI, Fibre Channel (1, 2, and 10 Gbps), SONET/SDH (OC-12 and OC-48), SPI-4.2, SDI, and Serial RapidIO interfaces. The Stratix II edition supports MSA-300 compliant OC-192 optics, SPI-4.2, 8-bit parallel RapidIO, HyperTransport, PCI-X, and DDR2 SDRAM standards.

PCI & PCI-X Development Kits

Altera's PCI development kits provide a flexible hardware platform to quickly begin hardware testing and validation of your PCI-based design. With a variety of memory, interfaces, and peripherals available on the standard PCI card form factor, the PCI development kits offer a complete design environment with support for 32- or 64-bit, 33- or 66-MHz PCI, as well as PCI-X operations. Each board comes with a user application and a library of reference designs to exercise PCI transactions right out of the box. OpenCore Plus hardware evaluation enables designers to use these kits as the perfect prototyping platform for a variety of interface IP. Use the development kits for evaluation of the PCI core and for rapid prototyping and debugging in a real-time environment.

Nios II Development Kits

Nios II development kits include everything you need for embedded processor system development. The kits include Nios II embedded processors and a perpetual license to create embedded systems, the Nios II IDE software development tool chain, and access to over 60 peripheral IP cores. In addition, the kits contain Quartus II design software (one-year, time-limited license), a feature-rich FPGA-based development board (including power supply, USB Blaster™ download cable, and LCD display), extensive reference designs, tutorials, and complete documentation. Nios II development kits are available for several Altera FPGA families: Stratix II, Stratix, Cyclone II, and Cyclone.

Nios II Development Kit, Stratix Edition

MAX CPLD Series Development Kits

Altera and its partners provide low-cost, easy-to-use development kits to ensure an easy and productive evaluation of MAX II and MAX CPLDs. The MAX II Development Kit comes with a complete design environment that includes all software, cables, and accessories needed to evaluate the MAX II feature set or begin prototyping a design prior to receiving custom hardware.

Development Kits

Devices	Product Name	Partner	Price (US$)
MAX II EPM1270	MAX II Development Kit	Altera Corporation	$150
MAX II EPM1270	MAX II Starter Kit	Galaxy	Contact Partner
MAX EPM3032A to EPM7160S	DIGILAB picoMAX	El Camino GmbH	Contact Partner
Cyclone II EP2C35	DSP Development Kit, Cyclone II Edition	Altera Corporation	$995
Cyclone II EP2C35	DSP Development Kit, Cyclone II Edition	Altera Corporation	$995
Cyclone II EP2C35	Nios II Development Kit, Cyclone II Edition	Altera Corporation	$995
Cyclone II EP2C35	PCI Development Kit, Cyclone II Edition	Altera Corporation	$995
Cyclone II EP2C35	PROCSpark II Development Board	GiDEL Limited	$549
Cyclone EP1C10 to EP1C12	DIGILAB CC Development Kit	El Camino GmbH	$599
Cyclone EP1C12	Nios II Evaluation Kit	Altera Corporation	$295
Cyclone EP1C12	LiveDesign Evaluation Kit	Altium	$99
Cyclone EP1C20	Nios II Development Kit, Cyclone Edition	Altera Corporation	$995
Cyclone EP1C20	Microtronix Cyclone Development Kit	Microtronix Inc.	$595
Cyclone EP1C20	MJL Cyclone Development Kit	MJL, Inc.	$695
Cyclone EP1C20	Parallax Cyclone Smartpack	Parallax Inc.	$295
Cyclone EP1C3	ezFPGA Cyclone EP1C3 Prototyping & Evaluation Kit	Dallas Logic	Contact Partner
Cyclone EP1C6	SOCkit Cyclone EP1C6 Nios/LVDS Evaluation Kit	Dallas Logic	Contact Partner
Cyclone EP1C6	Trex 1 Development Board	Terasic Technologies Inc.	$149
Cyclone EP1C6	Twister DDR SDRAM Evaluation Kit	www.fpga.nl	$349
Stratix II EP2S180	DSP Development Kit, Stratix II Professional Edition	Altera Corporation	$5,995
Stratix II EP2S60	DSP Development Kit, Stratix II Edition	Altera Corporation	$1,995
Stratix II EP2S60	High-Speed Development Kit, Stratix II Edition	Altera Corporation	$1,995
Stratix II EP2S30	Nios II Development Kit, Stratix II Edition	Altera Corporation	$995
Stratix II EP2S60 to EP2S180	PROCStar II Development Platform	GiDEL Limited	Contact Partner
Stratix II EP2S60 to EP2S180	PROC2S Stratix II FPGA Board	GiDEL Limited	$1,495
Stratix EP1S10	Nios II Development Kit, Stratix Edition	Altera Corporation	$150
Stratix EP1S10	CAS10 Stratix Development Board	CEPD Inc.	Contact Partner
Stratix EP1S10	MJL HardCopy Stratix Prototyping Kit	MJL, Inc.	$895
Stratix EP1S10	MJL Stratix Development Kit	MJL, Inc.	$795
Stratix EP1S10	Parallax Stratix Smartpack	Parallax Inc.	$395
Stratix EP1S10	Stratix High-Speed Development Kit	Rapid Technology	$1,795

Development Kits (Continued)

Devices	Product Name	Partner	Price (US$)
Stratix EP1S25	DSP Development Kit, Stratix Edition	Altera Corporation	$1,995
Stratix EP1S25	PCI Development Kit, Stratix Edition	Altera Corporation	$1,995
Stratix EP1S25	Microtronix Stratix Development Kit	Microtronix Inc.	$995
Stratix EP1S25	Parallax Stratix Smartpack	Parallax Inc.	$495
Stratix EP1S25	PMC-Stratix Development Kit	Rapid Technology	$1,995
Stratix EP1S25	TS-PCI A25 General-Purpose Development Kit	SBS Technologies	Contact Partner
Stratix EP1S25	TS-PCI A25 Imaging Tool Kit	SBS Technologies	Contact Partner
Stratix EP1S25	Tsunami PCI-Based Image Processing Solutions	SBS Technologies	$7,500
Stratix EP1S30	TS-PCI 140 General-Purpose Development Kit	SBS Technologies	Contact Partner
Stratix EP1S30 to EP1S80	DIGILAB SX High-End Prototyping System	El Camino GmbH	$2,595
Stratix EP1S30 to EP1S80	Advanced Stratix PCI-X/PCI Development Kit	PLDApplications	$2,490 to $3,990
Stratix EP1S30 to EP1S80	Q5V4 Series FPGA Development Boards	Rowe Engineering	$4,995
Stratix EP1S40	Nios II Development Kit, Stratix Professional Edition	Altera Corporation	$2,495
Stratix EP1S40	TS-PCI A40 General-Purpose Development Kit	SBS Technologies	Contact Partner
Stratix EP1S40	TS-PCI A40 Imaging Tool Kit	SBS Technologies	Contact Partner
Stratix EP1S40	TS-PMC General-Purpose Development Kit	SBS Technologies	Contact Partner
Stratix EP1S40	TS-PMC Video Development Kit	SBS Technologies	Contact Partner
Stratix EP1S40 to EP1S80	IPSP Development Kit	Soliton Systems	Contact Partner
Stratix EP1S40 to EP1S80	DN5000K10 Stratix FPGA-Based ASIC Prototyping Kit	The Dini Group	$10,950 to $27,950
Stratix EP1S60	PCI High-Speed Development Kit, Stratix Professional Edition	Altera Corporation	$4,995
Stratix EP1S80	DSP Development Kit, Stratix Professional Edition	Altera Corporation	$4,995
Stratix EP1S80	PROC1S Stratix 80 FPGA Board	GiDEL Limited	$5,845
Stratix EP1S80	PROCSuperStar Stratix 80 Board	GiDEL Limited	$7,995
Stratix EP1S80	TS-CPCI 6U Development Kit	SBS Technologies	Contact Partner
Stratix EP1S80	TS-Software-Defined Radio Development Kit	SBS Technologies	Contact Partner
Stratix EP1S80	TS-Software-Defined Radio Development Kit With Chassis	SBS Technologies	Contact Partner
Stratix EP1S80 (2 to 5 Devices)	DN5000K10S Stratix FPGA-Based ASIC Prototyping Kit	The Dini Group	$4,950 to $7,950
Stratix GX EP1SGX40	High-Speed Development Kit, Stratix GX Edition	Altera Corporation	$7,995

FOR MORE INFORMATION Development Kits www.altera.com/devkits

Training

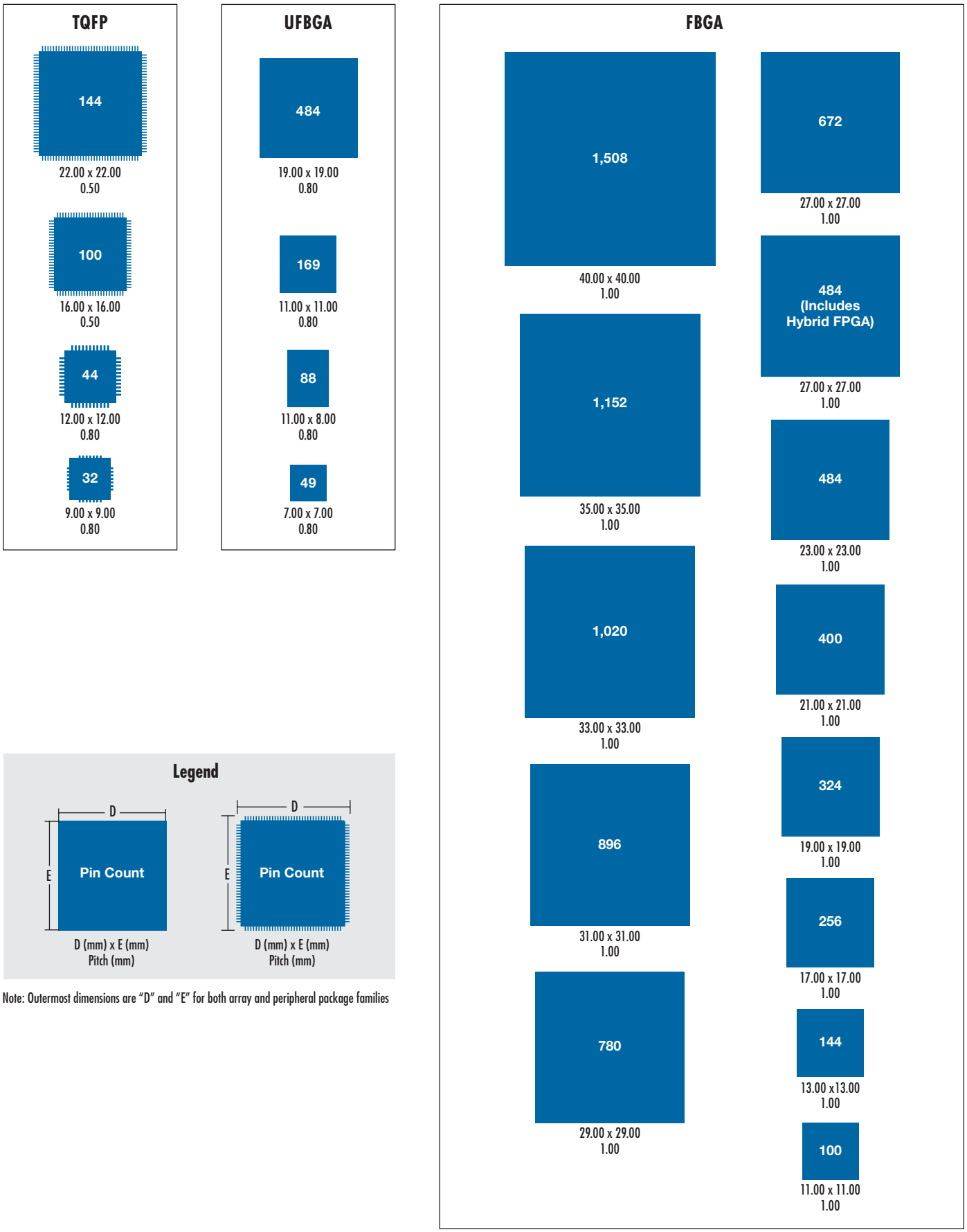
Attend an Altera technical training course to speed your time-to-market and achieve optimal design results. Our courses give you the skills you need to quickly produce high-performance, small-footprint designs. All courses are one-day and instructor-led, unless otherwise noted.

Altera Training Courses Summary

Category	General Description	Course Titles
DSP Design Courses	Solve DSP design challenges using Altera technology and the skills you will learn in these classes.	▪ DSP Design Series Part I: Implementing DSP Designs in FPGAs ▪ DSP Design Series Part II: Using FPGAs to Architect and Optimize a DSP System
Design Language Courses	Attain the skills needed to design with Verilog HDL and VHDL for programmable logic.	▪ Introduction to VHDL ▪ Advanced VHDL Design Techniques ▪ Introduction to Verilog HDL ▪ Advanced Verilog HDL Design Techniques
Embedded Systems Design Courses	Learn to design a Nios II soft-core microprocessor system in an Altera FPGA.	▪ Designing With the Nios II Processor and SOPC Builder (for Hardware Engineers) ▪ Developing Software for the Nios II Processor (Course Length: Two Days; for Software Engineers) ▪ Designing a System on a Programmable Chip
FPGA Courses	Create optimal FPGA designs by learning design techniques to take advantage of key device features and resources.	▪ Designing With Cyclone and Cyclone II Devices ▪ Fundamental Design Techniques for Stratix and Stratix II Devices ▪ Advanced Design Techniques for Stratix and Stratix II Devices
High-Speed Design Course	Learn how to implement high-speed I/O protocols using FPGA multigigabit transceivers. Optimize your design by taking advantage of the architecture, operating modes, and features discussed throughout the course. Gain an understanding of the fundamentals of signal integrity in high-speed design.	▪ High-Speed Design Using FPGAs (Course Length: Two Days)
Software Courses	Acquire design entry, compilation, and analysis skills by learning how to use both basic and advanced features of the Quartus II software and ModelSim-Altera software.	▪ Designing With the Quartus II Software ▪ Designing With the Quartus II Software for CPLDs (for MAX II Designs) ▪ Accelerating Design Cycles With the Quartus II Software ▪ Analyzing Designs Using Mentor Graphic's ModelSim and Altera's Quartus II Software
Online Classes	Online classes give you an overview of a variety of features and techniques for your designs. Use these free trainings to preview topics of more in-depth, instructor-led classes; jump-start your designs; or brush up on key how-to design tips. All courses listed are one-hour, online courses.	▪ Introduction to Tool Command Language (Tcl) Part 1 of 2 ▪ Introduction to Tcl Part 2 of 2 ▪ Command-Line Scripting ▪ Basic Quartus II Software Tcl Scripting Part 1 of 2 ▪ Basic Quartus II Software Tcl Scripting Part 2 of 2 ▪ VHDL Basics ▪ Verilog HDL Basics ▪ Using Quartus II Software: An Introduction ▪ Using Quartus II Software: Timing Analysis ▪ Using Quartus II Software: Managing Design Changes With Chip Editor ▪ Debugging Designs With the SignalTap II Logic Analyzer ▪ Power and Thermal Management ▪ System-on-a-Programmable-Chip Design Using the Nios II Embedded Processor ▪ Using SOPC Builder ▪ Using DSP Builder ▪ Using Stratix and Stratix II High-Speed Design Features ▪ Using Quartus II Software: Incremental Design

FOR MORE INFORMATION Training www.altera.com/training

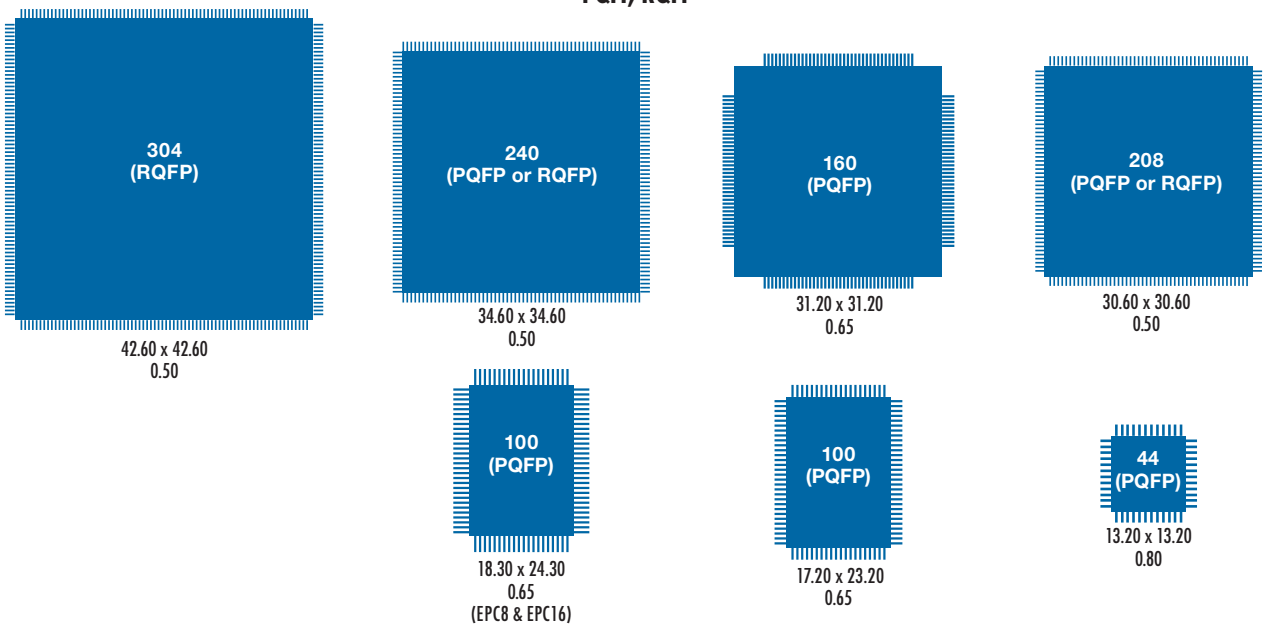
Package Matrix



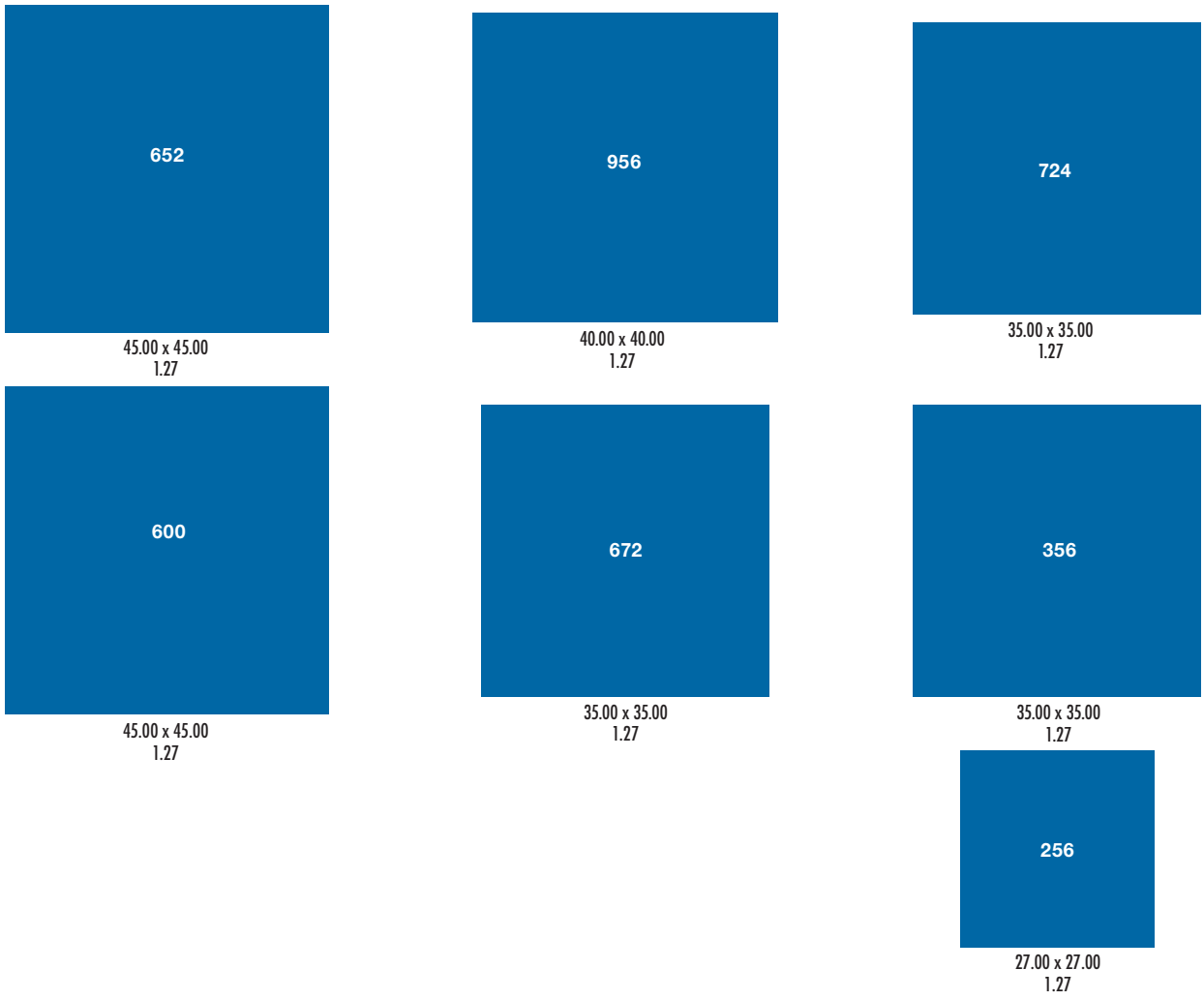
Note: Outermost dimensions are "D" and "E" for both array and peripheral package families

Package Matrix

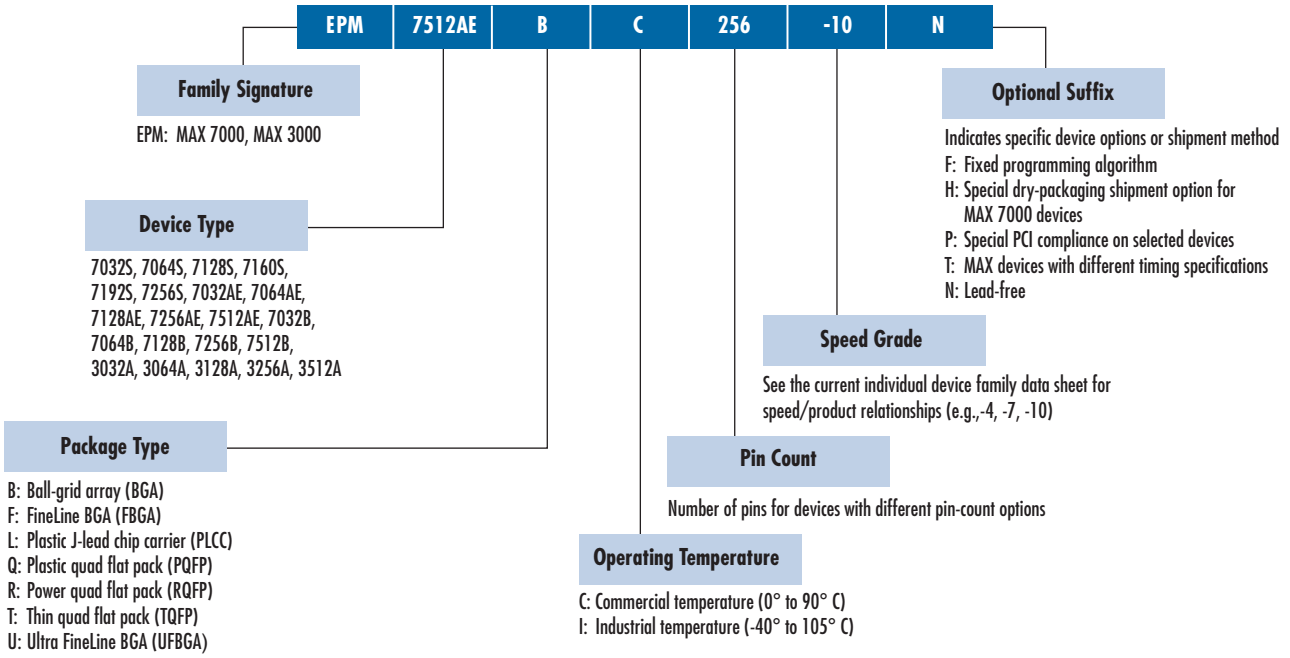
PQFP, RQFP

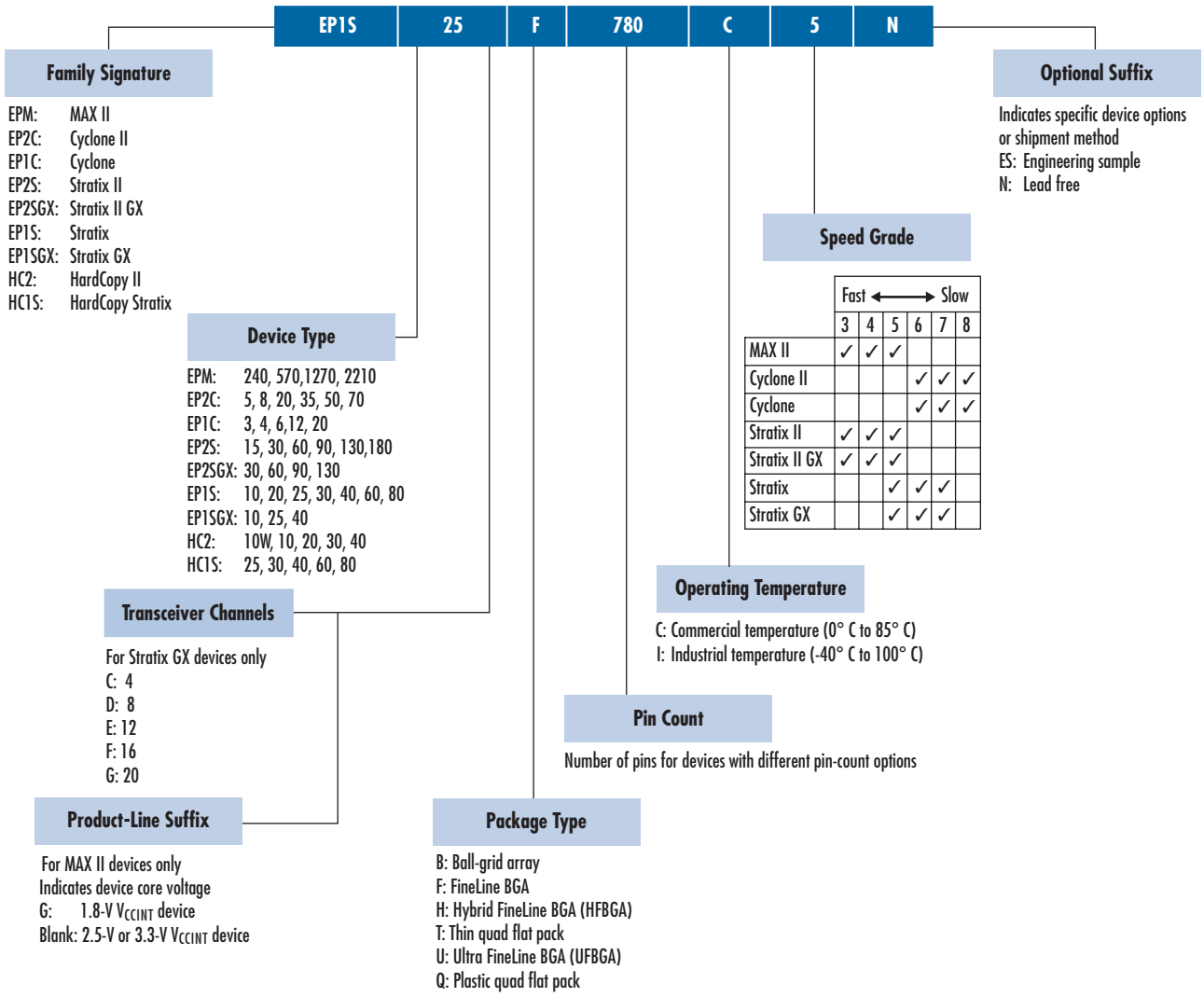


BGA



Ordering Codes





Product Websites & Information

MAX CPLD Series

MAX II CPLDs
www.altera.com/max2

MAX 3000A CPLDs
www.altera.com/products/devices/max3k

MAX 7000 CPLDs
www.altera.com/products/devices/max7k

Cyclone Low-Cost FPGA Series

Cyclone II FPGAs
www.altera.com/cyclone2

Cyclone FPGAs
www.altera.com/cyclone

Stratix High-Density FPGA Series

Stratix II FPGAs
www.altera.com/stratix2

Stratix II GX Transceiver FPGAs
www.altera.com/stratix2gx

Stratix FPGAs
www.altera.com/stratix

Stratix GX Transceiver FPGAs
www.altera.com/stratixgx

HardCopy Structured ASIC Series

HardCopy Structured ASIC Series
www.altera.com/hardcopy

HardCopy II Structured ASICs
www.altera.com/hardcopy2

HardCopy Stratix Structured ASICs
www.altera.com/hardcopystratix

Nios II Embedded Processors

Nios II Embedded Processors
www.altera.com/nios2

Nios II Development Kits
www.altera.com/nioskits

Third-Party Software Tool Support
www.altera.com/niospartners

Nios Community Forum
www.niosforum.org

Eclipse Project
www.eclipse.org

Intellectual Property Solutions

IP Megastore
www.altera.com/ipmegastore

Quartus II Design Software

Quartus II Software
www.altera.com/quartus2

Quartus II Web Edition Download
www.altera.com/download

SOPC Builder
www.altera.com/sopcbuilder

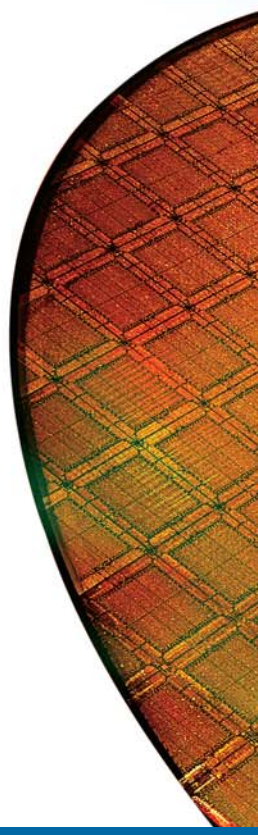
DSP Builder
www.altera.com/dspbuilder

Development Kits

Altera & Partner Development Kits
www.altera.com/devkits

Training

Altera Technical Training
www.altera.com/training



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