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December 1997

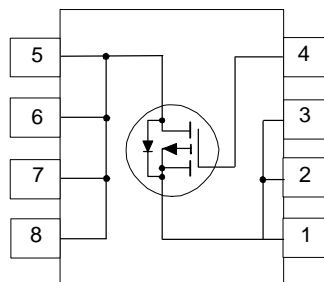
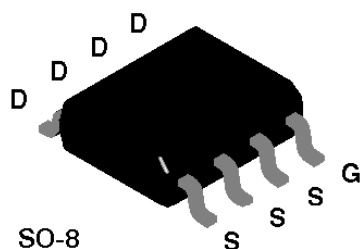
NDS9430A Single P-Channel Enhancement Mode Field Effect Transistor

General Description

These P-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- -5.3A, -20V. $R_{DS(ON)} = 0.05\Omega$ @ $V_{GS} = -10V$
 $R_{DS(ON)} = 0.065\Omega$ @ $V_{GS} = -6V$
 $R_{DS(ON)} = 0.09\Omega$ @ $V_{GS} = -4.5V$.
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.



Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	NDS9430A	Units
V_{DSS}	Drain-Source Voltage	-20	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Drain Current - Continuous (Note 1a)	± 5.3	A
	- Pulsed	± 20	
P_D	Maximum Power Dissipation (Note 1a)	2.5	W
	(Note 1b)	1.2	
	(Note 1c)	1	
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	50	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	25	$^\circ\text{C/W}$

Electrical Characteristics (T _A = 25°C unless otherwise noted)						
Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = -250 μA	-20			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -16 V, V _{GS} = 0 V			-1	μA
		V _{DS} = -10 V, V _{GS} = 0 V T _J = 70°C			-5	μA
I _{GSSF}	Gate - Body Leakage, Forward	V _{GS} = 20 V, V _{DS} = 0 V			100	nA
I _{GSSR}	Gate - Body Leakage, Reverse	V _{GS} = -20 V, V _{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = -250 μA	-1	-1.4	-3	V
		T _J = 125°C	-0.7	-1	-2	
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} = -10 V, I _D = -5.3 A		0.038	0.05	Ω
		T _J = 125°C		0.054	0.1	
		V _{GS} = -6 V, I _D = -4.7 A		0.046	0.065	
		V _{GS} = -4.5 V, I _D = -4.2 A		0.064	0.09	
I _{D(on)}	On-State Drain Current	V _{GS} = -10 V, V _{DS} = -5 V	-15			A
		V _{GS} = -4.5, V _{DS} = -5V	-3.6			
g _{FS}	Forward Transconductance	V _{DS} = 15 V, I _D = 5.3 A		10		S
DYNAMIC CHARACTERISTICS						
C _{iss}	Input Capacitance	V _{DS} = 15 V, V _{GS} = 0 V, f = 1.0 MHz		950		pF
C _{oss}	Output Capacitance			610		pF
C _{rss}	Reverse Transfer Capacitance			220		pF
SWITCHING CHARACTERISTICS (Note 2)						
t _{D(on)}	Turn - On Delay Time	V _{DD} = -10 V, I _D = -1 A, V _{GEN} = -10 V, R _{GEN} = 6 Ω		10	30	ns
t _r	Turn - On Rise Time			18	60	ns
t _{D(off)}	Turn - Off Delay Time			80	120	ns
t _f	Turn - Off Fall Time			45	100	ns
Q _g	Total Gate Charge	V _{DS} = -10 V, I _D = -5.3 A, V _{GS} = -10 V		29	50	nC
Q _{gs}	Gate-Source Charge			3		nC
Q _{gd}	Gate-Drain Charge			9		nC

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I _S	Maximum Continuous Drain-Source Diode Forward Current				-2.1	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = -2.4 A (Note 2)		-0.85	-1.2	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0V, I _F = -2.4 A, dI _F /dt = 100 A/μs			100	ns

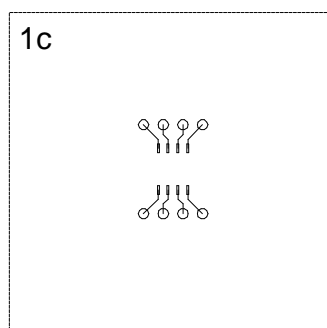
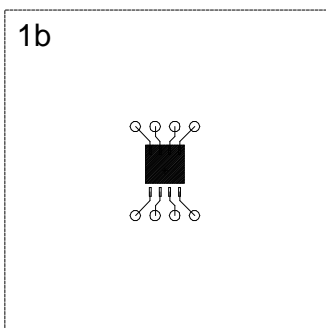
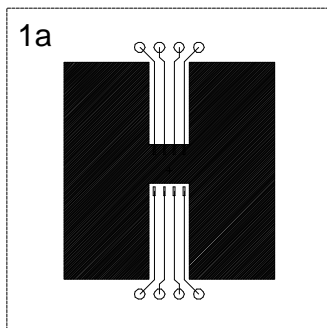
Notes:

1. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJA} is guaranteed by design while R_{θJC} is determined by the user's board design.

$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(on)} \theta_{TJ}$$

Typical R_{θJA} using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

- a. 50°C/W when mounted on a 1 in² pad of 2oz copper.
- b. 105°C/W when mounted on a 0.04 in² pad of 2oz copper.
- c. 125°C/W when mounted on a 0.006 in² pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

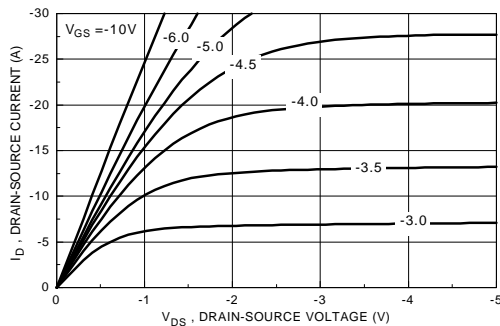


Figure 1. On-Region Characteristics

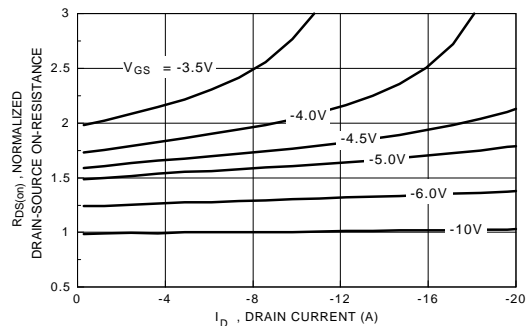


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

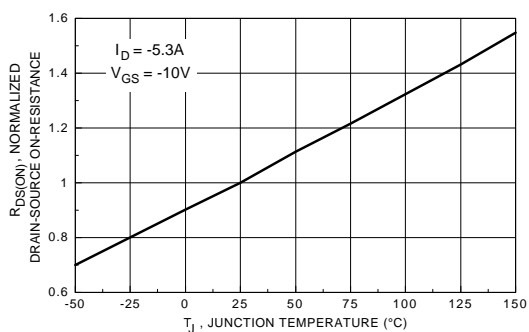


Figure 3. On-Resistance Variation with Temperature

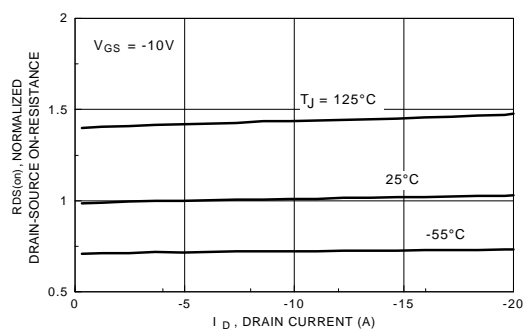


Figure 4. On-Resistance Variation with Drain Current and Temperature

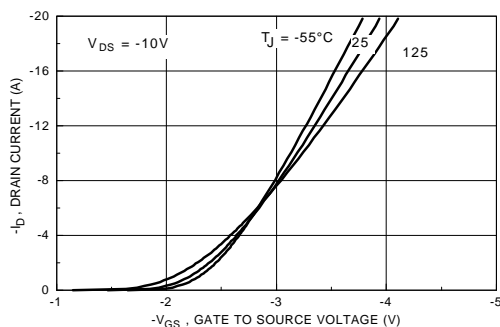


Figure 5. Transfer Characteristics

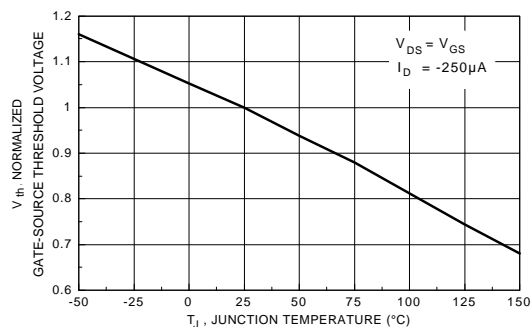


Figure 6. Gate Threshold Variation with Temperature

Typical Electrical Characteristics (continued)

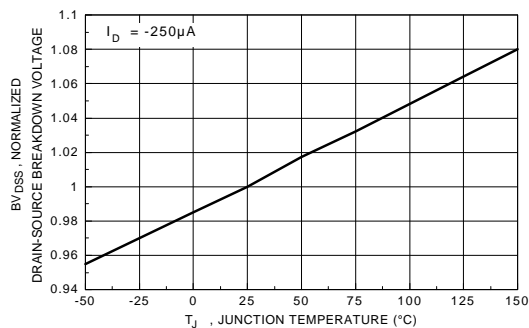


Figure 7. Breakdown Voltage Variation with Temperature

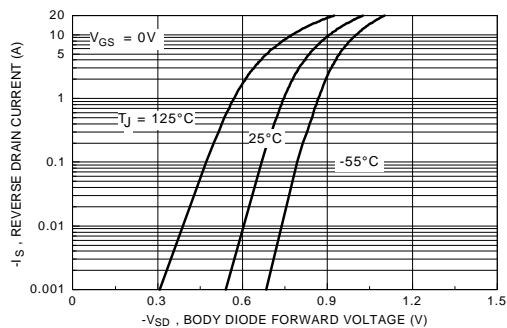


Figure 8. Body Diode Forward Voltage Variation with Source Current and Temperature

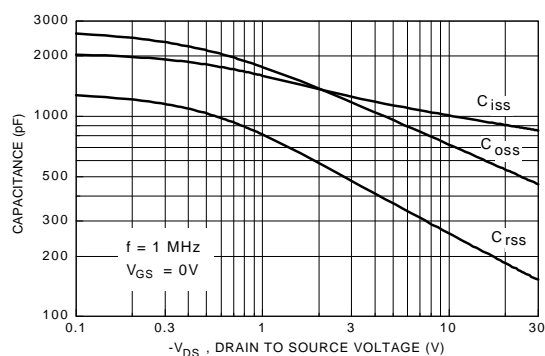


Figure 9. Capacitance Characteristics

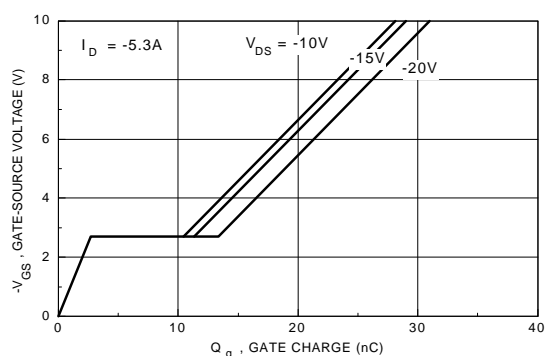


Figure 10. Gate Charge Characteristics

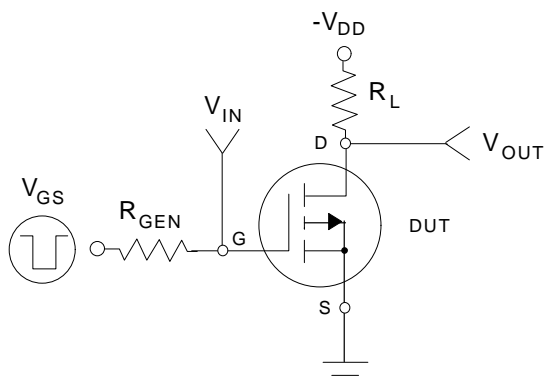


Figure 11. Switching Test Circuit

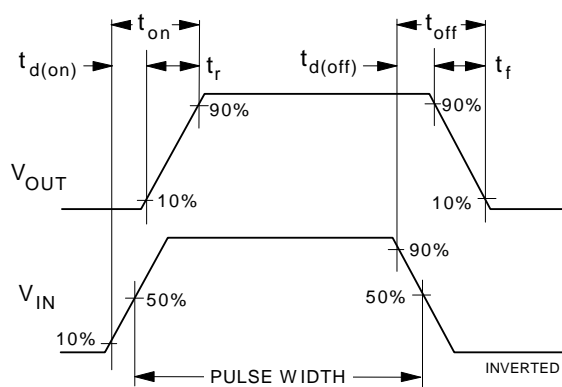


Figure 12. Switching Waveforms

Typical Electrical and Thermal Characteristics (continued)

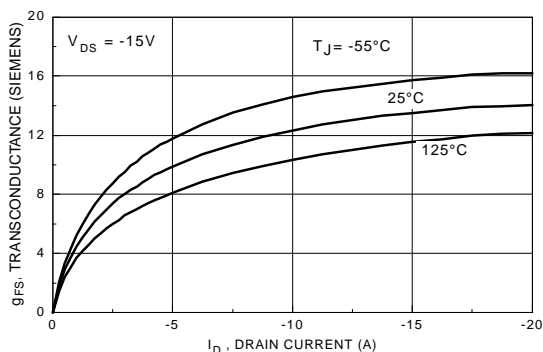


Figure 13. Transconductance Variation with Drain Current and Temperature

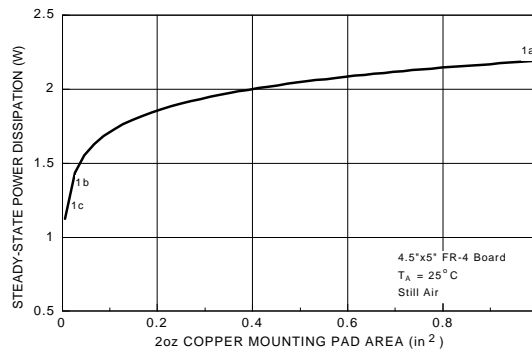


Figure 14. SO-8 Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.

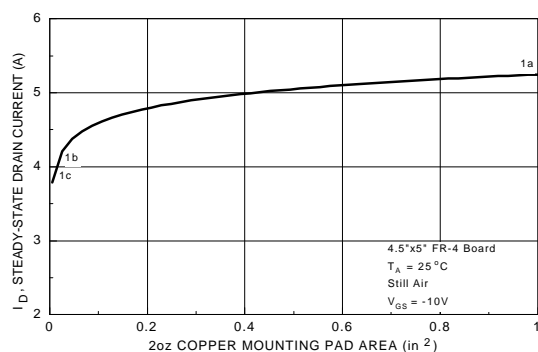


Figure 15. Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

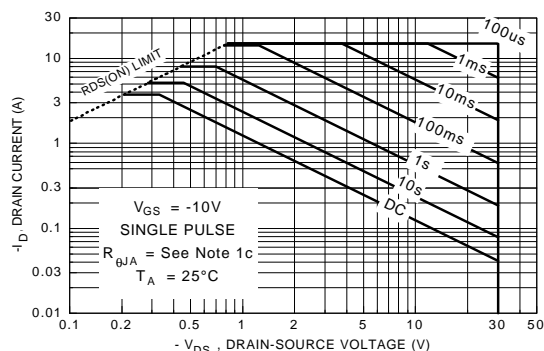


Figure 16. Maximum Safe Operating Area

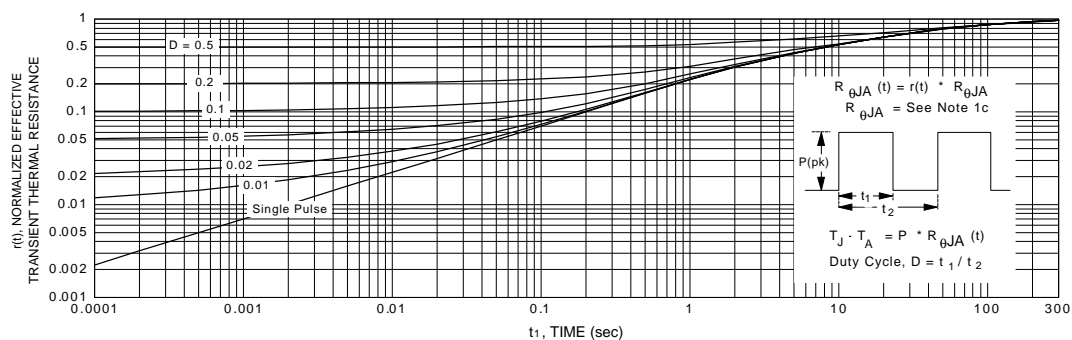


Figure 17. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

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