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November 2013

FQP85N06 — N-Channel QFET® MOSFET

FQP85N06

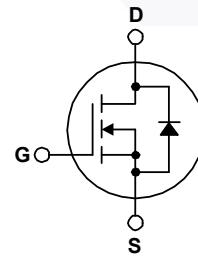
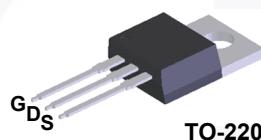
N-Channel QFET® MOSFET 60 V, 85 A, 10 mΩ

Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications.

Features

- 85 A, 60 V, $R_{DS(on)}$ = 10 mΩ (Max.) @ $V_{GS} = 10$ V, $I_D = 42.5$ A
- Low Gate Charge (Typ. 86 nC)
- Low C_{rss} (Typ. 165 pF)
- 100% Avalanche Tested
- 175°C Maximum Junction Temperature Rating



Absolute Maximum Ratings

$T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FQP85N06	Unit
V_{DSS}	Drain-Source Voltage	60	V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$) (Note 5)	85	A
	- Continuous ($T_C = 100^\circ\text{C}$)	60	A
I_{DM}	Drain Current - Pulsed	300	A
V_{GSS}	Gate-Source Voltage	± 25	V
E_{AS}	Single Pulsed Avalanche Energy	810	mJ
I_{AR}	Avalanche Current	85	A
E_{AR}	Repetitive Avalanche Energy	16.0	mJ
dv/dt	Peak Diode Recovery dv/dt	7.0	V/ns
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$)	160	W
	- Derate above 25°C	1.07	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +175	°C
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 seconds	300	°C

Thermal Characteristics

Symbol	Parameter	FQP85N06	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.94	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	62.5	°C/W

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQP85N06	FQP85N06	TO-220	Tube	N/A	N/A	50 units

Electrical Characteristics

$T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{\text{GS}} = 0 \text{ V}$, $I_D = 250 \mu\text{A}$	60	--	--	V
$\Delta \text{BV}_{\text{DSS}} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, Referenced to 25°C	--	0.06	--	$\text{V}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{\text{DS}} = 60 \text{ V}$, $V_{\text{GS}} = 0 \text{ V}$	--	--	1	μA
		$V_{\text{DS}} = 48 \text{ V}$, $T_C = 150^\circ\text{C}$	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{\text{GS}} = 25 \text{ V}$, $V_{\text{DS}} = 0 \text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{\text{GS}} = -25 \text{ V}$, $V_{\text{DS}} = 0 \text{ V}$	--	--	-100	nA

On Characteristics

$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{\text{DS}} = V_{\text{GS}}$, $I_D = 250 \mu\text{A}$	2.0	--	4.0	V
$R_{\text{DS(on)}}$	Static Drain-Source On-Resistance	$V_{\text{GS}} = 10 \text{ V}$, $I_D = 42.5 \text{ A}$	--	0.008	0.010	Ω
g_{FS}	Forward Transconductance	$V_{\text{DS}} = 25 \text{ V}$, $I_D = 42.5 \text{ A}$	--	54	--	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{\text{DS}} = 25 \text{ V}$, $V_{\text{GS}} = 0 \text{ V}$, $f = 1.0 \text{ MHz}$	--	3170	4120	pF
C_{oss}	Output Capacitance		--	1150	1500	pF
C_{rss}	Reverse Transfer Capacitance		--	165	220	pF

Switching Characteristics

$t_{\text{d(on)}}$	Turn-On Delay Time	$V_{\text{DD}} = 30 \text{ V}$, $I_D = 42.5 \text{ A}$, $R_G = 25 \Omega$	--	40	90	ns
t_r	Turn-On Rise Time		--	230	470	ns
$t_{\text{d(off)}}$	Turn-Off Delay Time		--	175	360	ns
t_f	Turn-Off Fall Time		--	170	350	ns
Q_g	Total Gate Charge	$V_{\text{DS}} = 48 \text{ V}$, $I_D = 85 \text{ A}$, $V_{\text{GS}} = 10 \text{ V}$	--	86	112	nC
Q_{gs}	Gate-Source Charge		--	20.5	--	nC
Q_{gd}	Gate-Drain Charge		--	36	--	nC

Drain-Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain-Source Diode Forward Current	(Note 5)	--	--	85	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	300	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{\text{GS}} = 0 \text{ V}$, $I_S = 85 \text{ A}$	--	--	1.5	V
t_{rr}	Reverse Recovery Time		$V_{\text{GS}} = 0 \text{ V}$, $I_S = 85 \text{ A}$, $dI_F / dt = 100 \text{ A}/\mu\text{s}$	--	70	ns
Q_{rr}	Reverse Recovery Charge		--	135	--	nC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature.
2. $L = 130 \mu\text{H}$, $I_{\text{AS}} = 85 \text{ A}$, $V_{\text{DD}} = 25 \text{ V}$, $R_G = 25 \Omega$, starting $T_J = 25^\circ\text{C}$.
3. $I_{\text{SD}} \leq 85 \text{ A}$, $dI/dt \leq 300 \text{ A}/\mu\text{s}$, $V_{\text{DD}} \leq \text{BV}_{\text{DSS}}$, starting $T_J = 25^\circ\text{C}$.
4. Essentially Independent of Operating Temperature.
5. Continuous Drain Current Calculated by Maximum Junction Temperature : Limited by Package.

Typical Characteristics

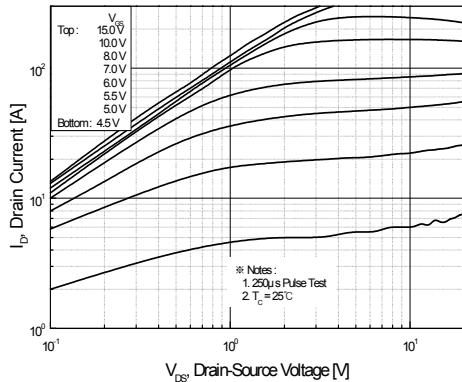


Figure 1. On-Region Characteristics

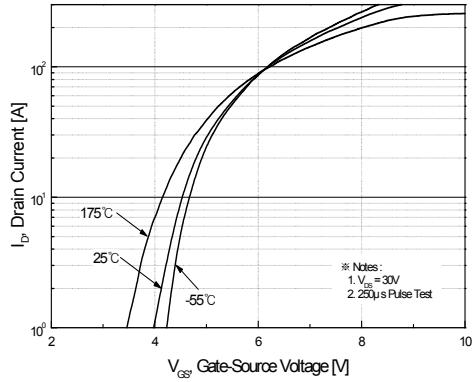


Figure 2. Transfer Characteristics

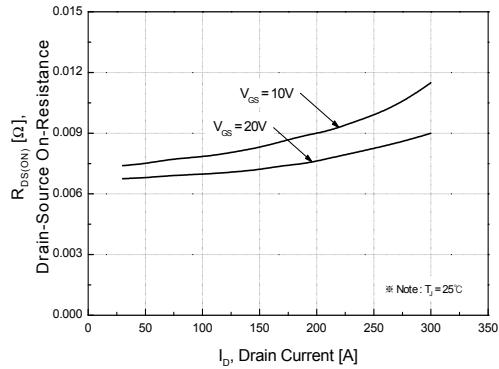


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

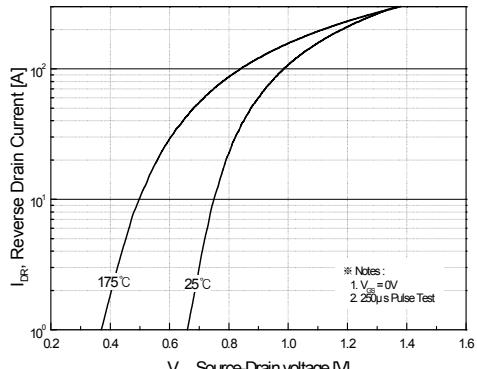


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

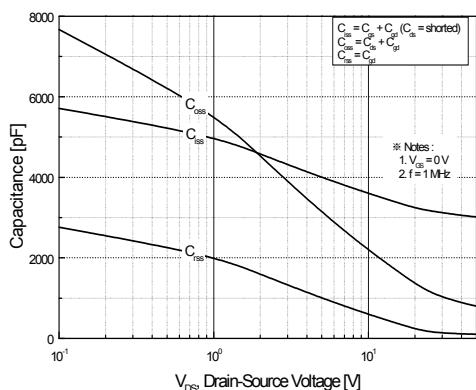


Figure 5. Capacitance Characteristics

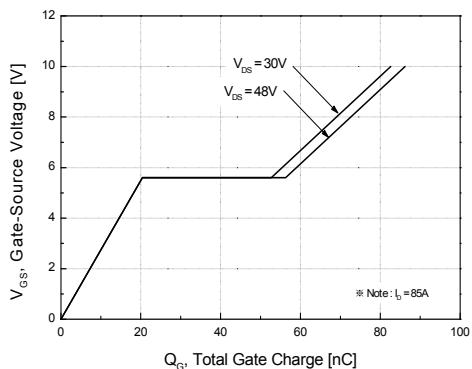


Figure 6. Gate Charge Characteristics

Typical Characteristics (continued)

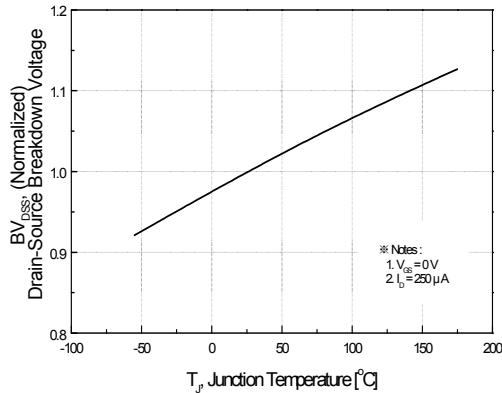


Figure 7. Breakdown Voltage Variation vs. Temperature

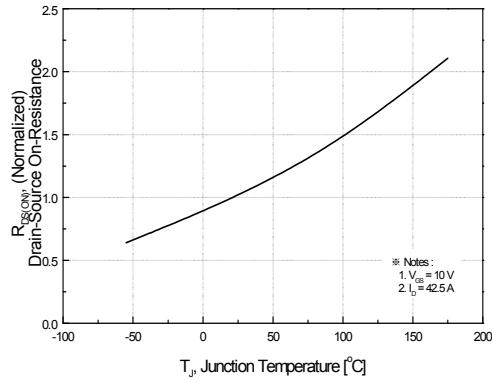


Figure 8. On-Resistance Variation vs. Temperature

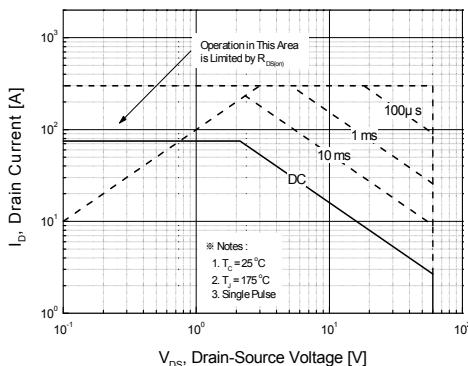


Figure 9. Maximum Safe Operating Area

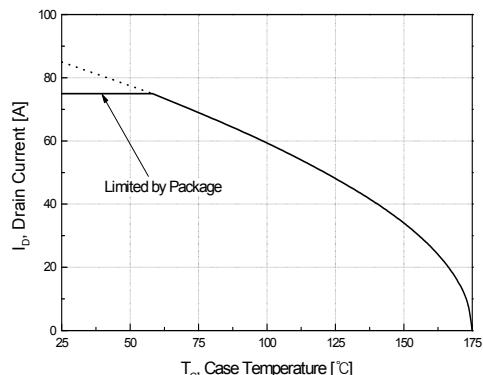


Figure 10. Maximum Drain Current vs. Case Temperature

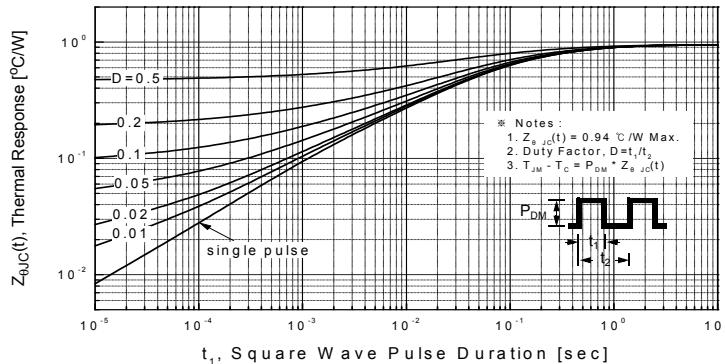


Figure 11. Transient Thermal Response Curve

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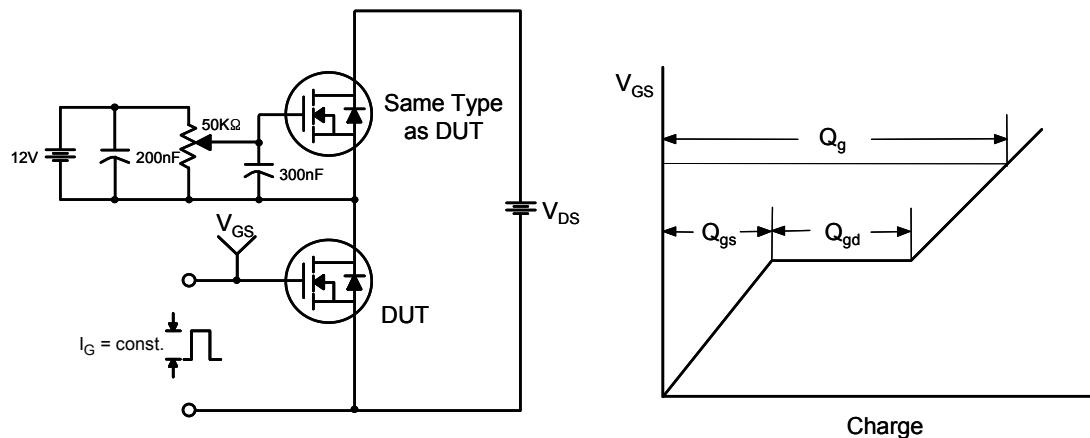


Figure 12. Gate Charge Test Circuit & Waveform

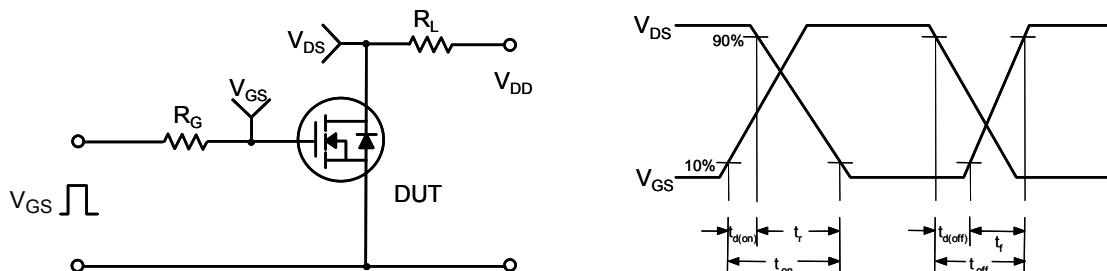


Figure 13. Resistive Switching Test Circuit & Waveforms

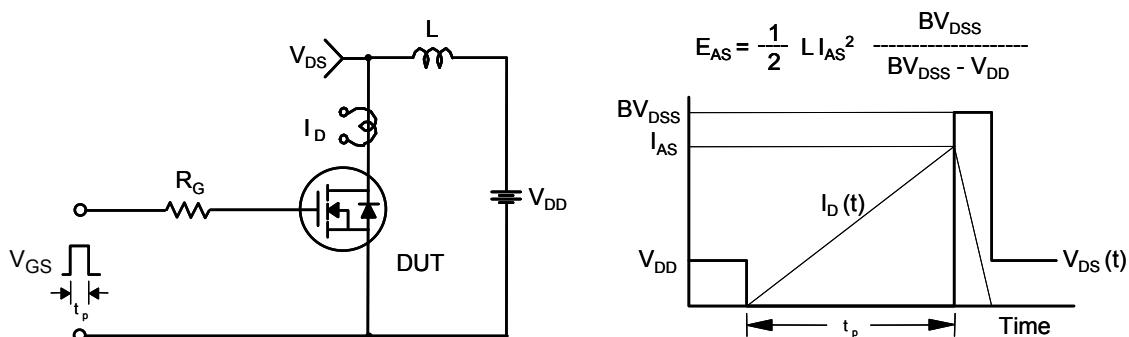


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

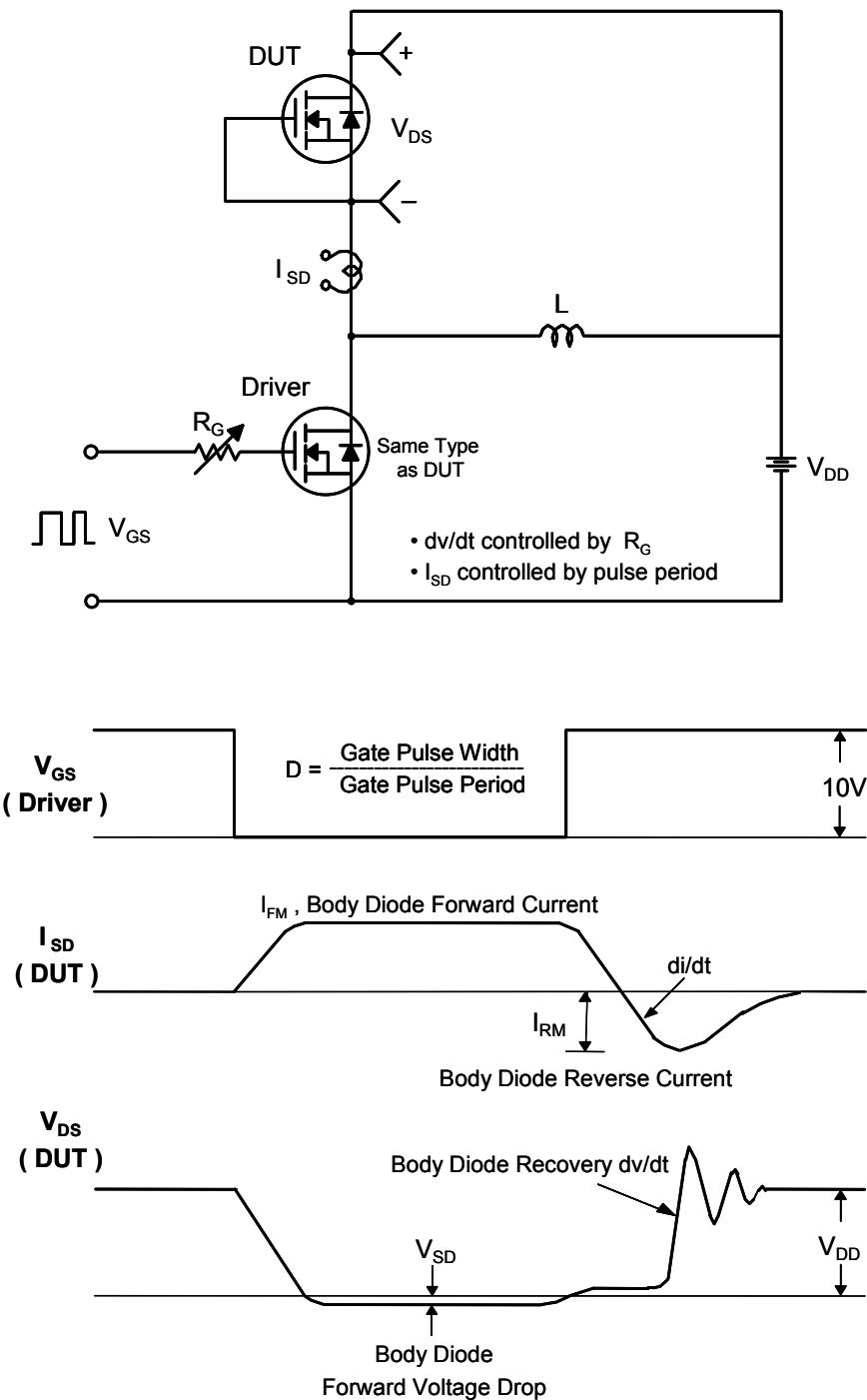
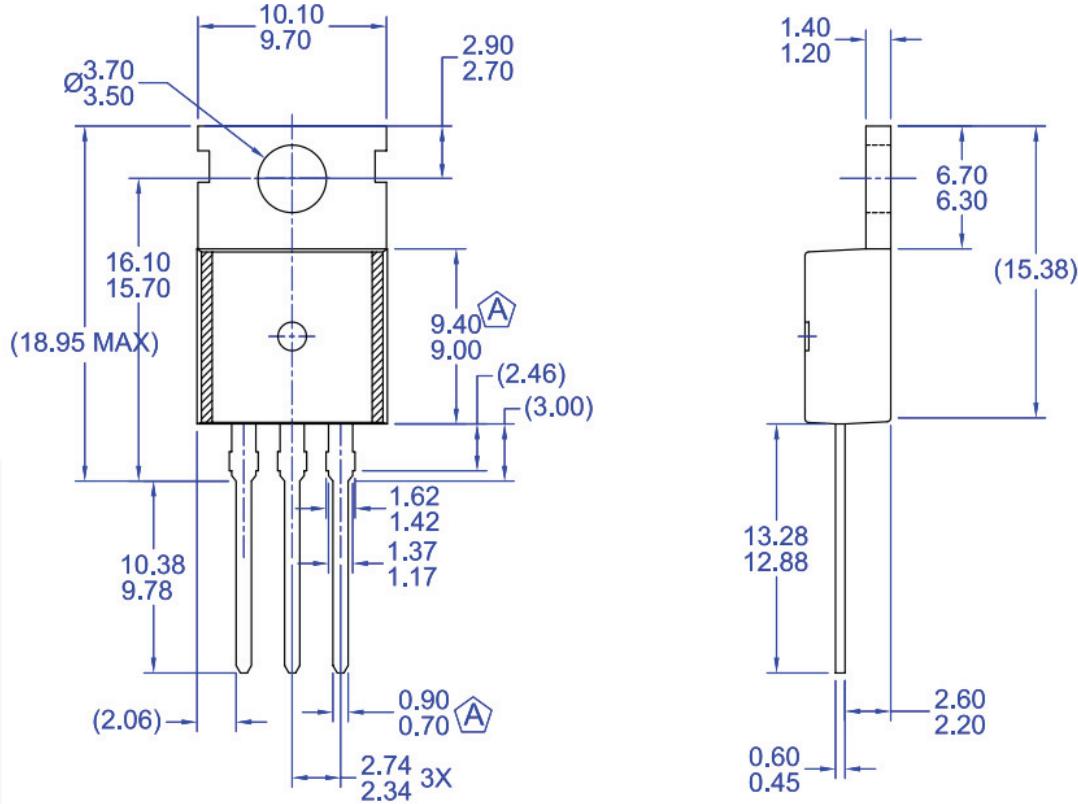


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions



NOTES:

- Ⓐ CONFORMS TO JEDEC TO-220 VARIATION AB EXCEPT WHERE NOTED
- Ⓑ ALL DIMENSIONS ARE IN MILLIMETERS.
- Ⓒ DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- Ⓓ DRAWING FILE/REVISION: MKT-TO220Y03REV1

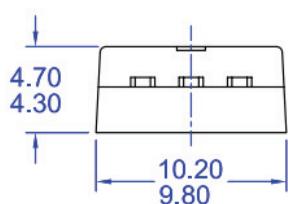


Figure 16. TO220, Molded, 3-Lead, Jedec Variation AB

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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