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HI5760EVAL1 Evaluation Board User's Manual

Application Note | October 1998 | AN9821.1

Description

The HI5760EVAL1 evaluation board provides a quick and easy method for evaluating the HI5760, 125 MSPS high speed DAC. The converter outputs a current into a load resistor to form a voltage which can be measured by using the included SMA connector. The amount of current out of the DAC is determined by an external resistor and either an internal or external reference voltage. The CMOS digital inputs have optional external termination resistors. The evaluation board also includes a VME digital interface that is compatible with the HSP-EVAL board, so DDS (Direct Digital Synthesis) can be performed with minimal setup time.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	CLOCK SPEED
HI5760EVAL1	25	Evaluation Platform	125MHz

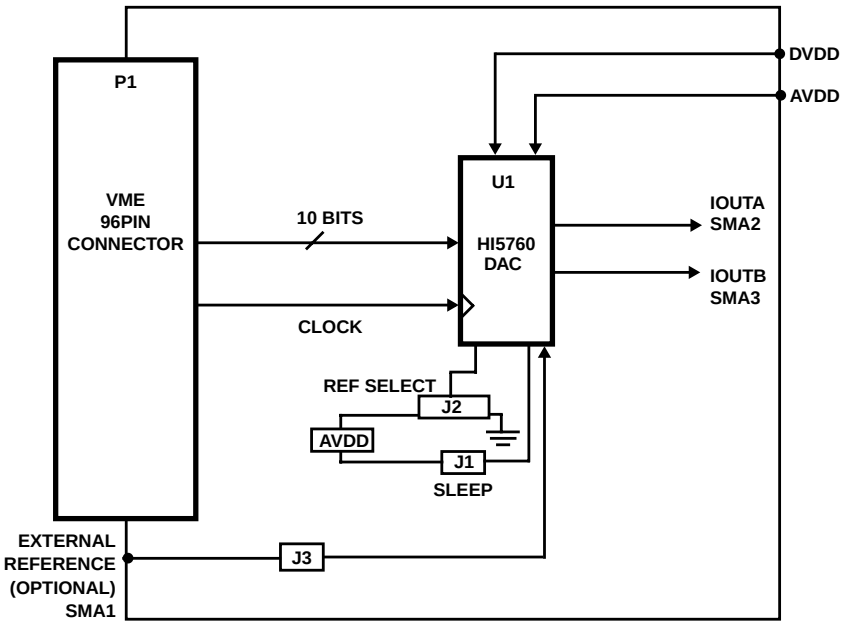
Features

- HI5760, 125 MSPS CMOS DAC
- Simple and Easy to Use
- Standard VME/DSP Interface, HSP-EVAL Compatible
- SMA Outputs
- Easily Selectable Internal or External Reference

Applications

- Single or Multi-Carrier Tone Generation
- Modulated Carrier Generation
- General DAC Performance Evaluation
- Amplitude Modulation Via External Reference

Functional Block Diagram



Functional Description

Voltage Reference

The HI5760 has an internal 1.2V voltage reference with a ±60ppm/^{0}C drift coefficient over the full temperature range of the converter. The REFLO pin (16) selects the reference. Access to pin 16 is provided through the center pin of Jumper J2. To enable the internal reference, it is necessary that the jumper be placed such that pin 16 is grounded (if facing the evaluation board so that the SMAs are on the user's left-hand side, then the jumper should be placed in the 'right' position of the three-stemmed jumper). The REFIO pin (17) provides access to the internal voltage reference, or can be overdriven if the user wishes to use an external source for the reference. Notice that a 0.1µF capacitor is placed as close as possible to the REFIO pin. This capacitor is necessary for ensuring a noise free reference voltage. If the user wishes to use an external reference voltage, jumper J3 must be in place and an external voltage reference provided via SMA1, labeled 'EXT REF'. The recommended limits of the external reference are between 15mV and 1.2V. Performance of the converter can be expected to decline as the reference voltage is reduced due to the reduction in LSB voltage size. If the user wants to amplitude modulate the DAC, they can overdrive the REFIO pin with a waveform. The input multiplying bandwidth of the REFIO input is approximately 1.4MHz. It is necessary that the multiplying signal be DC offset so that the minimum and maximum peaks of the signal do not exceed the limits imposed above. Jumper J2 must be changed so that pin 16 is tied high (the supply voltage, which is the 'left' position of J2) when using an external reference. The output current of the converter, IOUTA and IOUTB, is a function of the voltage reference used and the value of R_{SET} (R14 on the schematic).

Outputs

The output current of the device is set by choosing R_{SET} and V_{REF} such that the resultant of the following equation is between 2mA and 20mA:

$I_{OUT} = 32 \times V_{REF}/R_{SET}$.

For example, using the internal V_{REF} of 1.2V and an R_{SET} (R14 on the schematic) value of 1.91kΩ results in an I_{OUT} of approximately 20mA (maximum allowed). Choose the output loading so that the 'Output Voltage Compliance Range' is not violated (0 to 1.25V). If an external V_{REF} is chosen, it should not exceed +1.2V.

The output can be configured to drive a load resistor, a transformer, an operational amplifier, or any other type of output configuration so long as the output voltage compliance range and the maximum output current is not violated.

Load Resistor Output

The evaluation board comes with the simple resistor load output configuration. Both IOUTA and IOUTB have a 50Ω resistor connected to ground next to their respective SMAs. See the attached schematic for clarification.

Sleep

The converter can be put into 'sleep' mode by connecting pin 15 to either of the converter's supply voltages. For normal operation, it is recommended that pin 15 be tied to ground. However, the sleep pin does have an active pulldown current, so the pin can be left disconnected for normal operation. On the evaluation board, jumper J1 is provided for controlling the sleep pin. Remove the jumper from J1 for normal operation and replace it for sleep mode.

Power Supply(s) and Ground(s)

The user can operate from either a single supply or dual supplies. The DAC is designed to function with the digital and analog voltages at the same value. The evaluation board contains two power supply connections to allow for measuring the current drawn from the digital and analog sections independently. For single supply mode, it is recommended that a single power supply wire be attached to either DV_{DD1} or AV_{DD1}, and then a jumper wire placed from E2 to E3 (holes). A single ground wire should be attached to either DCOM1 or ACOM1 from the power supply. These grounds are identical, as the evaluation board uses a single ground plane. The user can select to use dual ground planes in their design connected at a single point near the converter (this is the recommended configuration). For dual supply mode, connect a power supply wire to both AV_{DD1} and DV_{DD1} and ground wires to DCOM1 and ACOM1 independently.

Getting Started

A summary of the external supplies, equipment, and signal sources needed to operate the board is given below:

1. +5V for HI5760.
2. Data generator capable of generating 10-bit patterns. The HSP-EVAL with the HSP45116 NCOM daughter board is an option (see *'Learning Your Way Around'*).
3. Square wave clock source (usually part of the Data Generator).
4. Spectrum analyzer or oscilloscope for viewing the output of the converter.

Attach a +5V power supply to the evaluation board. Connect the 10 input bits from the data generator to the evaluation board, preferably by using a male, 64 or 96-pin VME (Versa Module Eurocard) connector that mates with the eval board. Connect the clock source to the eval board, also preferably through the 64-pin connector. Failure to make clean and short connections to the data input lines and clock source will result in a decrease in spectral performance.

Using a coaxial cable with the proper SMA connector, attach the output of the converter, either IOUTA or IOUTB, to the measurement equipment that will be evaluating the converter's performance. Make sure that the jumpers are in their proper placement. Consult the 'Voltage Reference' section and the 'Sleep' section of this document for a definition of the jumpers' functionality. Optimum single-ended performance is usually achieved by either grounding or equally terminating the unused output so that its loading matches that of the output being measured.

Learning Your Way Around

Direct Digital Synthesis

To ensure that everything on the board is configured properly and functional, it is suggested that the following test be performed. The board test requires:

1. HI5760 Evaluation Board.
2. Spectrum analyzer.
3. HSP-EVAL Board with the HSP45116 NCOM Daughter Board attached and included software, NCOMCTRL (or a data/pattern generator).
4. Personal computer with a parallel port.
5. 50Ω SMA cable.

Two +5V power supplies. One for the DAC Eval Board and one for the HSP Eval Board.

Connections

Note: If the HSP-EVAL Board is to be used, it is highly recommended that the user obtain the User's Manual, the datasheet for the HSP45116 NCOM, and the User's Manual for the HSP45116-DB. This platform is capable of testing the converter up to 25 MSPS, which is the speed of the HSP-EVAL's on-board clock. The user can choose to substitute this clock with a slower one, but the DSP chip and DSP Eval Board are only designed to work at a maximum of 25MHz (a 52MHz version of this DSP chip does exist but not in this evaluation platform; see the HSP45116A). For testing of the HI5760 at higher speeds, it is recommended that the user obtain a high speed data generator capable of generating 10-bit patterns at clock speeds up to at least 125MHz.

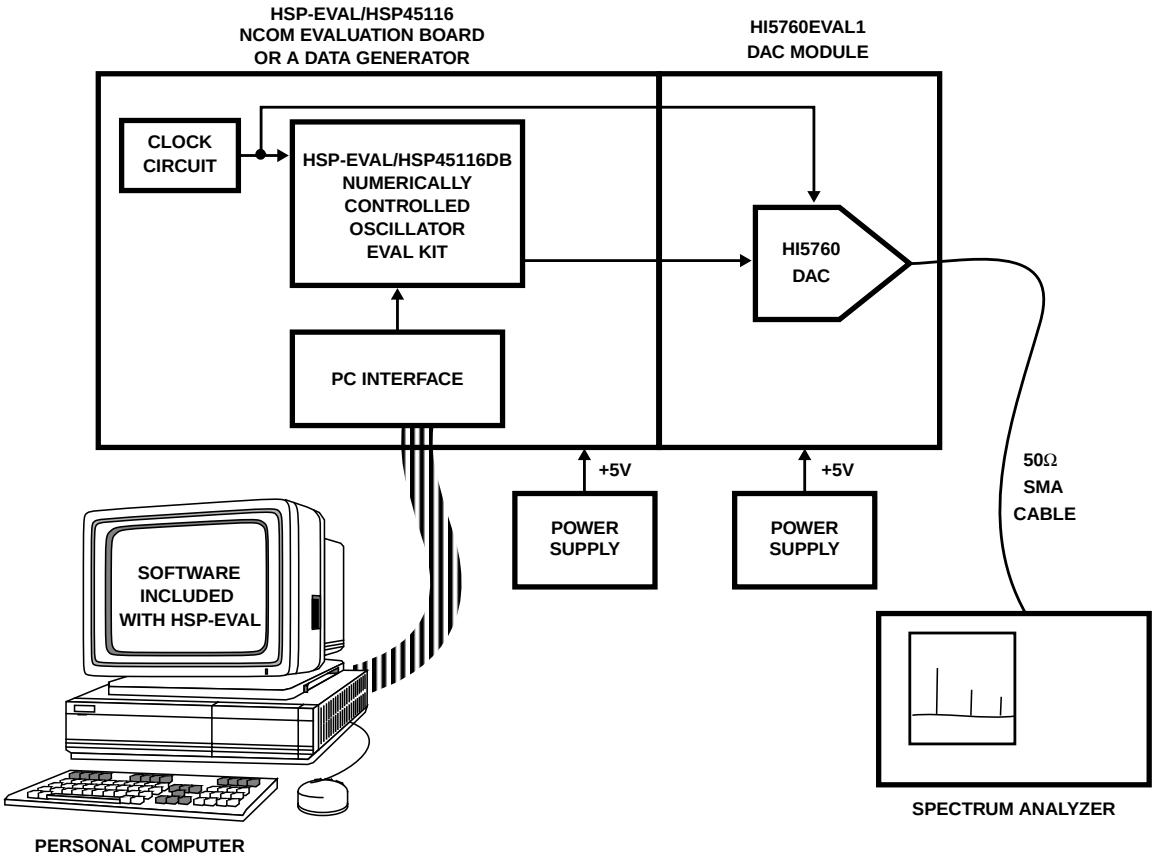


FIGURE 1. INTERSIL HI5760/DDS EVALUATION SYSTEM SETUP BLOCK DIAGRAM

HSP-Eval Setup for DDS

Attach the HSP-EVAL and the HSP45116 Daughter Board together. Consult their respective user manuals for details. Connect the HI5760EVAL1 board to the P2 connector of the HSPEVAL board. Then connect these to an IBM compatible PC via the parallel port. Provide power to both boards. To run the software (NCOMCTRL) that accompanied the HSP evaluation kit, place the diskette into the A: drive of the PC and type:

A:NCOMCTRL,

which will run the HSP45116 Control Panel software. Set the control panel's selections to the following and check the output of the DAC at either IOUTA or IOUTB for a frequency equal to 1.63MHz.

The clock select of the control panel should be set to 'Osc. CLK'. The control signals should be as follows:

0$\overline{\text{ENPHREG}}$

0$\overline{\text{CLROFR}}$

1$\overline{\text{LOAD}}$

0$\overline{\text{BINFMT}}$

1PMSEL

The amplitude of the real output (RIN0-15) should be 8000_{HEX} for full scale output. The center frequency register can be set to $10ABCDEF_{HEX}$ for a 1.63MHz tone. The Offset Frequency, Phase Offset, and Time Accumulator Registers should all be set to zeros. The spurious free dynamic range that can be expected is typically 70dBc with this setup operating at this frequency.

Appendix A Description of Architecture

The segmented current source architecture has the ability to improve the converter's performance by reducing the amount of current that is switching at any one time. In traditional architectures, major transition points required the converter to switch on or off large amounts of current. In a traditional 10-bit R/2R ladder design, for example, the midscale transition required approximately equal amounts of currents switching on and off. In a segmented current source arrangement, transitions such as midscale become one in which you simply have an additional intermediate current source turning on and several minor ones turning off. In the case of the HI5760, there are 31 intermediate current segments that represent the 5 MSBs and five, binary-weighted current sources representing each of the five LSBs. See the Functional Block Diagram in the datasheet for a visual representation. To relate the midscale transition example to the HI5760, consider the following: The code 0111111111 would be represented by 15 intermediate current segments and each of the 5 LSB current sources all turned on. To transition to code 1000000000 would simply require turning off the 5 LSB current sources and turning on the next intermediate current segment, bringing the total amount of current switching at this 'major' code transition equal to the same amount switching at 30 other code transition points in the code ramp from 0 to 1023, so that the total glitch energy is distributed more evenly.

Appendix B Pin Descriptions

PIN NO.	PIN NAME	PIN DESCRIPTION
1-10	D9 (MSB) Through D0 (LSB)	Digital data bit-9, (most significant bit) through digital data bit-0, (least significant bit).
11-14	NC	No Connect. Recommend ground.
15	SLEEP	Control Pin for Power-Down Mode. Sleep mode is active high; Connect to ground for normal mode. Sleep pin has internal 20µA active pull-down current.
16	REFLO	Connect to analog ground to enable internal 1.2V reference or connect to AV_{DD} to disable internal reference.
17	REFIO	Reference voltage input if internal reference is disabled. Reference voltage output if internal reference is enabled. Use 0.1µF cap to ground when internal reference is enabled.
18	FSADJ	Full Scale Current Adjust. Use a resistor to ground to adjust full scale output current. Full scale output current = 32 x V_{REFIO}/R_{SET}.
19	COMP1	For use in reducing bandwidth/noise. Recommended: Connect 0.1µF to AV_{DD}.
20	ACOM	Analog Ground.
21	IOUTB	The complementary current output of the device. Full scale output current is achieved when all input bits are set to binary 0.
22	IOUTA	Current output of the device. Full scale output current is achieved when all input bits are set to binary 1.
23	COMP2	Connect to ACOM directly or through a 0.1µF capacitor.
24	AV_{DD}	Analog supply (+3V to +5V).
25	NC	No connect.
26	DCOM	Digital ground.
27	DV_{DD}	Digital supply (+3V to +5V).
28	CLK	Input for clock. Positive edge of clock latches data.

Appendix C Circuit Board Layout

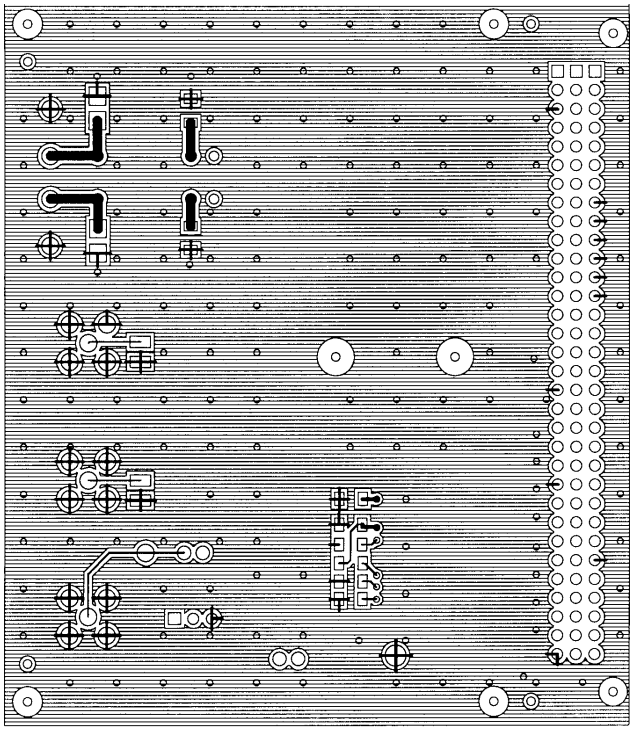


FIGURE 2. PRIMARY SIDE

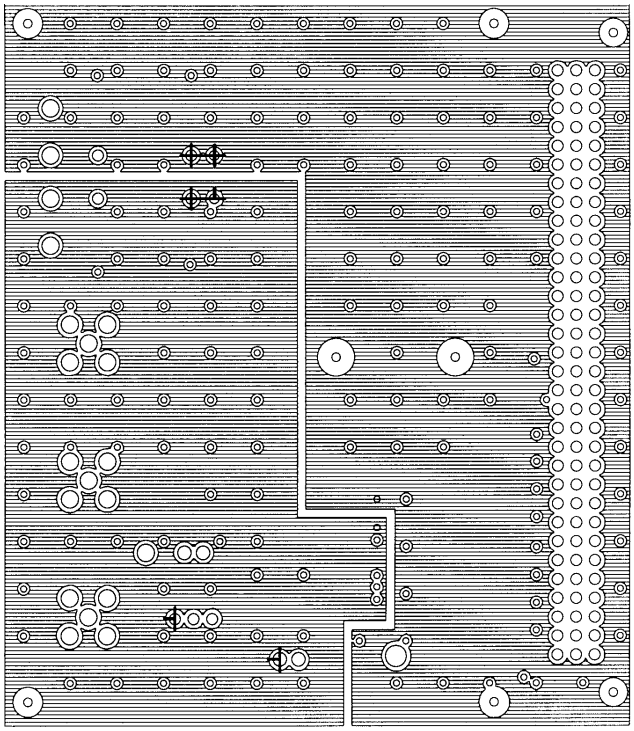


FIGURE 3. POWER LAYER (2)

Appendix C Circuit Board Layout (Continued)

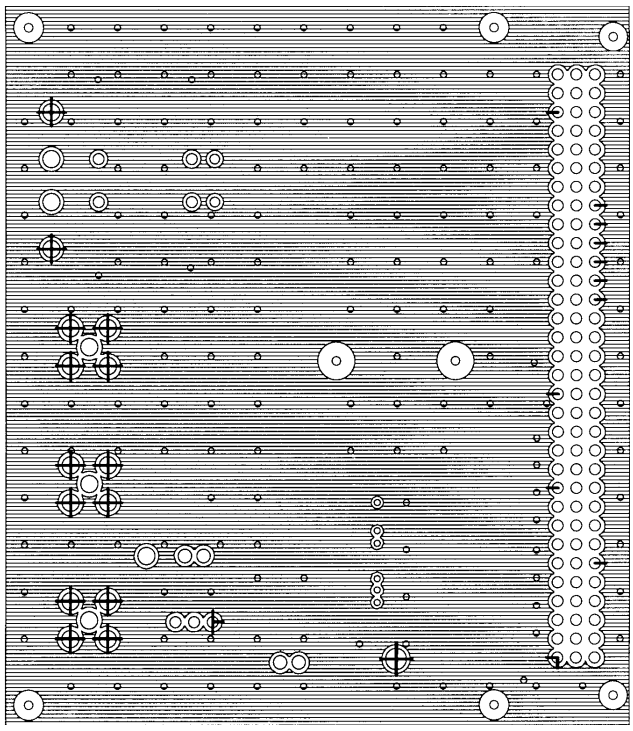


FIGURE 4. GROUND LAYER (3)

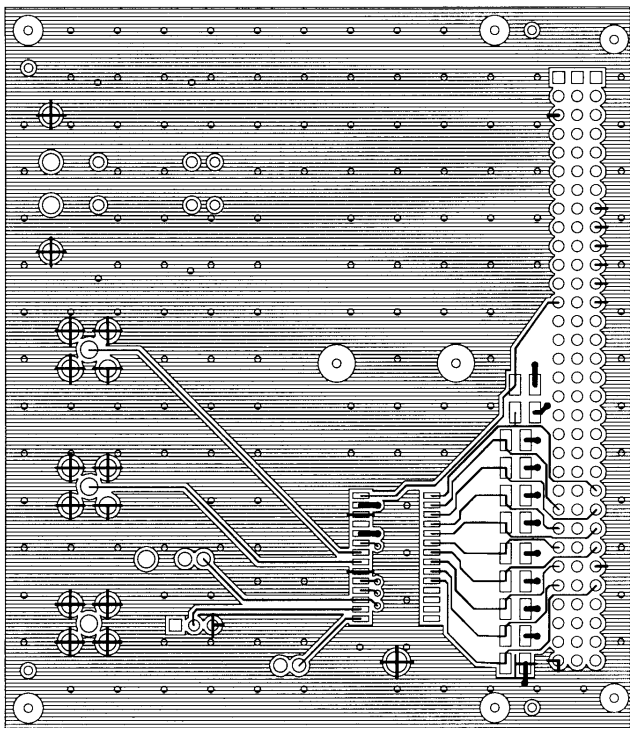
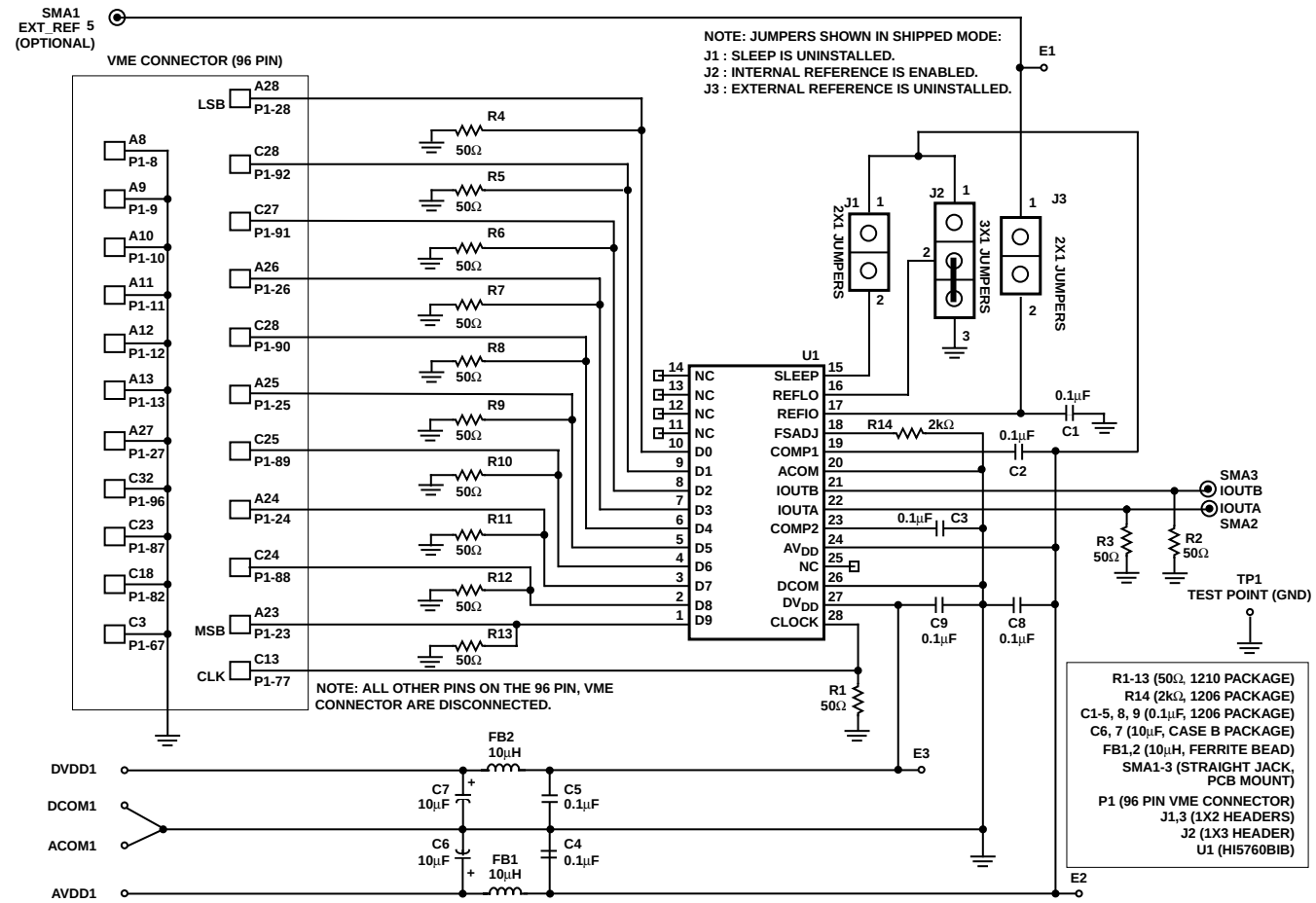


FIGURE 5. SECONDARY SIDE

Appendix D Schematic



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