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Using the ISL6420 PWM Controller Evaluation Board

Application Note | November 10, 2004 | AN1159.0

Advanced Single Synchronous Buck Pulse-Width Modulation (PWM) Controller

The ISL6420 simplifies the work of implementing a complete control and protection scheme for a high-performance DC-DC buck converter. Designed to drive N-channel MOSFETs in a synchronous rectified buck topology, the ISL6420 integrates the control, output adjustment, monitoring and protection functions into a single package.

The ISL6420 provides simple, single feedback loop, voltage mode control with fast transient response. The output voltage of the converter can be precisely regulated to as low as 0.6V, with a maximum tolerance of ±1.0% over temperature and line voltage variations.

The operating frequency is fully adjustable from 100kHz to 1.4MHz. High frequency operation offers cost and space savings.

The error amplifier features a 15MHz gain-bandwidth product and 6V/µs slew rate that enables high converter bandwidth for fast transient response. The resulting PWM duty cycle ranges from 0% to 100%. Selecting the capacitor value from the ENSS pin to ground sets a fully adjustable PWM soft-start; while pulling ENSS pin LOW disables the controller.

The ISL6420 monitors the output voltage and generates a PGOOD (power good) signal when soft-start is complete and the output is within regulation. A built-in overvoltage protection circuit prevents the output voltage from going above typically 115% of the set point. Protection from overcurrent conditions is provided by monitoring the $r_{DS(ON)}$ of the upper MOSFET to inhibit the PWM operation appropriately. This approach simplifies the implementation and improves efficiency by eliminating the need for a current sensing resistor. The IC also features voltage margining for networking DC-DC converter applications.

ISL6420 Reference Design

The ISL6420 evaluation board highlights the operation of the IC in an embedded application. The evaluation board is configured for an output voltage of 3.3V and 10A maximum load.

TABLE 1.

BOARD NAME	IC	PACKAGE
ISL6420EVAL3	ISL6420IR	20 Ld QFN

Quick Start Evaluation

The evaluation board is shipped “ready to use” right from the box. The board has been optimized for a 12V input from a standard power supply but can accept a range from 4.5V to 16V. The board can be connected to the source and load with the help of stand-off terminals provided.

Recommended Test Equipment

To test the functionality of the ISL6420, the following equipment is recommended:

- An adjustable 12V, 8A capable bench power supply
- An electronic load
- Four channel oscilloscope with probes
- Precision digital multimeter

Power and Load Connections

Refer to the ISL6420EVAL3 schematic for reference designators.

Jumper Settings - JP1 controls what terminal post is connected to the VIN pin of the IC (See the Input Voltage explanation below). JP2 and JP3, when shorted with a jumper, pull the GPIO2 and GPIO1 pins to GND. With the jumpers removed, GPIO2 and GPIO1 will be floating.

Input Voltage - The ISL6420EVAL3 reference design is optimized for an input supply of 12V, however, the input supply can range from 4.5V to 16V.

If using an input supply ranging from 5.6V to 16V, short pins 1 and 2 of jumper JP1. In this mode, the VIN post (P1) is connected to the drain of the upper MOSFET and the VIN pin of the IC and the chip is powered by the 5V output (VCC5, post P5) of the internal LDO.

To use a 5V ±10% input supply, short pins 2 and 3 of JP1 and connect the power supply to the VIN (P1) post and the VCC5 (P5) post. This will disable the internal LDO and the chip will be powered by the input power supply.

CAUTION: When JP1 pins 2 & 3 are shorted, applying voltages >6V can damage the IC.

For quick start evaluation, adjust the power supply to provide the 12V input voltage and short pins 1 and 2 of JP1. With the power supply turned off, connect the positive lead of the 12V supply to the VIN post (P1) and the ground lead to the GND post (P2).

Output Voltage Loading and Monitoring - Connect the positive lead of the electronic load and the positive lead of a digital multimeter to the VOUT post (P3) and the ground lead to the GND post (P4). You can use the scope probe terminal (SC1) to monitor VOUT with an oscilloscope.

Start-up

The Power On Reset (POR) function initiates the soft-start sequence. An internal 10µA current source charges an external capacitor connected to the ENSS (P9) pin from 0V to 3.3V. When the ENSS pin reaches 1V the error amplifier reference voltage ramps from 0V to 0.6V following the slope of the ENSS pin voltage.

There are two distinct start-up methods for the ISL6420. The first method is invoked through the application of power to the IC. The soft-start feature allows for a controlled turn on of the output once the POR threshold of the input voltage has been reached. Figure 1 shows the start-up profile of the regulator in relation to the start-up of the 12V input supply.

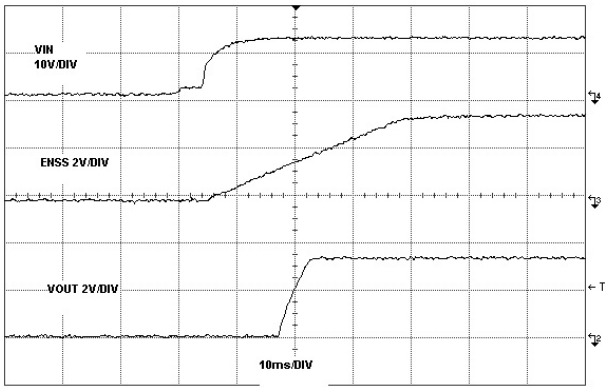


FIGURE 1. SOFT-START

The second method of start-up is through the use of the enable feature. Holding the ENSS (P9) pin on the ISL6420 below 1V will disable the regulator by forcing both the upper and lower MOSFETs off. Releasing the pin allows the regulator to start-up.

Shutdown

As discussed in the previous section, if the ENSS pin is pulled down and held below 1V the regulator will be turned off. Figure 2 shows the shutdown profile of the regulator with the ENSS pin pulled low. Figure 3 shows the shutdown of the regulator when powering down of the input supply.

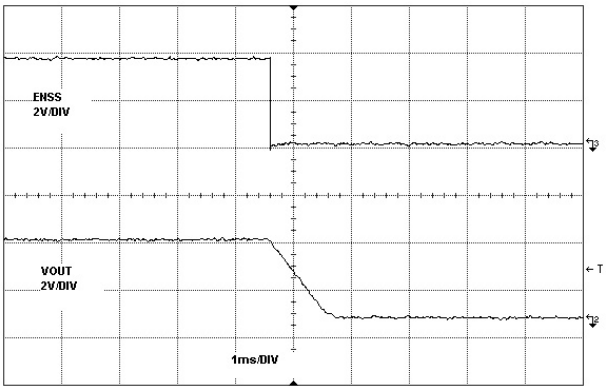


FIGURE 2. SHUTDOWN USING ENSS

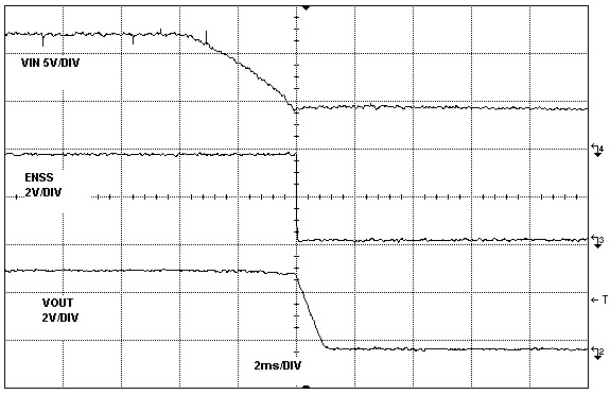


FIGURE 3. POWER DOWN OF THE INPUT SUPPLY

Output Performance

Switching Frequency

The switching frequency of the ISL6420 can be adjusted from 100kHz to 1.4MHz by connecting a resistor from the RT pin to GND. The free running frequency of the IC is 300kHz when the RT pin is tied to VCC5. The evaluation board has a 0Ω resistor (R9) connecting RT to VCC5. By removing this 0Ω resistor and placing a resistor (R4) from this pin to GND, the nominal 300kHz switching frequency can be increased or decreased as per Figure 4.

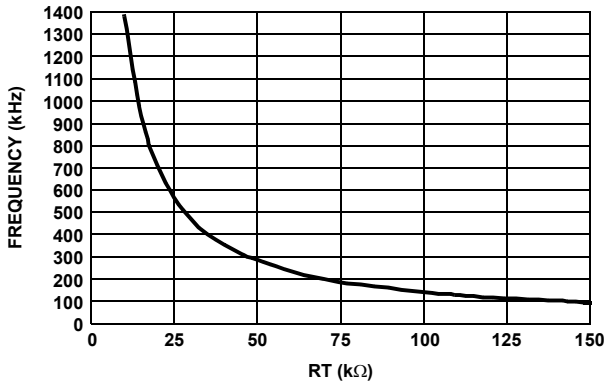


FIGURE 4. RT vs SWITCHING FREQUENCY

Output Ripple

Figure 5 shows the ripple voltage on the output of the regulator at the free running 300kHz frequency and at 600kHz.

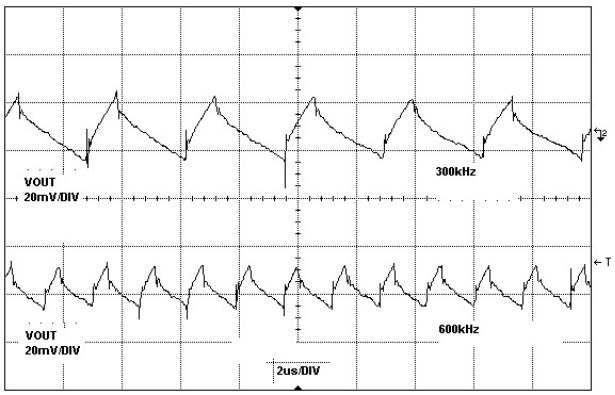


FIGURE 5. OUTPUT RIPPLE

Efficiency

ISL6420 based regulators enable the design of highly efficient systems. The efficiency of the evaluation board using a 12V and a 5V input supply is shown in Figure 6.

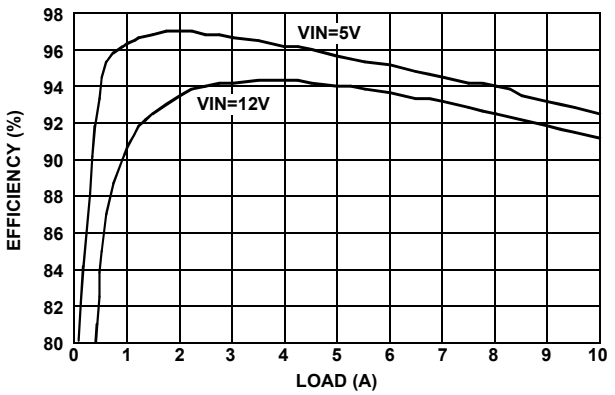


FIGURE 6. EVALUATION BOARD EFFICIENCY

Power Good

PGOOD will be true (open drain) when the FB pin voltage is within ±10% of the reference voltage and the soft-start sequence is complete, i.e., once the soft-start capacitor is finished charging. The status of PGOOD can be monitored at the PGOOD test point (TP1).

Overcurrent Protection

The overcurrent function cycles the soft-start function in a hiccup mode to provide fault protection. Figure 7 shows the overcurrent hiccup mode.

The overcurrent function protects the converter from a shorted output by using the upper MOSFET's $R_{DS(ON)}$ to monitor the current. This method enhances the converter's efficiency and reduces cost by eliminating a current sensing resistor.

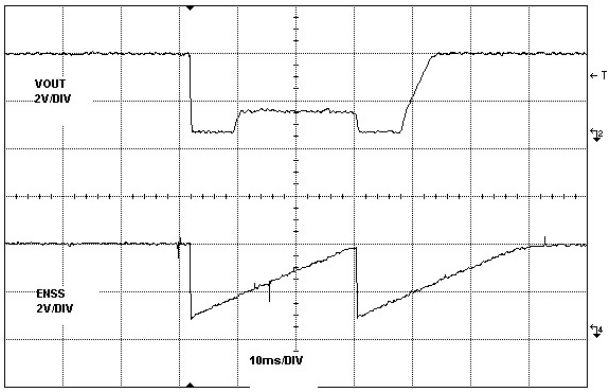


FIGURE 7. OVERCURRENT HICCUP MODE

A resistor, R_{OCSET} (R8), programs the overcurrent trip level. The PHASE node voltage is compared to the voltage on the OCSET pin, while the upper FET is on. A current (100µA typically) is pulled from the OCSET pin to establish this voltage across an external resistor. If PHASE is lower than OCSET, while the upper FET is on, then an overcurrent condition is detected for that clock cycle. The pulse is immediately terminated, and a counter is incremented. If an overcurrent condition is detected for 8 consecutive clock cycles, and the circuit is not in soft-start, the ISL6420 enters into hiccup mode. During hiccup, the external capacitor on the ENSS pin is discharged and soft-start is initiated. During soft-start, pulse termination limiting is enabled, but the 8-cycle hiccup counter is held in reset until soft-start is completed.

The overcurrent function will trip at a peak inductor current (I_{PEAK}) determined by,

$$I_{PEAK} = \frac{I_{OCSET} \bullet R_{OCSET}}{R_{DS(ON)}}$$

where I_{OCSET} is the internal OCSET current source.

The OC trip point varies mainly due to the MOSFET's $r_{DS(ON)}$ variations. To avoid overcurrent tripping in the normal operating load range, calculate the R_{OCSET} resistor from the equation above using:

1. The maximum $R_{DS(ON)}$ at the highest junction temperature.
2. The minimum I_{OCSET} from the specification table.

Determine I_{PEAK} for $I_{PEAK} > I_{OUT(MAX)} + (\Delta I)/2$,

where ΔI is the output inductor ripple current. A small ceramic capacitor should be placed in parallel with R_{OCSET} to smooth the voltage across R_{OCSET} in the presence of switching noise on the input voltage.

The overcurrent trip point on the evaluation board has been set to 18A. Figure 7 shows the overcurrent hiccup mode.

Transient Performance

Figure 8 shows the response of the output when subjected to transient loading from 10mA to 10A.

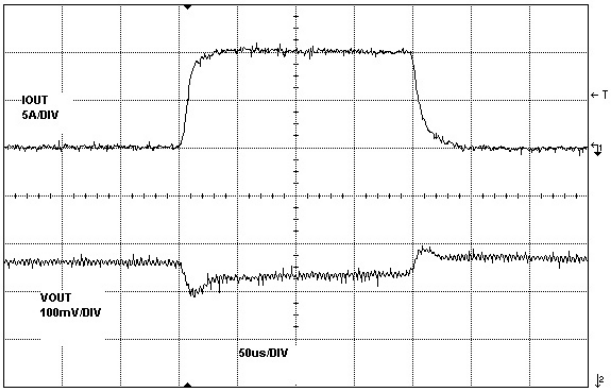


FIGURE 8. TRANSIENT RESPONSE

Voltage Margining

Voltage margining mode is enabled by connecting a margining set resistor (R6) from the VMSET pin to ground. This resistor to ground will set a current, which is switched to the FB pin. The current will be equal to 2.468V divided by the value of the external resistor tied to the VMSET pin.

The GPIO1 (P8) and GPIO2 (P7) pins control the current switching as per Table 2 below. The power supply output increases when GPIO2 is HIGH and decreases when GPIO1 is HIGH. Using a jumper to short the pins of JP2 and JP3 will pull GPIO1 and GPIO2 LOW. Remove these jumpers to pull GPIO1 or GPIO2 HIGH for voltage margining. The amount that the output voltage of the power supply changes with voltage margining will be equal to 2.468V times the ratio of the external feedback resistor (R2) and the external resistor tied to VMSET (R6).

TABLE 2.

GPIO1	GPIO2	VOUT
L	L	No Change
L	H	+ Delta VOUT
H	L	- Delta VOUT
H	H	Ignored

The evaluation board has a 330kΩ VMSET resistor (R6) setting a current:

IVM = 2.468V/330kΩ = 7.48µA

and

V(delta) = 7.48µA*20.5kΩ = 0.153V

Figure 8 shows the output voltage in voltage margining mode for various VMSET resistor values.

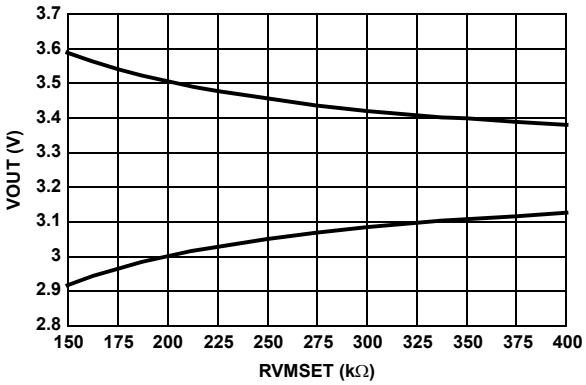


FIGURE 9. CHANGE IN OUTPUT VOLTAGE FOR VARIOUS RESISTORS

The slew time of the current is set by an external capacitor (C13) on the CDEL pin, which is charged and discharged with a 100µA current source. The change in voltage on the capacitor is 2.5V. This same capacitor is also used to set the PGOOD rise delay. When PGOOD is low, the internal PGOOD circuitry uses the capacitor and when PGOOD is high the voltage margining circuit uses the capacitor. The slew time for voltage margining can be in the range of 300µs to 2.5ms. The CDEL capacitor on the evaluation board is 0.1µF leading to a voltage margining slew rate of 2.5ms.

Figure 8 shows positive and negative voltage margining with a CDEL capacitor of 0.1µF.

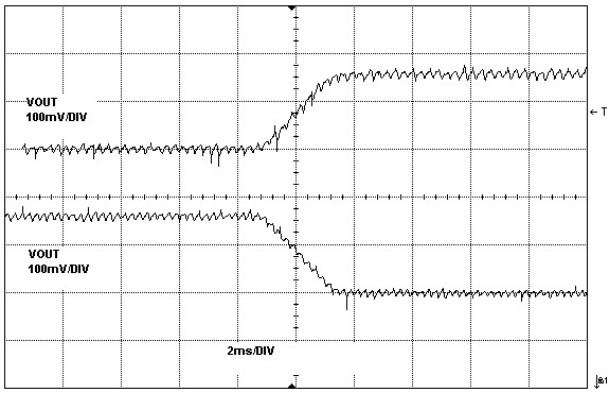


FIGURE 10. VOLTAGE MARGINING SLEW TIME

Conclusion

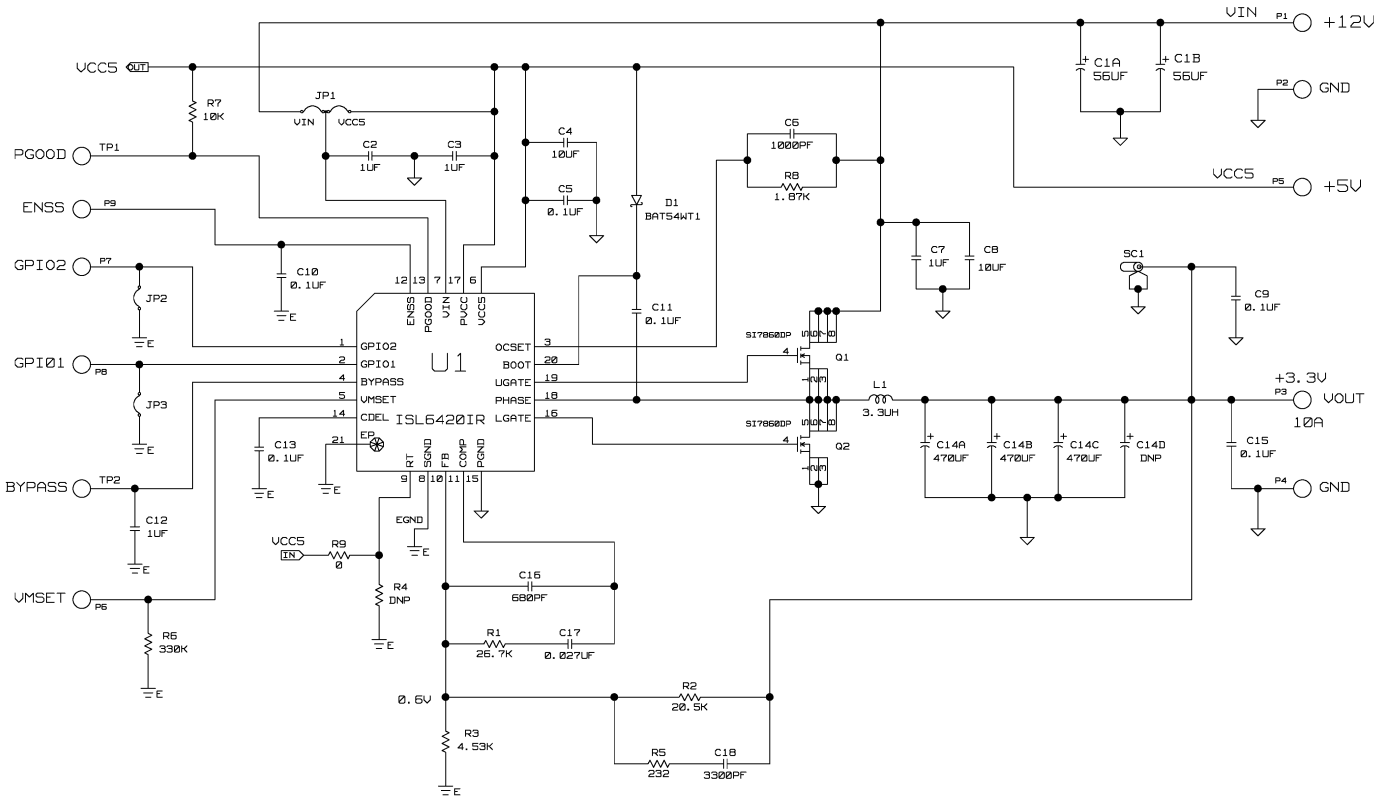
The ISL6420 is a versatile PWM controller. The small footprint and the numerous features enables the implementation of compact and highly efficient regulators, delivering low voltage power solutions.

References

For Intersil documents available on the web, see http://www.intersil.com/

[1] *ISL6420 Data Sheet,* Intersil Corporation, File No. FN9073.

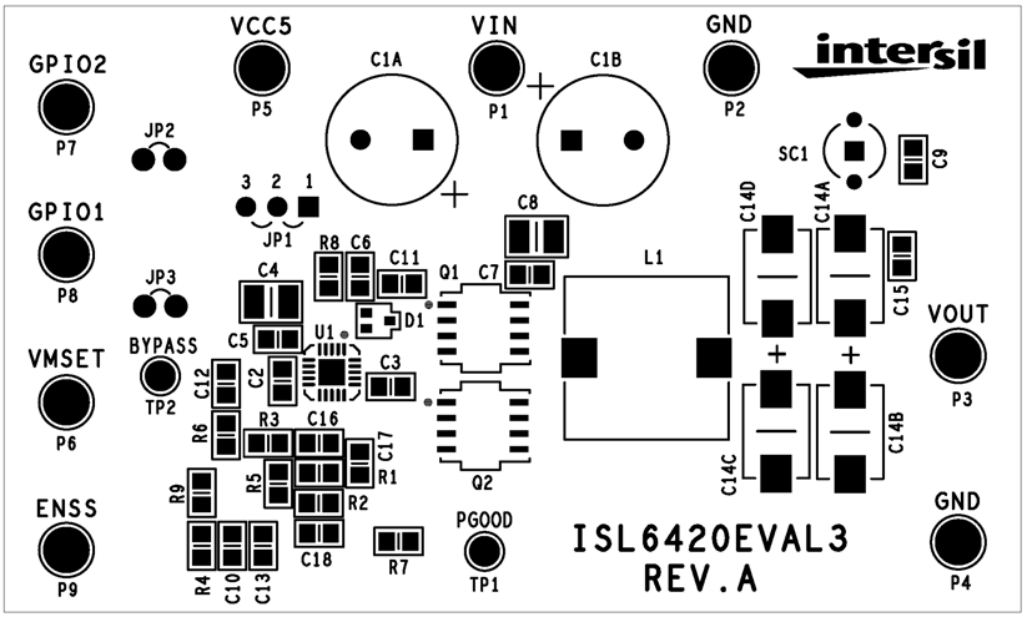
ISL6420EVAL Schematic



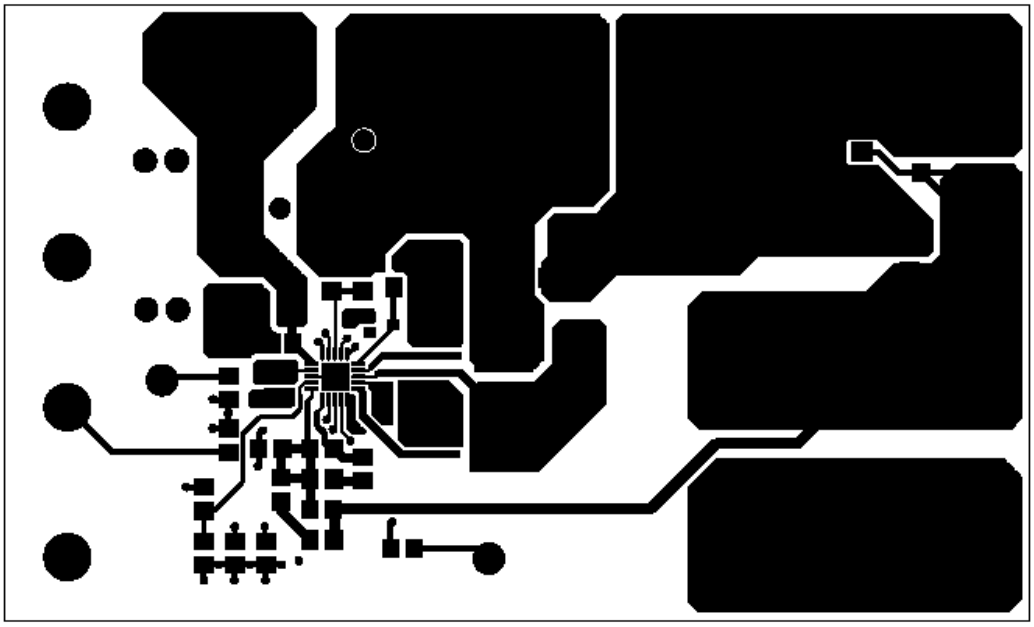
ISL6420EVAL Bill of Materials

REFERENCE	QTY	PART NUMBER	PART TYPE	DESCRIPTION	PACKAGE	VENDOR
U1	1	ISL6420IR	IC, Linear	IC, Single PWM Controller	20 Ld QFN	Intersil
Q1, Q2	2	SI7860DP	MOSFET, Single	N-channel, 30V, 15A, 0.011Ω	PowerPAK SO-8	Vishay Siliconix
D1	1	BAT54WT1	Diode, Schottky	30V, 200mA	SOT-323	On Semi
L1	1	IHLP-5050CE-RZ-3R3M	Inductor	3.3µH, 20%, 27A	SMD	Vishay
CAPACITORS						
C1A, C1B	2	25SP56M	Capacitor, Alu. Elec.	56µF, 20%, 25V, 0.025Ω	10 X 11.5	SANYO
C2, C3, C7, C12	4	08053D105KAT2A	Capacitor, Ceramic, X5R	1.0µF, 10%, 25V	SM_0805	AVX/Generic
C4, C8	2	12103D106MAT2A	Capacitor, Ceramic, X5R	10µF, 20%, 25V	SM_1210	AVX/Generic
C5, C9, C10, C11, C13, C15	6	08053C104KAT2	Capacitor, Ceramic, X7R	0.1µF, 10%, 25V	SM_0805	AVX/Generic
C6	1	08053C102KAT2	Capacitor, Ceramic, X7R	1000pF, 10%, 25V	SM_0805	AVX/Generic
C14A, C14B, C14C	3	6TPB470M	Capacitor, POSCAP	470µF, 20%, 6.3V, 0.035Ω	Case D4	SANYO
C14D - (DNP)	1		Capacitor, POSCAP		Case D3L/D4	SANYO
C16	1	0805YC681KAT2	Capacitor, Ceramic, X7R	680pF, 10%, 16V	SM_0805	AVX/Generic
C17	1	0805YC273KAT2	Capacitor, Ceramic, X7R	0.027µF, 10%, 16V	SM_0805	AVX/Generic
C18	1	0805YC332KAT2	Capacitor, Ceramic, X7R	3300pF, 10%, 16V	SM_0805	AVX/Generic
RESISTORS						
R1	1		Resistor, Film	26.7kΩ, 1%, 1/10 Watt	SM_0805	Panasonic/Generic
R2	1		Resistor, Film	20.5kΩ, 1%, 1/10 Watt	SM_0805	Panasonic/Generic
R3	1		Resistor, Film	4.53kΩ, 1%, 1/10 Watt	SM_0805	Panasonic/Generic
R4 - (DNP)	1		Resistor, Film		SM_0805	Panasonic/Generic
R5	1		Resistor, Film	232Ω, 1%, 1/10 Watt	SM_0805	Panasonic/Generic
R6	1		Resistor, Film	330kΩ, 1%, 1/10 Watt	SM_0805	Panasonic/Generic
R7	1		Resistor, Film	10kΩ,1%,1/10 Watt	SM_0805	Panasonic/Generic
R8	1		Resistor, Film	1.87kΩ, 1%, 1/10 Watt	SM_0805	Panasonic/Generic
R9	1		Resistor, Film	0 Ohm, 1%, 1/10 Watt	SM_0805	Panasonic/Generic
OTHERS						
SC1	1	129-0701-202	Terminal, Scope Probe	Terminal, Scope Probe		Johnson Components
P1 - P9	9	1514-2	Turrett Post	Terminal post, through hole, 1/4 inch	PTH	Keystone
TP1, TP2	2	5002	TEST POINT vertical, white	PC test jack	PTH	Keystone
JP1	1	68000-236-1X3	Header	1X3 Break Strip GOLD		
JP2, JP3	2	68000-236-1X2	Header	1X2 Break Strip GOLD		
JP1, JP2, JP3	3	S9001-ND	Jumper	2 pin jumper		Digikey

ISL6420EVAL3 Printed Circuit Board Layers

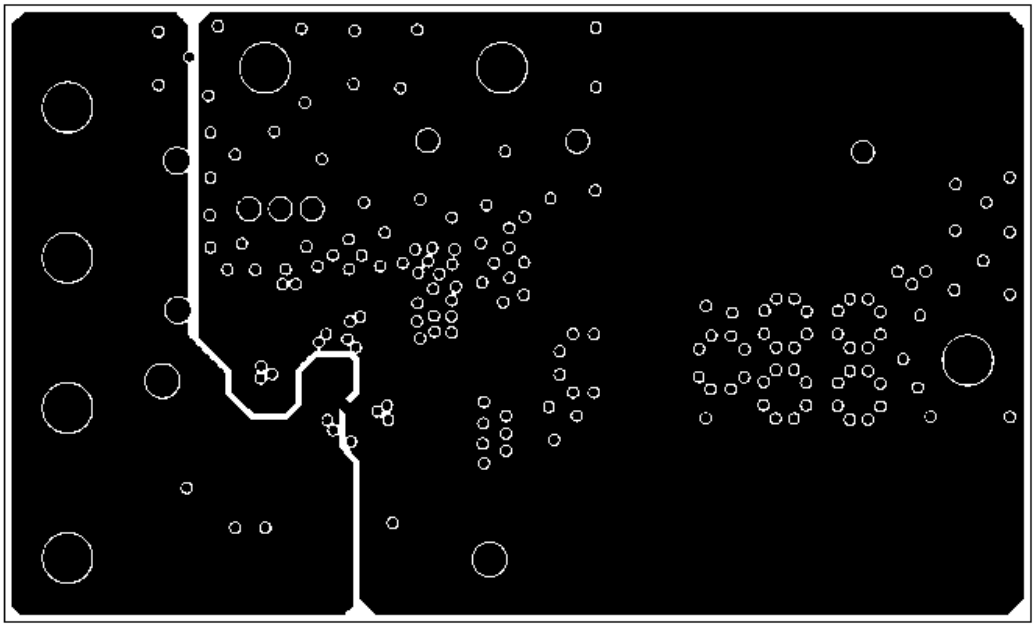


ISL6420EVAL3 - Top Layer (Silkscreen)

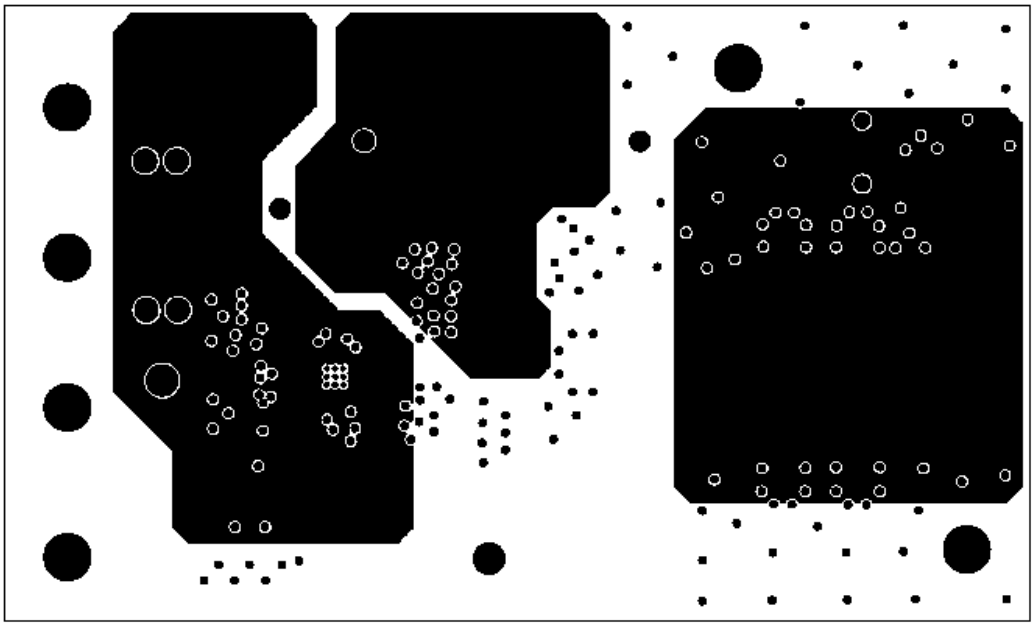


ISL6420EVAL3 - Layer 2

ISL6420EVAL3 Printed Circuit Board Layers (Continued)

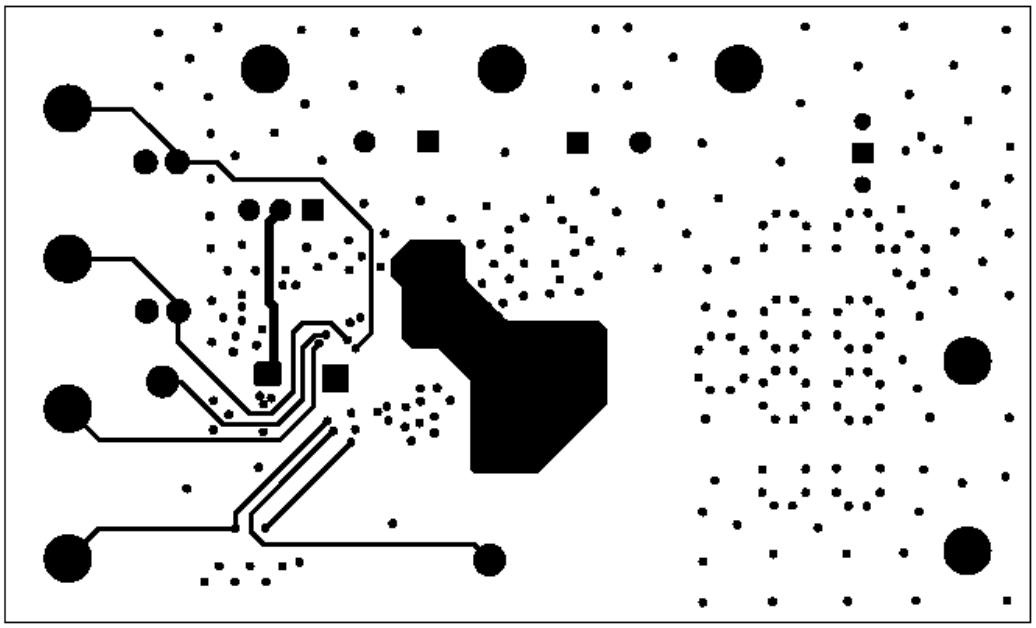


ISL6420EVAL3 - Layer 3

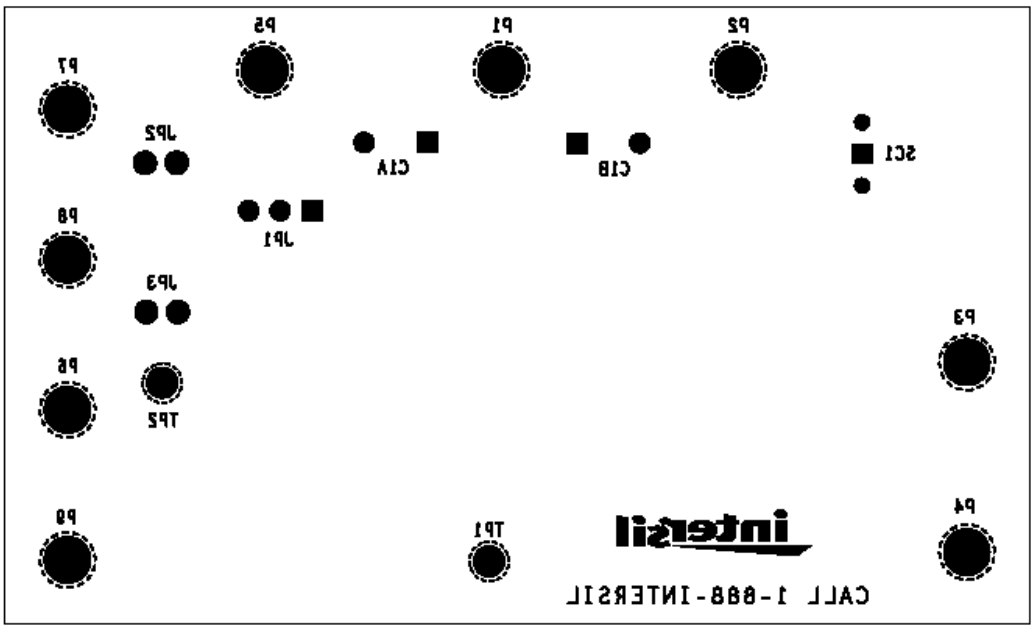


ISL6420EVAL3 - Layer 4

ISL6420EVAL3 Printed Circuit Board Layers (Continued)



ISL6420EVAL3 - Layer 5



ISL6420EVAL3 - Bottom Layer (Silkscreen)