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## LM5109A High Voltage 1A Peak Half Bridge Gate Driver

### 1 Features

- Drives Both a High-Side and Low-Side N-Channel MOSFET
- 1A peak Output Current (1.0A Sink / 1.0A Source)
- Independent TTL Compatible Inputs
- Bootstrap Supply Voltage to 108V DC
- Fast Propagation Times (30 ns Typical)
- Drives 1000 pF Load with 15ns Rise and Fall Times
- Excellent Propagation Delay Matching (2 ns Typical)
- Supply Rail Under-Voltage Lockout
- Low Power Consumption
- Pin Compatible with ISL6700
- Packages:
  - SOIC
  - WSON-8 (4 mm x 4 mm)

### 2 Applications

- Current Fed Push-Pull Converters
- Half and Full Bridge Power Converters
- Solid State Motor Drives
- Two Switch Forward Power Converters

### 3 Description

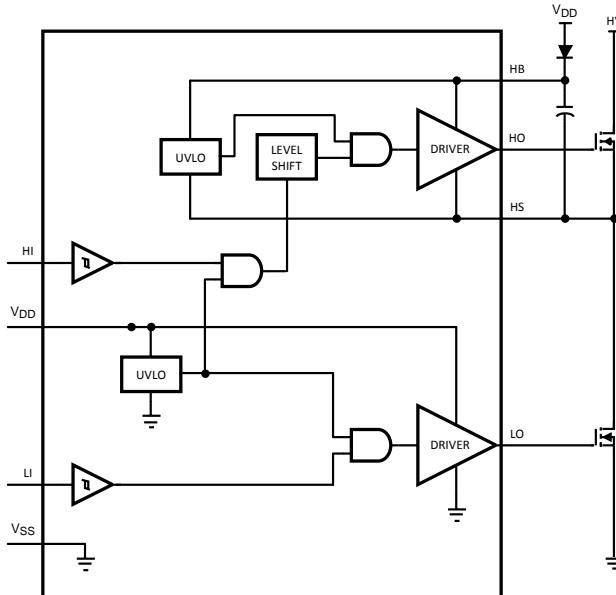
The LM5109A is a cost effective, high voltage gate driver designed to drive both the high-side and the low-side N-Channel MOSFETs in a synchronous buck or a half bridge configuration. The floating high-side driver is capable of working with rail voltages up to 90V. The outputs are independently controlled with TTL compatible input thresholds. The robust level shift technology operates at high speed while consuming low power and providing clean level transitions from the control input logic to the high-side gate driver. Under-voltage lockout is provided on both the low-side and the high-side power rails. The device is available in the SOIC and the thermally enhanced WSON packages.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM5109A	SOIC (8)	4.90 mm x 3.91 mm
	WSON (8)	4.00 mm x 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

#### Simplified Block Diagram



An **IMPORTANT NOTICE** at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. **PRODUCTION DATA**.

**LM5109A**

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[www.ti.com](http://www.ti.com)**Table of Contents**

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**4 Revision History**

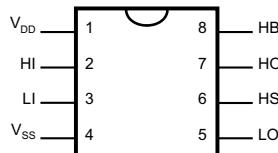
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision A (March 2013) to Revision B</b>	<b>Page</b>
• Added <i>Device Information</i> table, <i>ESD Ratings</i> , <i>Pin Configuration and Functions</i> section, <i>Detailed Description</i> section, <i>Application and Implementation</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section.	1

<b>Changes from Original (March 2013) to Revision A</b>	<b>Page</b>
• Changed layout of National Data Sheet to TI format	9

## 5 Pin Configuration and Functions

**D and NGT Packages**  
**8-Pin SOIC, WSON**  
**Top View**



### Pin Functions

Pin #		NAME	DESCRIPTION	APPLICATION INFORMATION
SOIC	WSON <sup>(1)</sup>			
1	1	V <sub>DD</sub>	Positive gate drive supply	Locally decouple to V <sub>SS</sub> using low ESR/ESL capacitor located as close to IC as possible.
2	2	HI	High side control input	The HI input is compatible with TTL input thresholds. Unused HI input should be tied to ground and not left open
3	3	LI	Low side control input	The LI input is compatible with TTL input thresholds. Unused LI input should be tied to ground and not left open.
4	4	V <sub>SS</sub>	Ground reference	All signals are referenced to this ground.
5	5	LO	Low side gate driver output	Connect to the gate of the low-side N- MOS device.
6	6	HS	High side source connection	Connect to the negative terminal of the bootstrap capacitor and to the source of the high-side N-MOS device.
7	7	HO	High side gate driver output	Connect to the gate of the high-side N-MOS device.
8	8	HB	High side gate driver positive supply rail	Connect the positive terminal of the bootstrap capacitor to HB and the negative terminal of the bootstrap capacitor to HS. The bootstrap capacitor should be placed as close to IC as possible.

(1) For WSON package it is recommended that the exposed pad on the bottom of the package be soldered to ground plane on the PCB and the ground plane should extend out from underneath the package to improve heat dissipation.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

See <sup>(1)(2)</sup>

V <sub>DD</sub> to V <sub>SS</sub>	-0.3V to 18V
HB to HS	-0.3V to 18V
LI or HI to V <sub>SS</sub>	-0.3V to V <sub>DD</sub> + 0.3V
LO to V <sub>SS</sub>	-0.3V to V <sub>DD</sub> + 0.3V
HO to V <sub>SS</sub>	V <sub>HS</sub> - 0.3V to V <sub>HB</sub> + 0.3V
HS to V <sub>SS</sub> <sup>(3)</sup>	-5V to 90V
HB to V <sub>SS</sub>	108V
Junction Temperature	-40°C to 150°C
Storage Temperature Range	-55°C to 150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is specified. Operating Ratings do not imply performance limits. For performance limits and associated test conditions, see the [Electrical Characteristics](#).

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

(3) In the application the HS node is clamped by the body diode of the external lower N-MOSFET, therefore the HS voltage will generally not exceed -1V. However in some applications, board resistance and inductance may result in the HS node exceeding this stated voltage transiently. If negative transients occur on HS, the HS voltage must never be more negative than V<sub>DD</sub> - 15V. For example, if V<sub>DD</sub> = 10V, the negative transients at HS must not exceed -5V.

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## 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge Human-body model (HBM) <sup>(1)</sup>	±1500	V

(1) The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin.

## 6.3 Recommended Operating Conditions

V <sub>DD</sub>		8V to 14V
HS <sup>(1)</sup>		–1V to 90V
HB		V <sub>HS</sub> + 8V to V <sub>HS</sub> + 14V
HS Slew Rate		< 50 V/ns
Junction Temperature		–40°C to 125°C

(1) In the application the HS node is clamped by the body diode of the external lower N-MOSFET, therefore the HS voltage will generally not exceed –1V. However in some applications, board resistance and inductance may result in the HS node exceeding this stated voltage transiently. If negative transients occur on HS, the HS voltage must never be more negative than V<sub>DD</sub> – 15V. For example, if V<sub>DD</sub> = 10V, the negative transients at HS must not exceed –5V.

## 6.4 Electrical Characteristics

Specifications in standard typeface are for T<sub>J</sub> = 25°C, and those in **boldface** type apply over the full **operating junction temperature range**. Unless otherwise specified, V<sub>DD</sub> = V<sub>HB</sub> = 12V, V<sub>SS</sub> = V<sub>HS</sub> = 0V, No Load on LO or HO<sup>(1)</sup>.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
<b>Supply Currents</b>						
I <sub>DD</sub>	V <sub>DD</sub> quiescent current	LI = HI = 0V		0.3	<b>0.6</b>	mA
I <sub>DDO</sub>	V <sub>DD</sub> operating current	f = 500 kHz		1.8	<b>2.9</b>	mA
I <sub>HB</sub>	Total HB quiescent current	LI = HI = 0V		0.06	<b>0.2</b>	mA
I <sub>HBO</sub>	Total HB operating current	f = 500 kHz		1.4	<b>2.8</b>	mA
I <sub>HBS</sub>	HB to V <sub>SS</sub> current, quiescent	V <sub>HS</sub> = V <sub>HB</sub> = 90V		0.1	<b>10</b>	μA
I <sub>HBSO</sub>	HB to V <sub>SS</sub> current, operating	f = 500 kHz		0.5		mA
<b>Input Pins LI and HI</b>						
V <sub>IL</sub>	Low-level input voltage threshold		<b>0.8</b>	1.8		V
V <sub>IH</sub>	High-level input voltage threshold			1.8	<b>2.2</b>	V
R <sub>I</sub>	Input pulldown resistance		<b>100</b>	200	<b>500</b>	kΩ
<b>Under-Voltage Protection</b>						
V <sub>DDR</sub>	V <sub>DD</sub> rising threshold	V <sub>DDR</sub> = V <sub>DD</sub> – V <sub>SS</sub>	<b>6.0</b>	6.7	<b>7.4</b>	V
V <sub>DDH</sub>	V <sub>DD</sub> threshold hysteresis			0.5		V
V <sub>HBR</sub>	HB rising threshold	V <sub>HBR</sub> = V <sub>HB</sub> – V <sub>HS</sub>	<b>5.7</b>	6.6	<b>7.1</b>	V
V <sub>HBH</sub>	HB threshold hysteresis			0.4		V
<b>LO Gate Driver</b>						
V <sub>OLL</sub>	Low-level output voltage	I <sub>LO</sub> = 100 mA, V <sub>OHL</sub> = V <sub>LO</sub> – V <sub>SS</sub>		0.38	<b>0.65</b>	V
V <sub>OHL</sub>	High-level output voltage	I <sub>LO</sub> = –100 mA, V <sub>OHL</sub> = V <sub>DD</sub> – V <sub>LO</sub>		0.72	<b>1.20</b>	V
I <sub>OHL</sub>	Peak pullup current	V <sub>LO</sub> = 0V		1.0		A
I <sub>OLL</sub>	Peak pulldown current	V <sub>LO</sub> = 12V		1.0		A
<b>HO Gate Driver</b>						
V <sub>OLH</sub>	Low-level output voltage	I <sub>HO</sub> = 100 mA, V <sub>OLH</sub> = V <sub>HO</sub> – V <sub>HS</sub>		0.38	<b>0.65</b>	V
V <sub>OHH</sub>	High-level output voltage	I <sub>HO</sub> = –100 mA, V <sub>OHH</sub> = V <sub>HB</sub> – V <sub>HO</sub>		0.72	<b>1.20</b>	V
I <sub>OHH</sub>	Peak pullup current	V <sub>HO</sub> = 0V		1.0		A
I <sub>OLH</sub>	Peak pulldown current	V <sub>HO</sub> = 12V		1.0		A
<b>Thermal Resistance</b>						

(1) Minimum and maximum limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).

## Electrical Characteristics (continued)

Specifications in standard typeface are for  $T_J = 25^\circ\text{C}$ , and those in **boldface type** apply over the full **operating junction temperature range**. Unless otherwise specified,  $V_{DD} = V_{HB} = 12\text{V}$ ,  $V_{SS} = V_{HS} = 0\text{V}$ , No Load on LO or HO<sup>(1)</sup>.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$\theta_{JA}$	Junction to ambient	SOIC <sup>(2)(3)</sup>		160		$^\circ\text{C/W}$
		WSON <sup>(2)(3)</sup>		40		

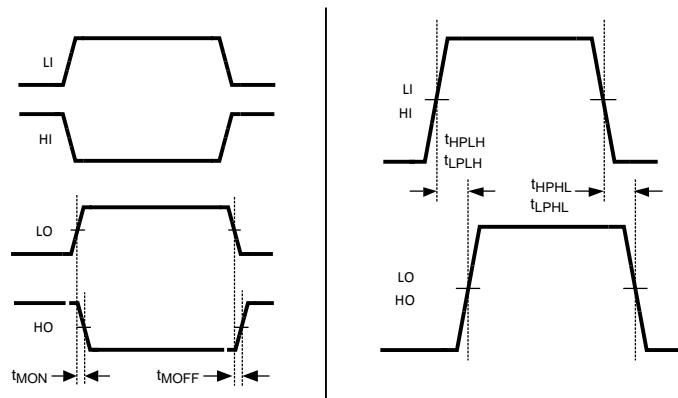
(2) 4-layer board with Cu finished thicknesses 1.5/1.1/1.5 oz. Maximum die size used. 5x body length of Cu trace on PCB top. 50 x 50mm ground and power planes embedded in PCB. See Application Note AN-1187.

(3) The  $\theta_{JA}$  is not a constant for the package and depends on the printed circuit board design and the operating conditions.

## 6.5 Switching Characteristics

Specifications in standard typeface are for  $T_J = 25^\circ\text{C}$ , and those in **boldface type** apply over the full **operating junction temperature range**. Unless otherwise specified,  $V_{DD} = V_{HB} = 12\text{V}$ ,  $V_{SS} = V_{HS} = 0\text{V}$ , No Load on LO or HO.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
<b>LM5109A</b>						
$t_{LPHL}$	Lower turn-off propagation delay (LI falling to LO falling)			30	<b>56</b>	ns
$t_{HPLH}$	Upper turn-off propagation delay (HI falling to HO falling)			30	<b>56</b>	ns
$t_{LPLH}$	Lower turn-on propagation delay (LI rising to LO rising)			32	<b>56</b>	ns
$t_{HPLH}$	Upper turn-on propagation delay (HI rising to HO rising)			32	<b>56</b>	ns
$t_{MON}$	Delay matching: lower turn-on and upper turn-off			2	<b>15</b>	ns
$t_{MOFF}$	Delay matching: lower turn-off and upper turn-on			2	<b>15</b>	ns
$t_{RC}, t_{FC}$	Either output rise or fall time	$C_L = 1000 \text{ pF}$		15	-	ns
$t_{PW}$	Minimum input pulse width that changes the output			50		ns



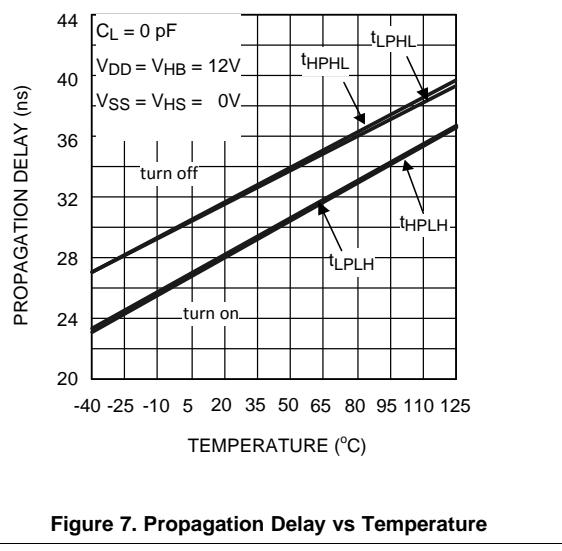
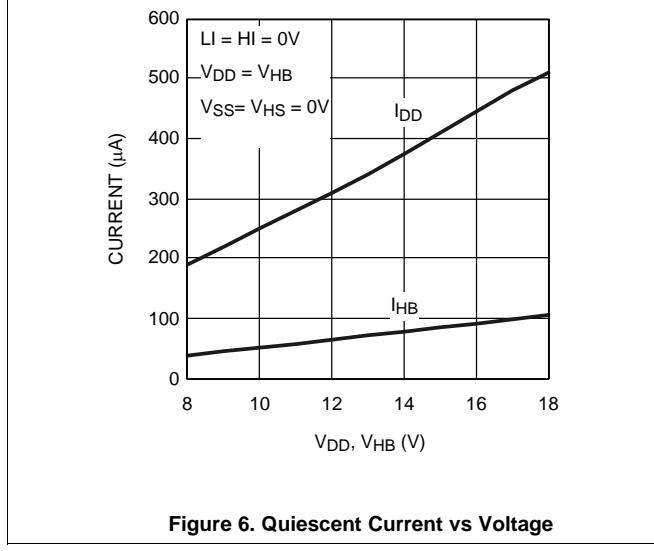
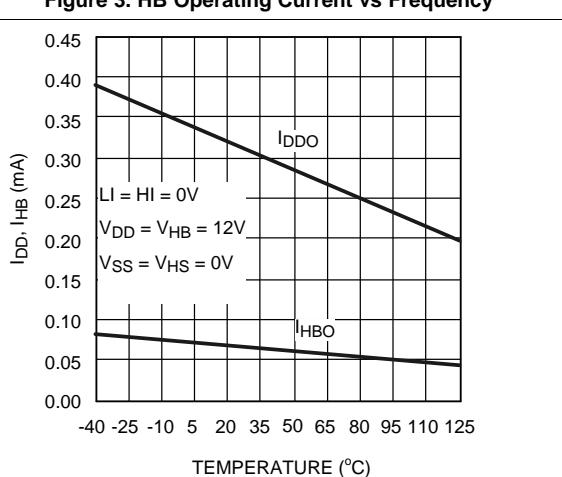
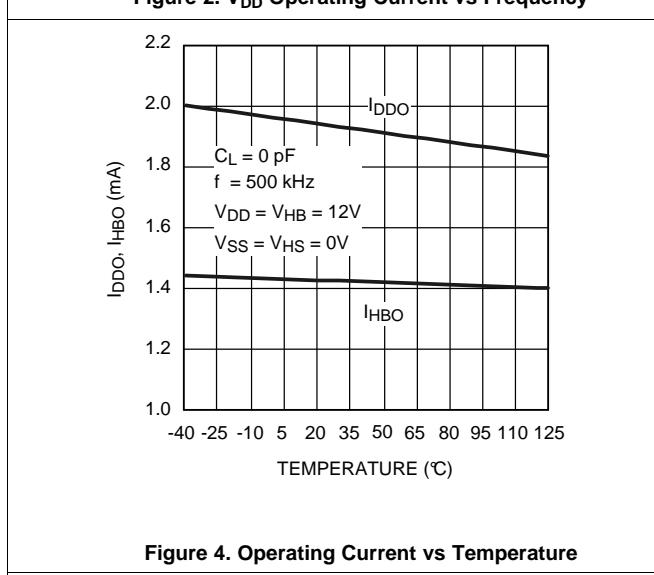
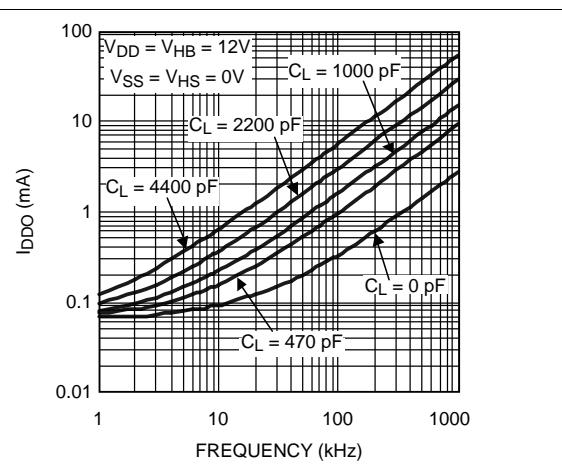
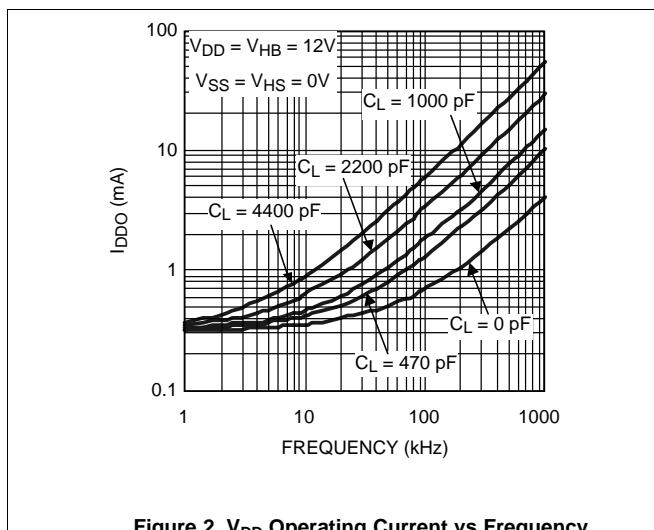
**Figure 1. Timing Diagram**

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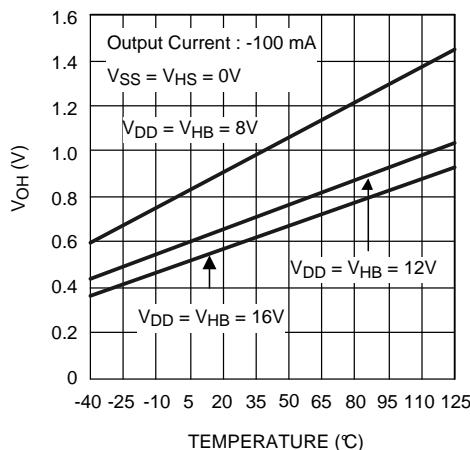
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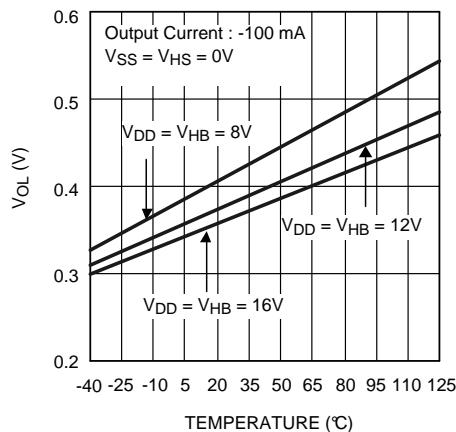
### 6.6 Typical Performance Characteristics



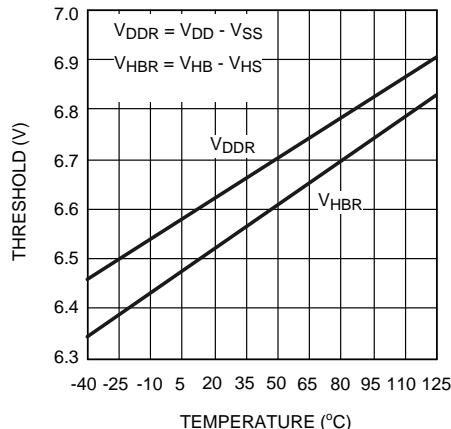
### Typical Performance Characteristics (continued)



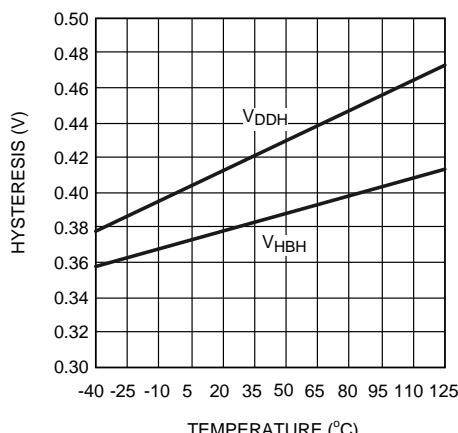
**Figure 8. LO and HO High Level Output Voltage vs Temperature**



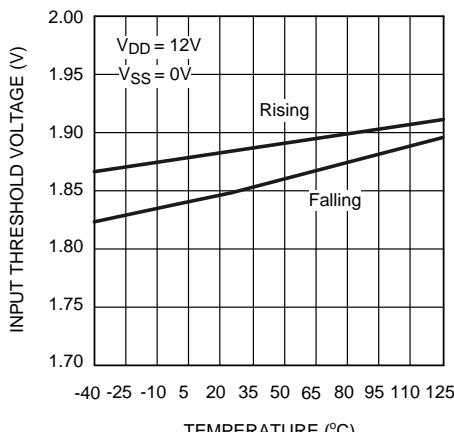
**Figure 9. LO and HO Low Level Output Voltage vs Temperature**



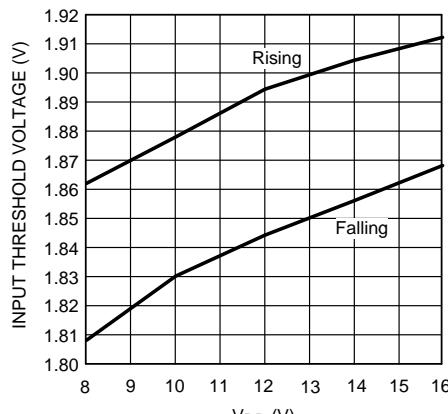
**Figure 10. Undervoltage Rising Thresholds vs Temperature**



**Figure 11. Undervoltage Hysteresis vs Temperature**



**Figure 12. Input Thresholds vs Temperature**



**Figure 13. Input Thresholds vs Supply Voltage**

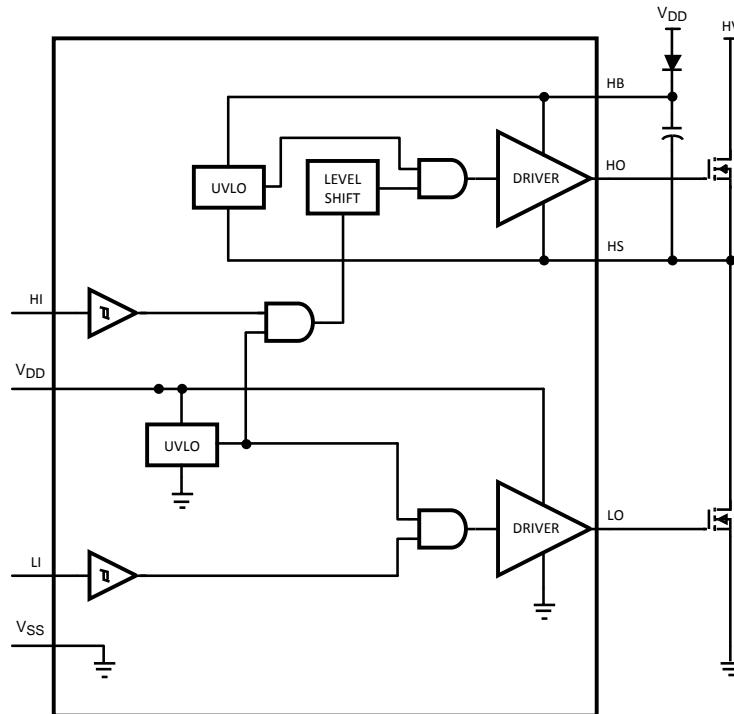
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## 7 Detailed Description

### 7.1 Functional Block Diagram



## 8 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

#### 8.1.1 HS Transient Voltages Below Ground

The HS node will always be clamped by the body diode of the lower external FET. In some situations, board resistances and inductances can cause the HS node to transiently swing several volts below ground. The HS node can swing below ground provided:

1. HS must always be at a lower potential than HO. Pulling HO more than  $-0.3V$  below HS can activate parasitic transistors resulting in excessive current flow from the HB supply, possibly resulting in damage to the IC. The same relationship is true with LO and VSS. If necessary, a Schottky diode can be placed externally between HO and HS or LO and GND to protect the IC from this type of transient. The diode must be placed as close to the IC pins as possible in order to be effective.
2. HB to HS operating voltage should be 15V or less. Hence, if the HS pin transient voltage is  $-5V$ , VDD should be ideally limited to 10V to keep HB to HS below 15V.
3. Low ESR bypass capacitors from HB to HS and from VDD to VSS are essential for proper operation. The capacitor should be located at the leads of the IC to minimize series inductance. The peak currents from LO and HO can be quite large. Any series inductances with the bypass capacitor will cause voltage ringing at the leads of the IC which must be avoided for reliable operation.

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[www.ti.com](http://www.ti.com)**9 Layout****9.1 Layout Guidelines**

Optimum performance of high and low-side gate drivers cannot be achieved without taking due considerations during circuit board layout. The following points are emphasized:

1. Low ESR / ESL capacitors must be connected close to the IC between VDD and VSS pins and between HB and HS pins to support high peak currents being drawn from VDD and HB during the turn-on of the external MOSFETs.
2. To prevent large voltage transients at the drain of the top MOSFET, a low ESR electrolytic capacitor and a good quality ceramic capacitor must be connected between the MOSFET drain and ground (VSS).
3. In order to avoid large negative transients on the switch node (HS) pin, the parasitic inductances between the top MOSFET source and the of the bottom MOSFET drain (synchronous rectifier) must be minimized.
4. Grounding considerations:
  - The first priority in designing grounding connections is to confine the high peak currents that charge and discharge the MOSFET gates to a minimal physical area. This will decrease the loop inductance and minimize noise issues on the gate terminals of the MOSFETs. The gate driver should be placed as close as possible to the MOSFETs.
  - The second consideration is the high current path that includes the bootstrap capacitor, the bootstrap diode, the local ground referenced bypass capacitor, and the low-side MOSFET body diode. The bootstrap capacitor is recharged on a cycle-by-cycle basis through the bootstrap diode from the ground referenced VDD bypass capacitor. The recharging occurs in a short time interval and involves high peak current. Minimizing this loop length and area on the circuit board is important to ensure reliable operation.

## 10 Device and Documentation Support

### 10.1 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 10.2 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

### 10.3 Electrostatic Discharge Caution

 These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 10.4 Glossary

**SLYZ022 — TI Glossary.**

This glossary lists and explains terms, acronyms, and definitions.

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5109AMA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L5109 AMA	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
LM5109AMAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L5109 AMA	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
LM5109ASD/NOPB	ACTIVE	WSON	NGT	8	1000	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-40 to 125	5109ASD	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
LM5109ASDX/NOPB	ACTIVE	WSON	NGT	8	4500	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-40 to 125	5109ASD	<span style="background-color: red; color: white; padding: 2px;">Samples</span>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

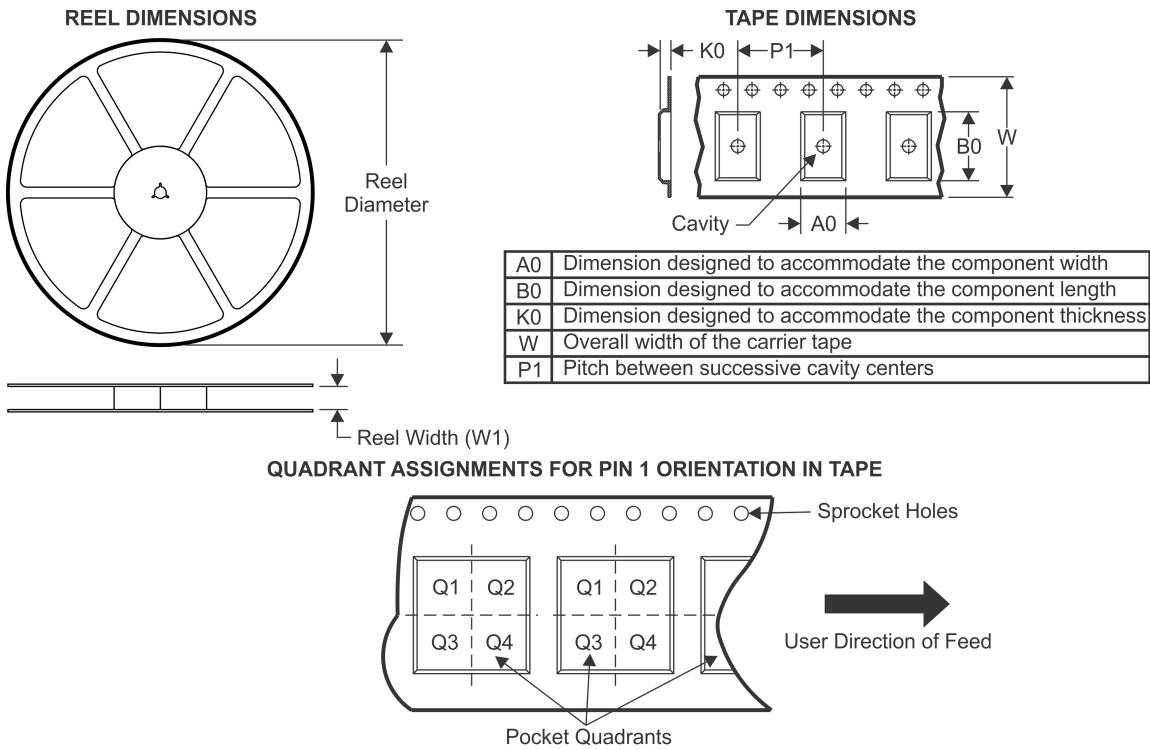
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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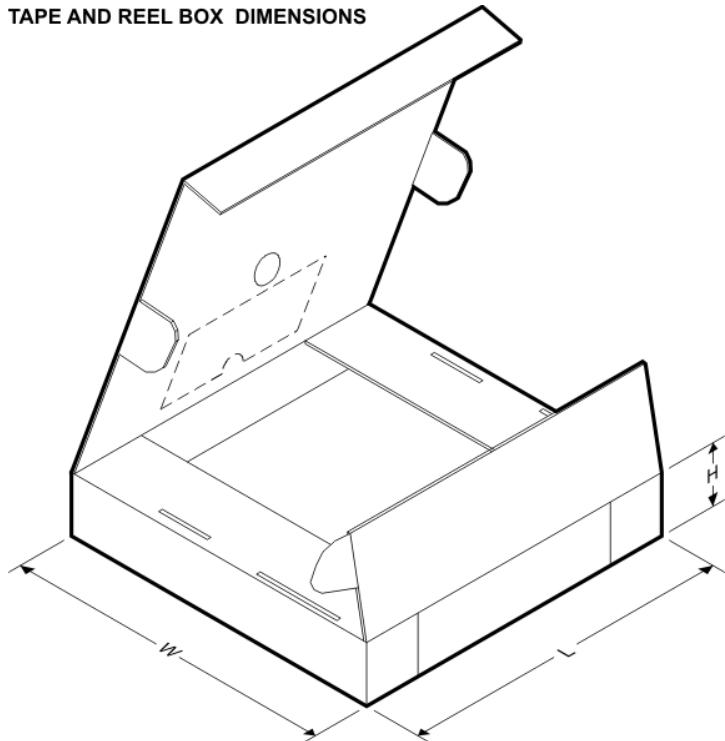
**TAPE AND REEL INFORMATION**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5109AMAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5109ASD/NOPB	WSON	NGT	8	1000	180.0	12.4	4.3	4.3	1.1	8.0	12.0	Q1
LM5109ASDX/NOPB	WSON	NGT	8	4500	330.0	12.4	4.3	4.3	1.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

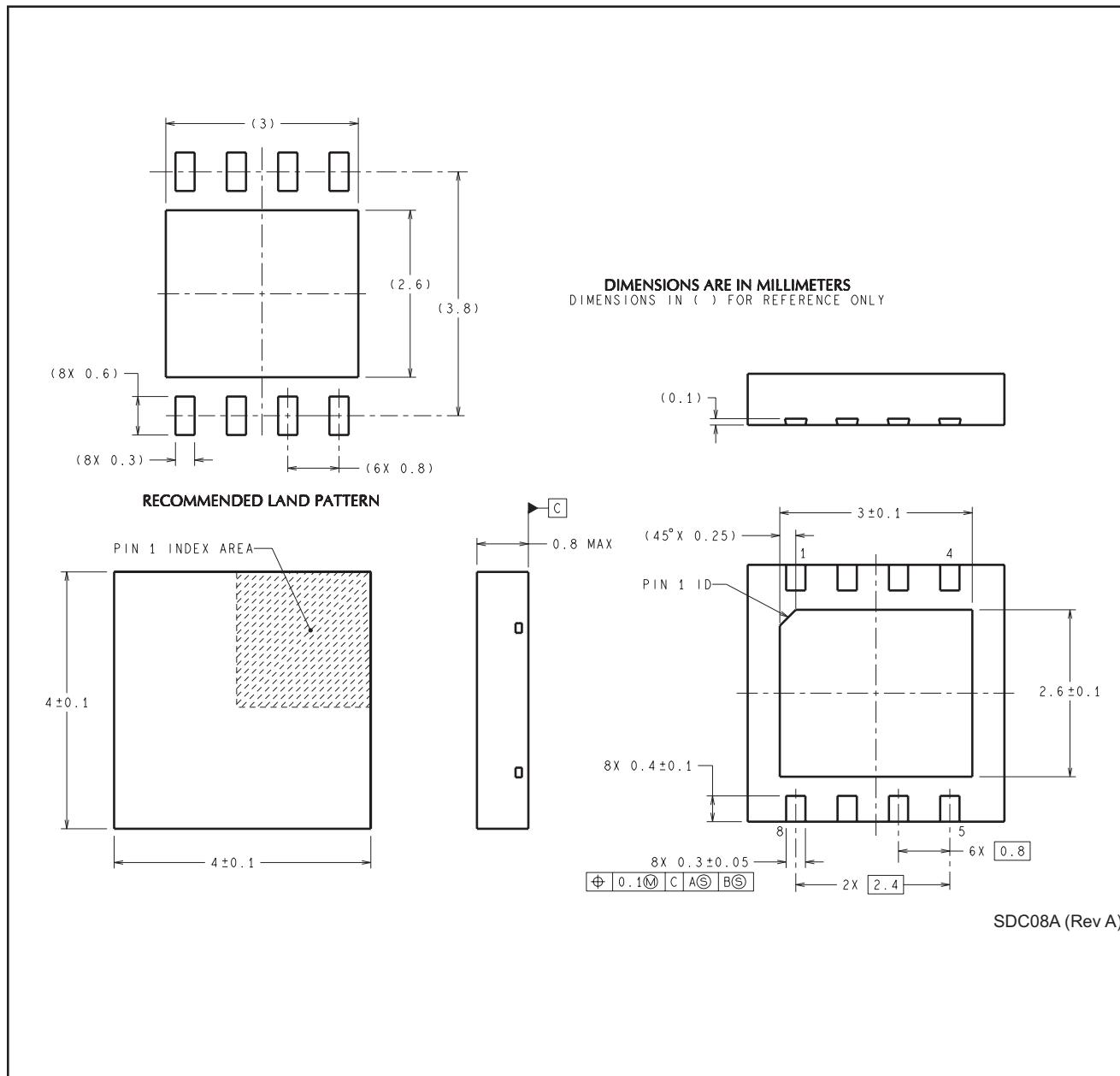


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5109AMAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM5109ASD/NOPB	WSON	NGT	8	1000	203.0	203.0	35.0
LM5109ASDX/NOPB	WSON	NGT	8	4500	346.0	346.0	35.0

## MECHANICAL DATA

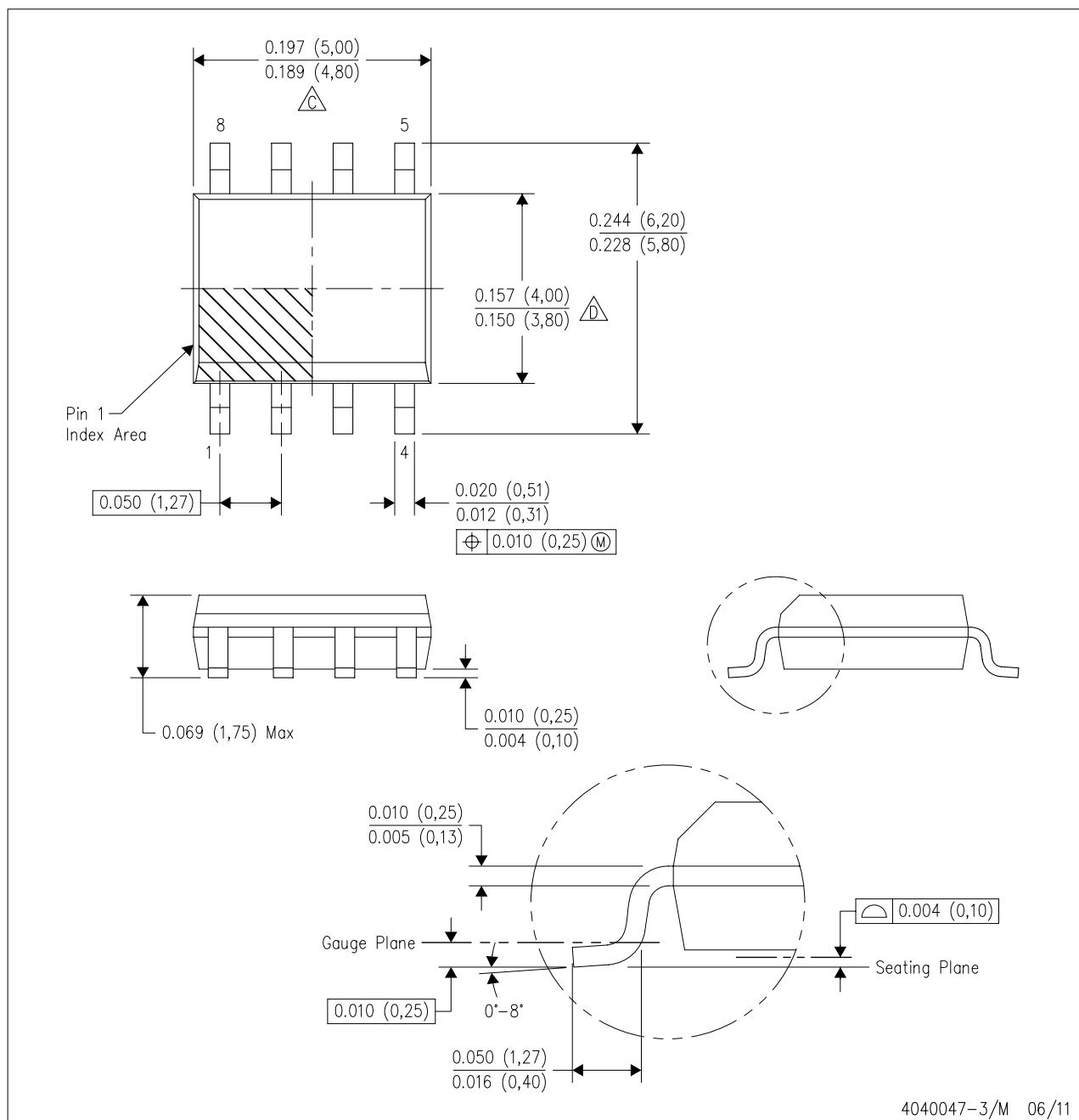
NGT0008A



## MECHANICAL DATA

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



4040047-3/M 06/11

NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.

C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.  
E. Reference JEDEC MS-012 variation AA.

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