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DSP Pro Development Board Stratix II 2S180 Edition Rev 01

Revision History		Rev
Date	Change Description	
8/18/05	Created schematic and changed the component from the 2S60 on the DSP board to the 2S180 on this Pro version of the board	01

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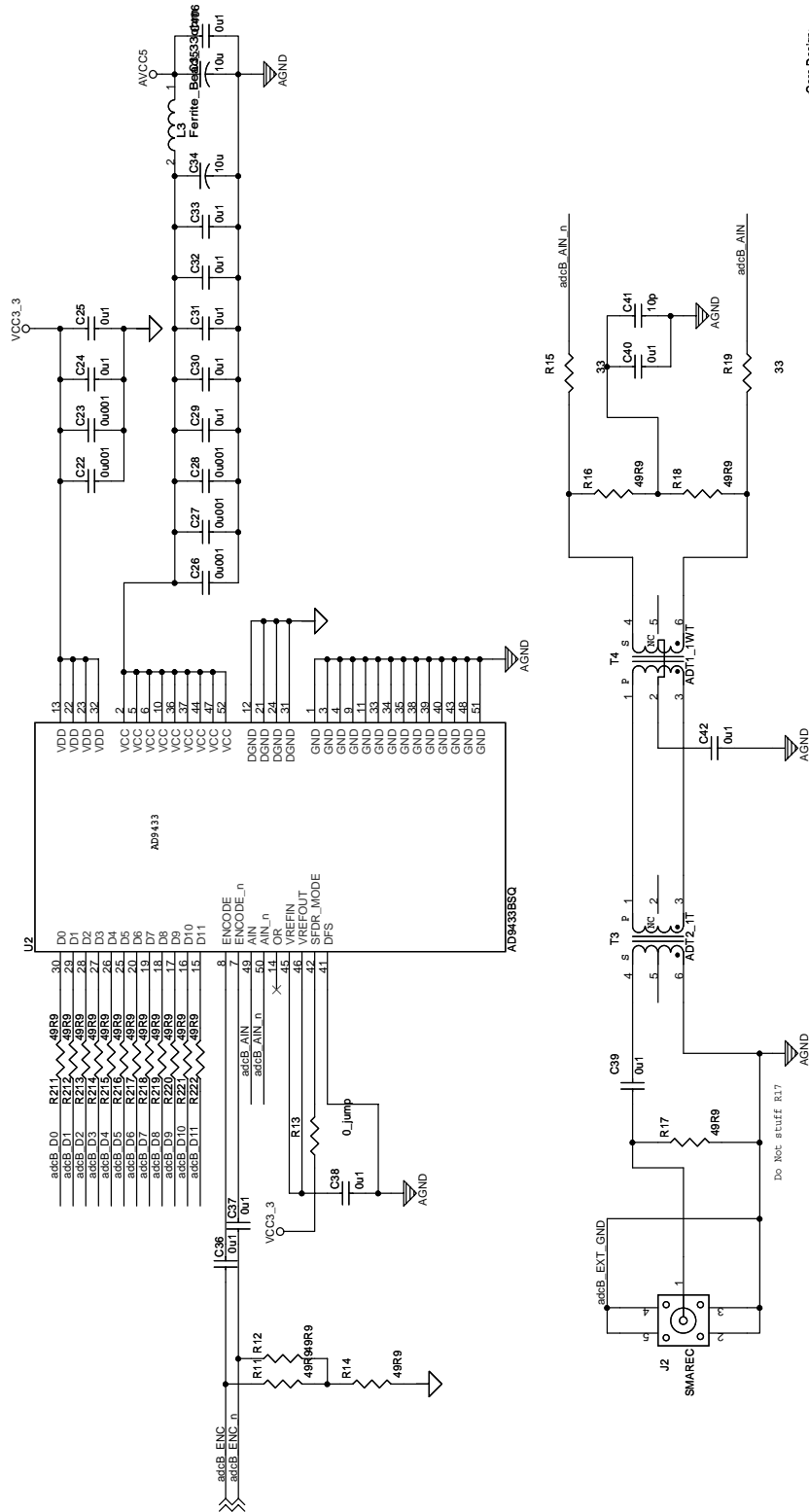
Title DSP Pro Stratix II 2S180 (Maine Pro)

Size	Document Number	Rev
A	P06-10217-01	01

Date: Thursday, August 18, 2005 Sheet 1 of 40

ADC B

adcB_D11:01



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File DSP Pro Streak II 2S180 (Maine Pro)

Size B

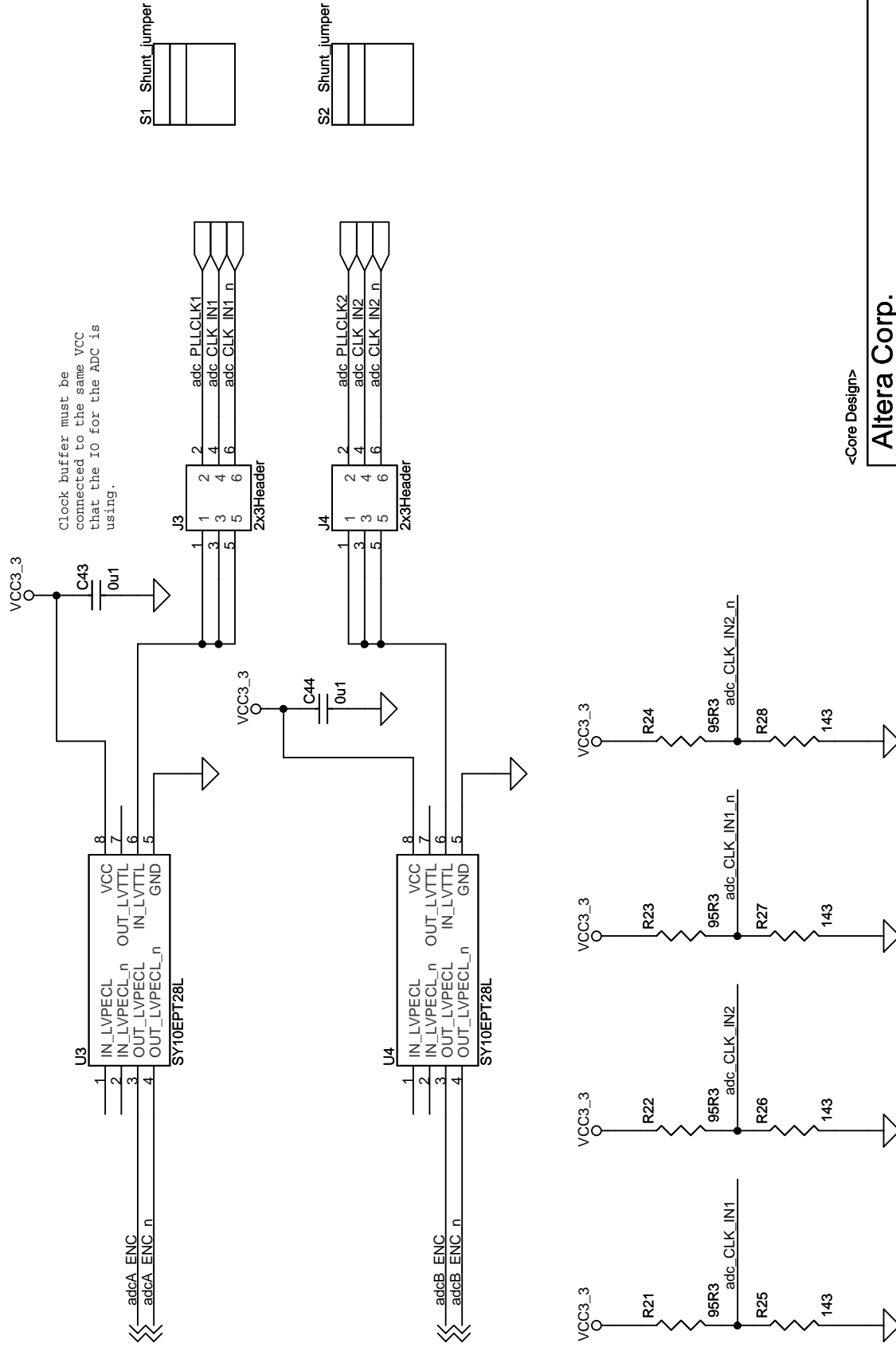
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Date: Thursday, August 18, 2005

Sheet 4 of 40

Rev 01

ADC Clock Selection



Clock buffer must be connected to the same VCC that the IO for the ADC is using.

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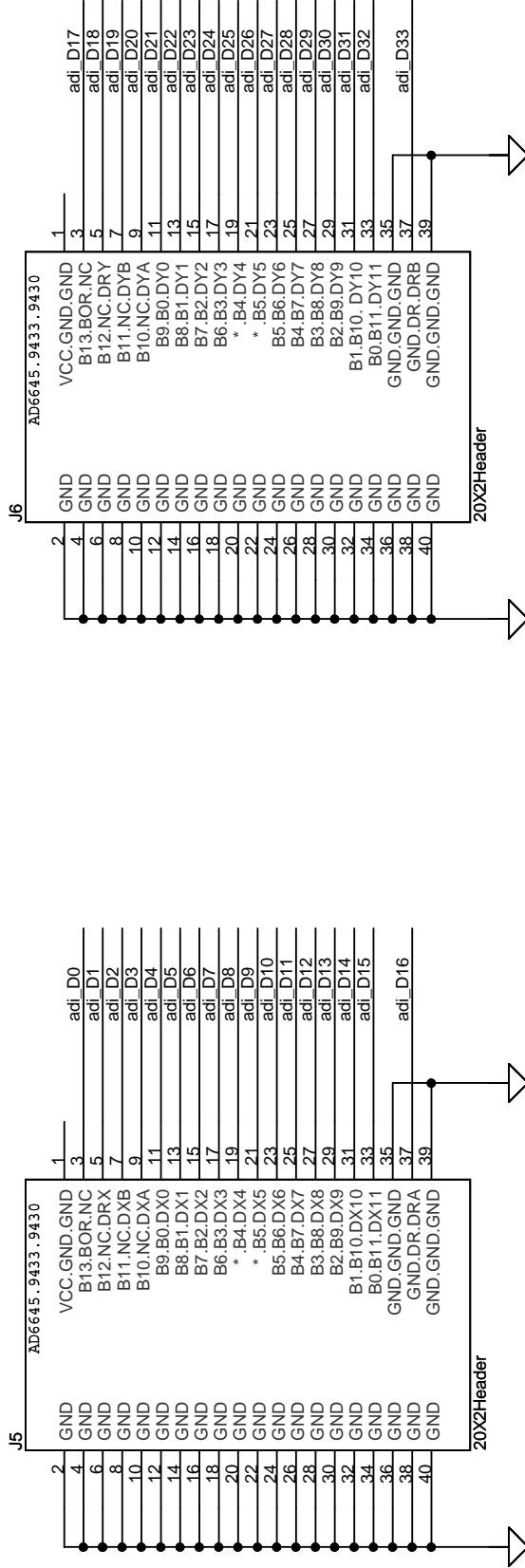
Size A Document Number P06-10217-01

Rev 01

Date: Thursday, August 18, 2005 Sheet 5 of 40

ADI Connector

adi_D183:01



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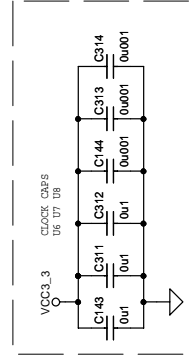
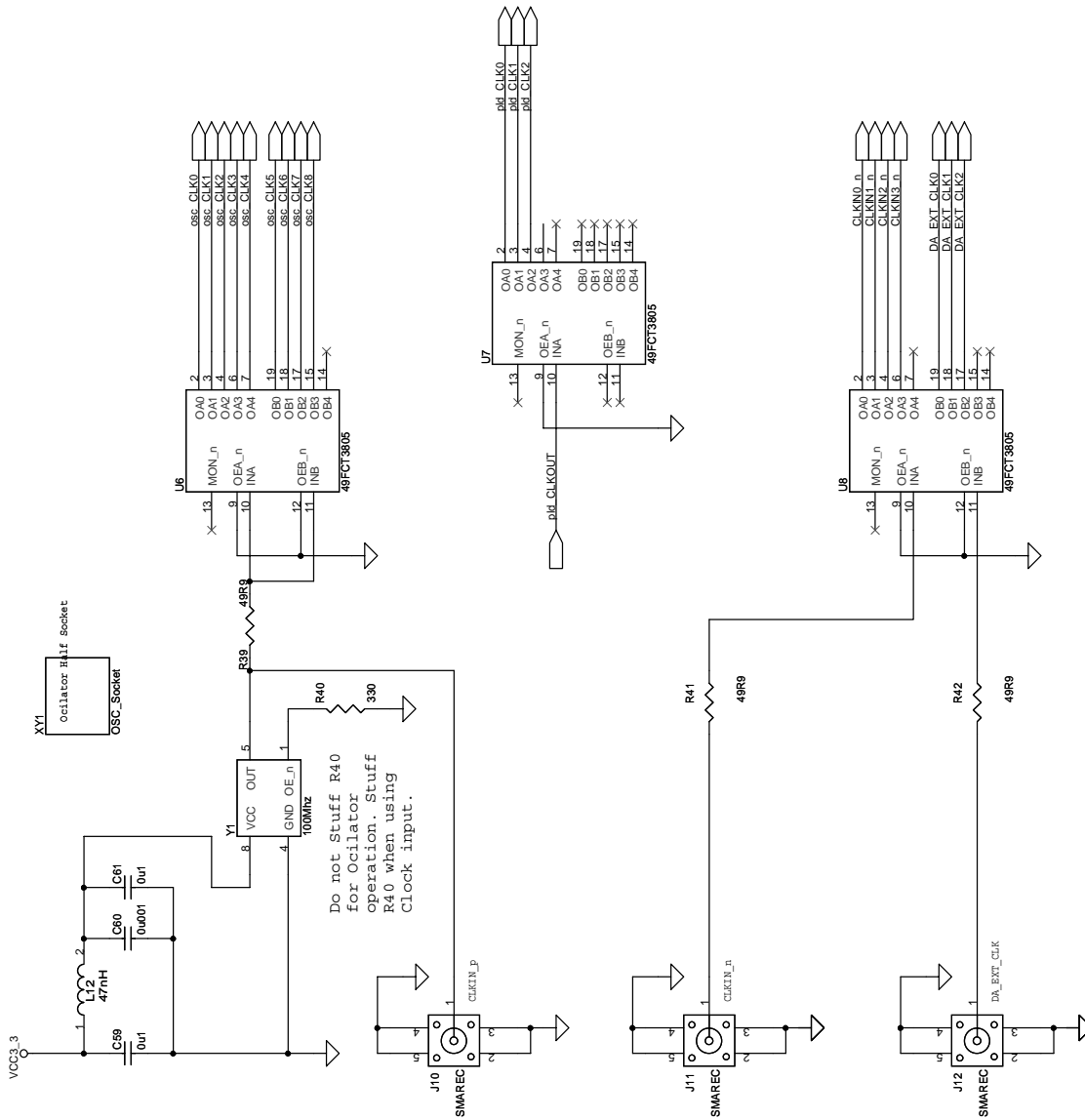
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Size A Document Number P06-10217-01

Rev 01

Date: Thursday, August 18, 2005 Sheet 6 of 40

Clocks



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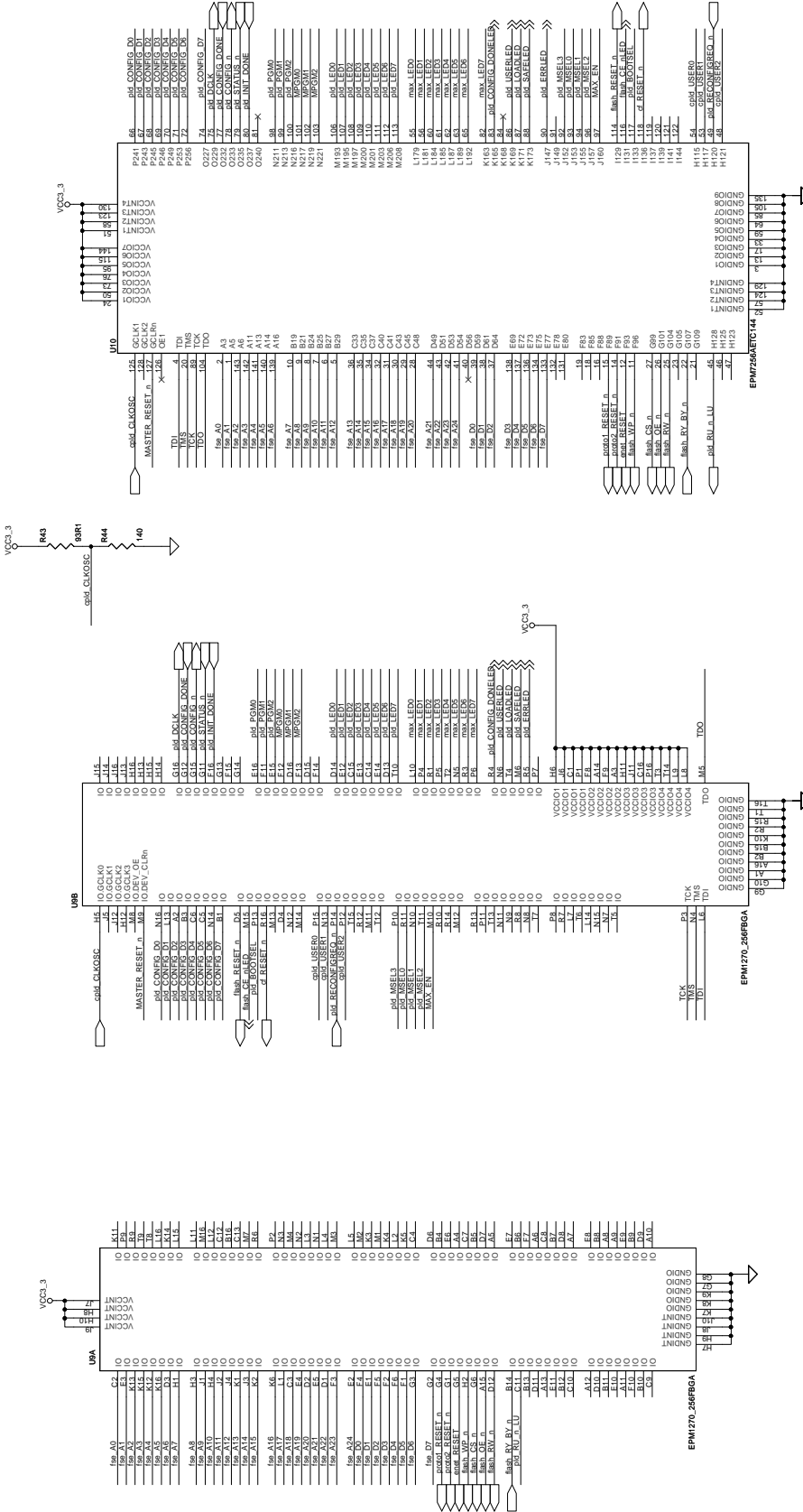
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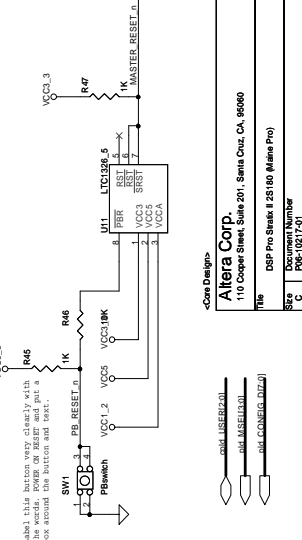
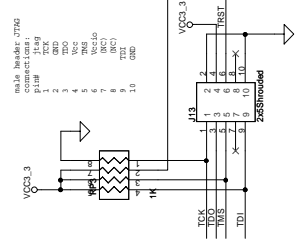
Size B Document Number P06-10217-01

Date: Thursday, August 18, 2005 Sheet 8 of 40 Rev 01

Configuration PLD

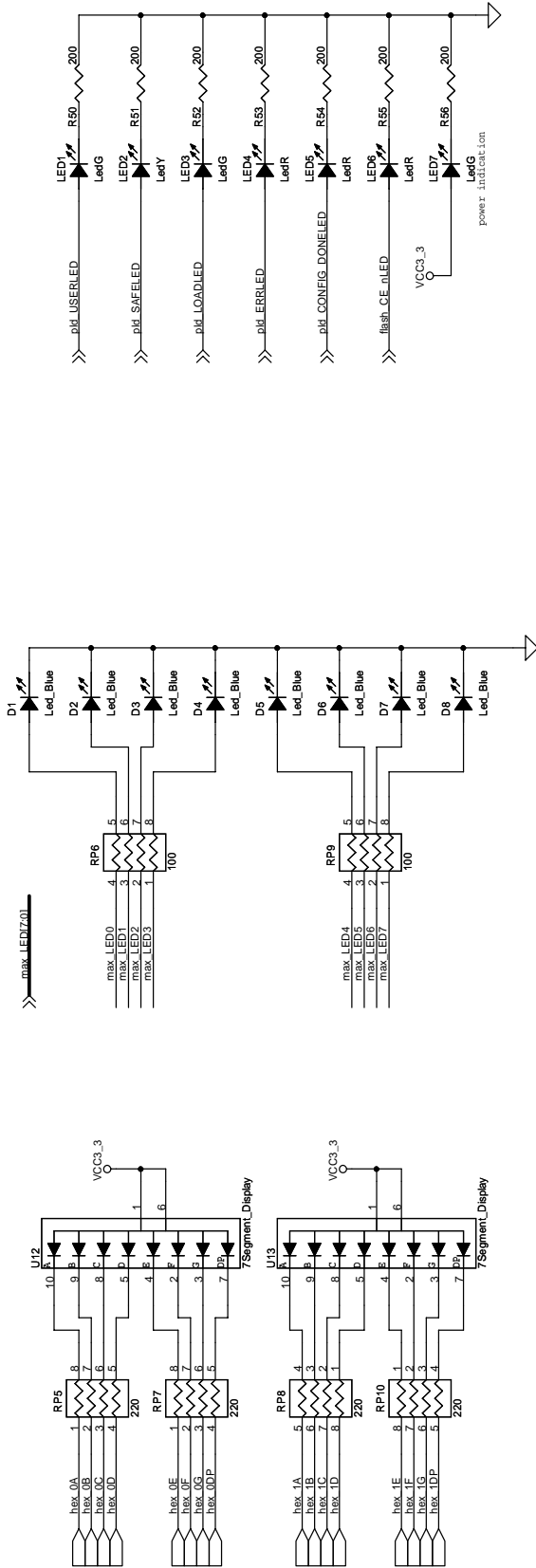


Configuration PLD



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Rev: 01

LEDs and Buttons



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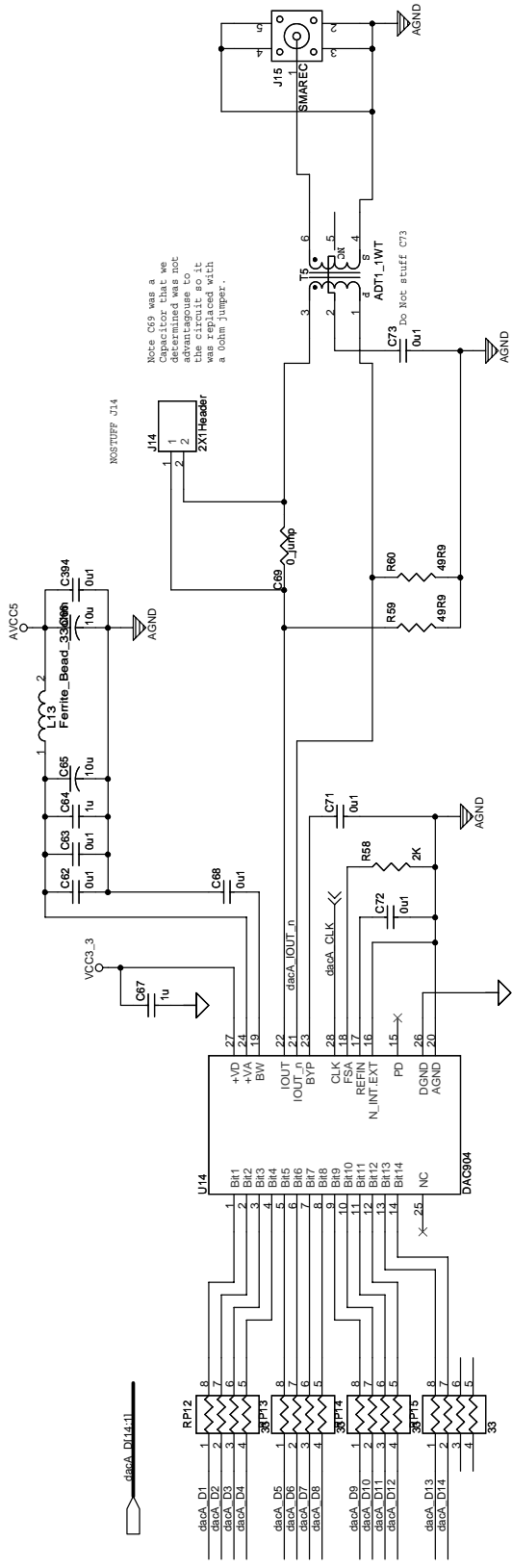
Document Number P06-10217-01

Date: Thursday, August 18, 2005

Sheet 10 of 40

Rev 01

DAC A



Note: C99 was a capacitor that we determined was not advantageous to the design. It was replaced with a 0ohm jumper.

TP1 should be labeled IOUT_n in silk screen
 Test_Header

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Size: B

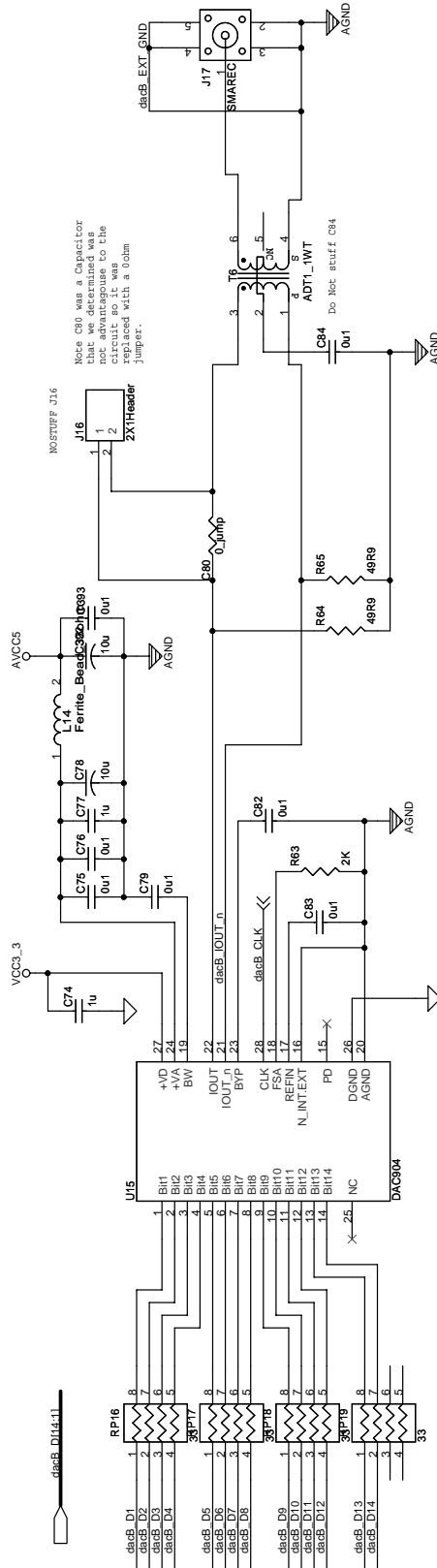
Document Number: P06-0217-01

Date: Thursday, August 18, 2005

Sheet 11 of 40

Rev: 01

DAC B



TP3 Should be labeled IOUT_n in silk screen
Test_Header

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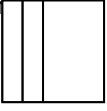
B P06-0217-01

Date: Thursday, August 18, 2005 Sheet 12 of 40

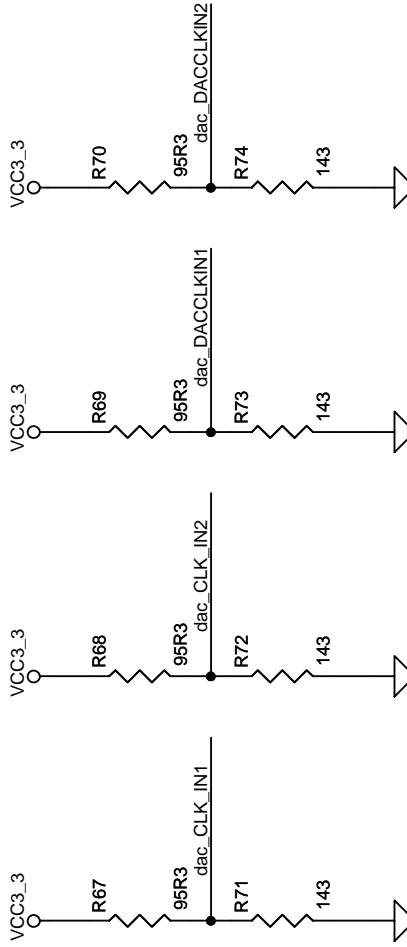
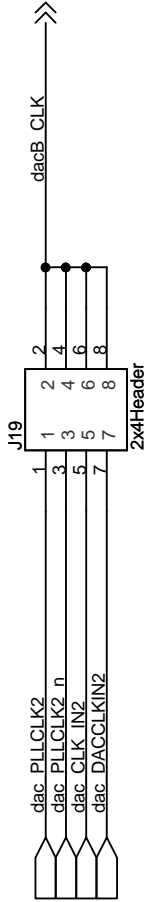
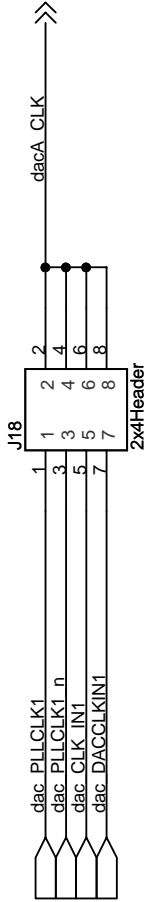
Rev 01

DAC Clock Jumper

S3 Shunt Jumper



S4 Shunt Jumper



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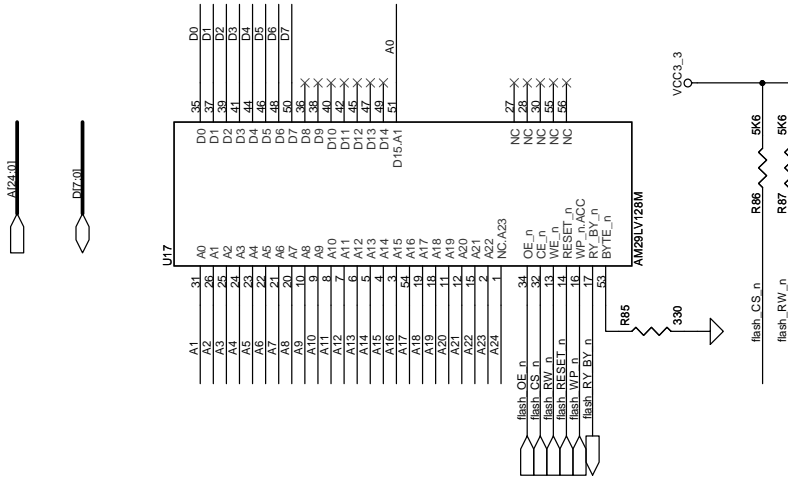
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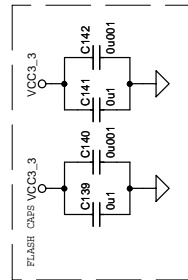
Size A Document Number P06-10217-01

Date: Thursday, August 18, 2005 Sheet 13 of 40

Flash



Flash chip is 16M x 8 for 16Mbytes of flash



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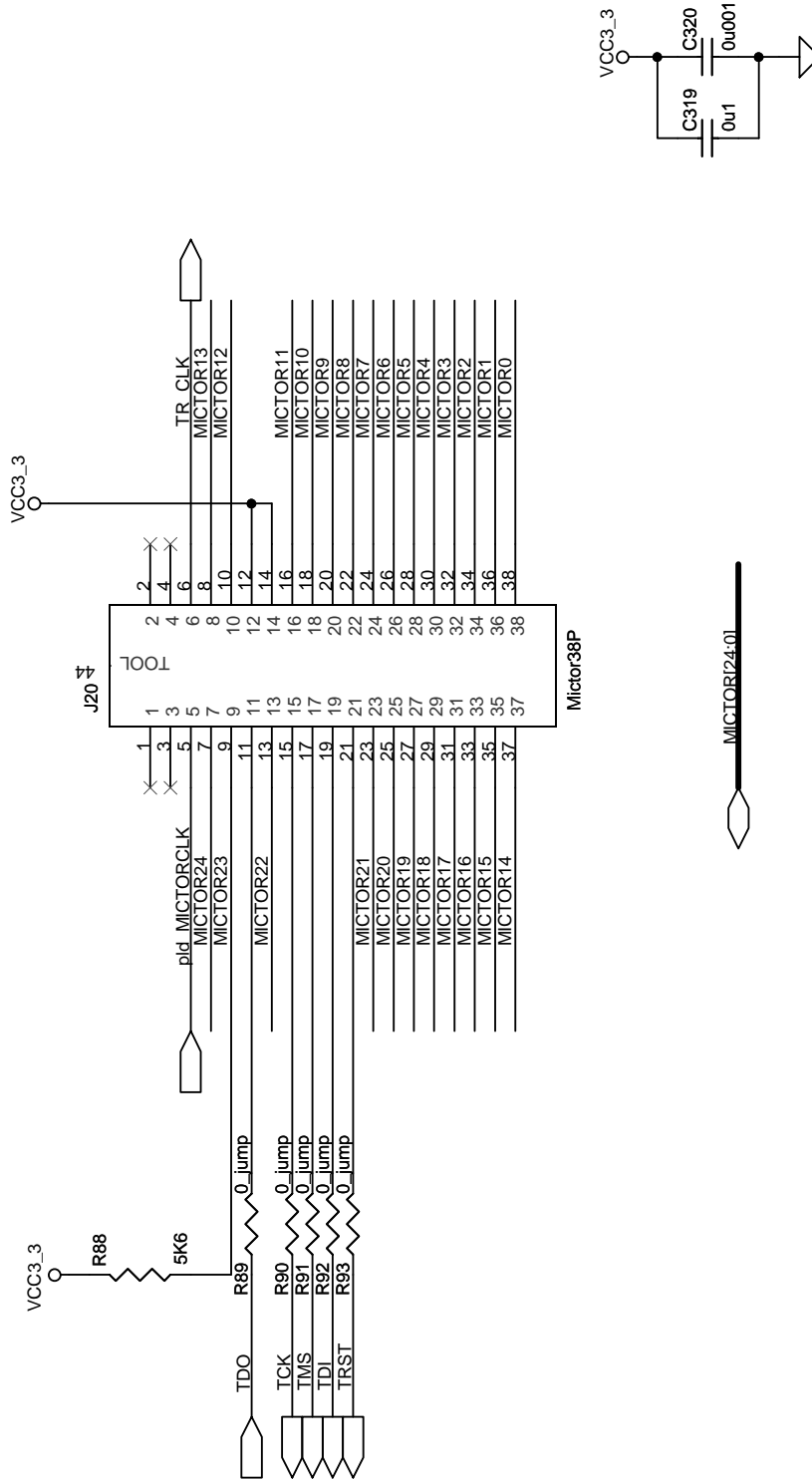
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Date: Thursday, August 18, 2005

Sheet 15 of 40

Rev 01

Mictor Connector



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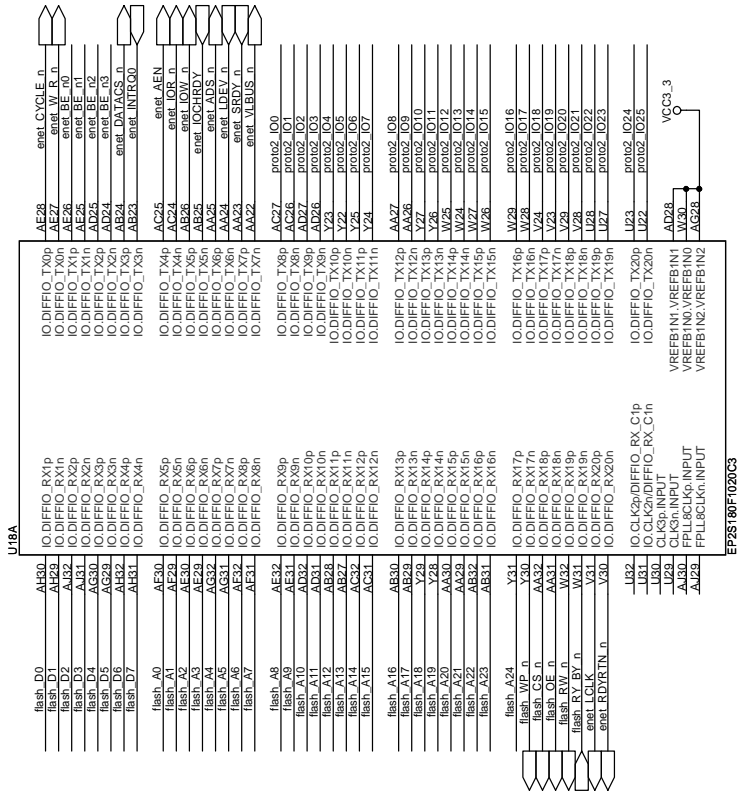
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Size A Document Number P06-10217-01

Rev 01

Date: Thursday, August 18, 2005 Sheet 16 of 40

PLD Bank 1



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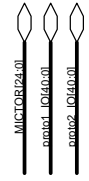
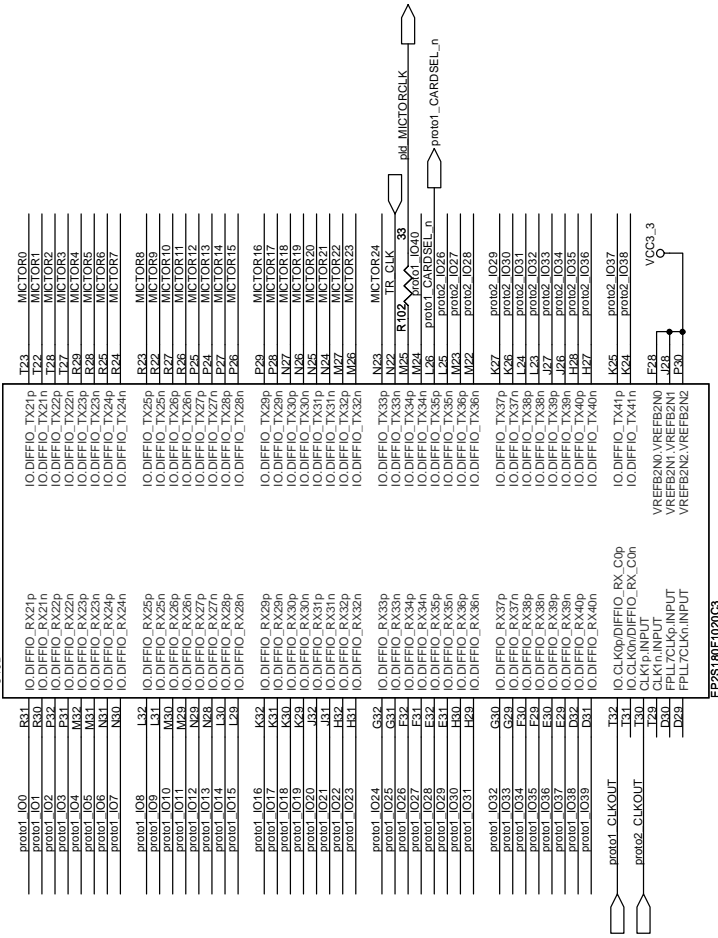
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Size	Document Number	Rev
B	P06-10217-01	01

Date: Thursday, August 18, 2005 Sheet 17 of 40

U18B



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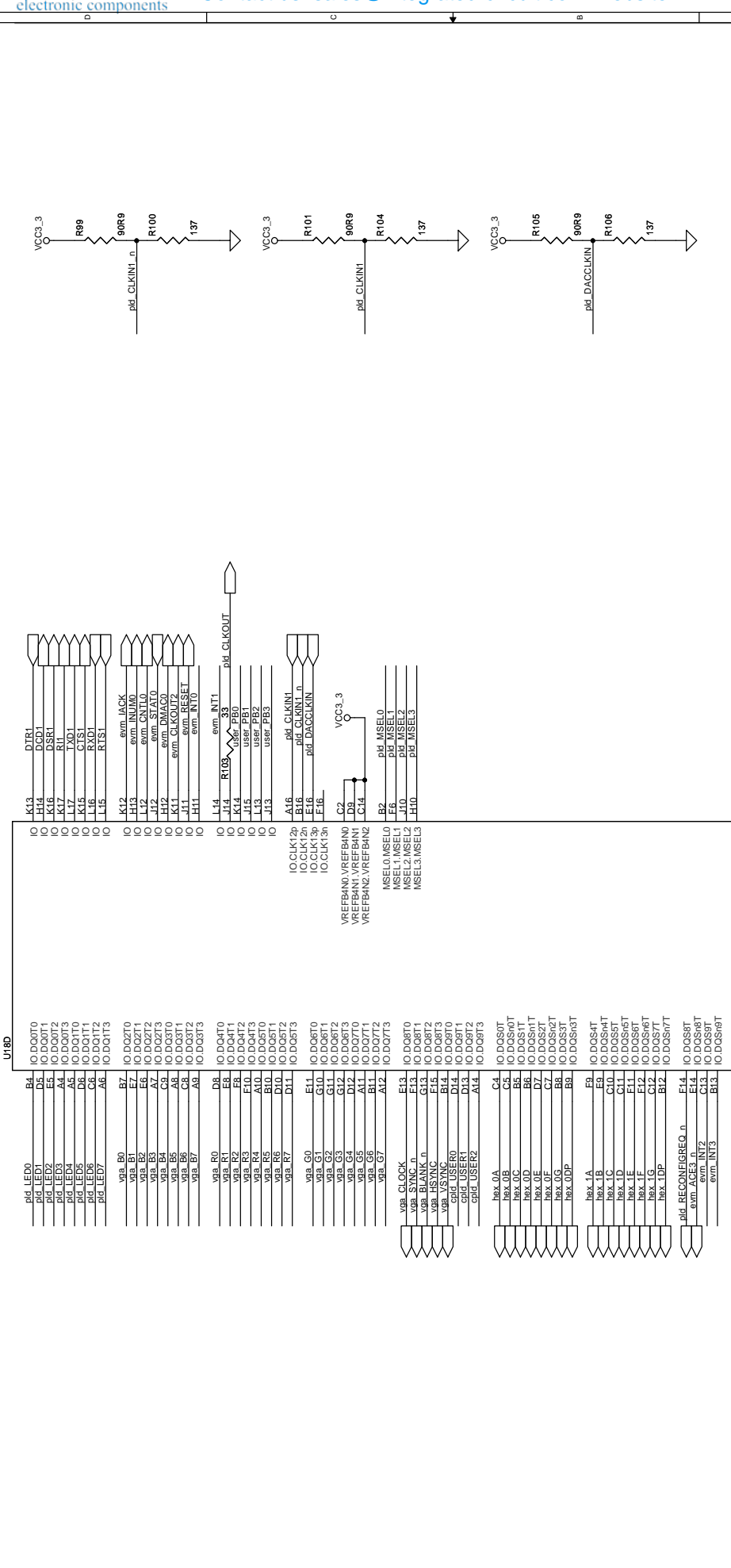
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Size	Document Number	Rev
B	P06-10217-01	01

Date: Thursday, August 18, 2005 Sheet 18 of 40

EP2S180F1020C3

PLD Bank 4



EP2S180F1020C3

IO.D00070	B4	pdl_LED0
IO.D00071	B5	pdl_LED1
IO.D00072	E5	pdl_LED2
IO.D00073	A4	pdl_LED3
IO.D00110	A5	pdl_LED4
IO.D00111	D6	pdl_LED5
IO.D00112	C8	pdl_LED6
IO.D00113	A6	pdl_LED7
IO.D00270	B7	vba_B0
IO.D00271	E7	vba_B1
IO.D00272	E8	vba_B2
IO.D00273	A7	vba_B3
IO.D00370	A8	vba_B5
IO.D00371	C8	vba_B6
IO.D00372	A8	vba_B7
IO.D00470	D8	vba_R0
IO.D00471	E8	vba_R1
IO.D00472	E8	vba_R2
IO.D00473	F10	vba_R3
IO.D00570	A10	vba_R4
IO.D00571	R10	vba_R5
IO.D00572	D11	vba_R7
IO.D00670	E11	vba_G0
IO.D00671	G10	vba_G1
IO.D00672	G11	vba_G3
IO.D00673	G12	vba_G4
IO.D00770	A11	vba_G5
IO.D00771	B11	vba_G6
IO.D00772	B11	vba_G7
IO.D00773	A12	vba_G7
IO.D00870	F13	vba_CLOCK
IO.D00871	F13	vba_SYNC_n
IO.D00872	G13	vba_BLANK_n
IO.D00873	F15	vba_USYNC
IO.D00970	F14	vba_USER0
IO.D00971	D14	chd_USER0
IO.D00972	D13	chd_USER1
IO.D00973	A14	chd_USER2
IO.D00974	A14	chd_USER2
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IO.D01261	B8	hex_08
IO.D01262	B8	hex_09
IO.D01263	B8	hex_0A
IO.D01264	B8	hex_0B
IO.D01265	B8	hex_0C
IO.D01266	B8	hex_0D
IO.D01267	B8	hex_0E
IO.D01268	B8	hex_0F
IO.D01269	B8	hex_08
IO.D01270	B8	hex_09
IO.D01271	B8	hex_0A
IO.D01272	B8	hex_0B
IO.D01273	B8	hex_0C
IO.D01274	B8	hex_0D
IO.D01275	B8	hex_0E
IO.D01276	B8	hex_0F
IO.D01277	B8	hex_08
IO.D01278	B8	hex_09
IO.D01279	B8	hex_0A
IO.D01280	B8	hex_0B
IO.D01281	B8	hex_0C
IO.D01282	B8	hex_0D
IO.D01283	B8	hex_0E
IO.D01284	B8	hex_0F
IO.D01285	B8	hex_08
IO.D01286	B8	hex_09
IO.D01287	B8	hex_0A
IO.D01288	B8	hex_0B
IO.D01289	B8	hex_0C
IO.D01290	B8	hex_0D
IO.D01291	B8	hex_0E
IO.D01292	B8	hex_0F
IO.D01293	B8	hex_08
IO.D01294	B8	hex_09
IO.D01295	B8	hex_0A
IO.D01296	B8	hex_0B
IO.D01297	B8	hex_0C
IO.D01298	B8	hex_0D
IO.D01299	B8	hex_0E
IO.D01300	B8	hex_0F
IO.D01301	B8	hex_08
IO.D01302	B8	hex_09
IO.D01303	B8	hex_0A
IO.D01304	B8	hex_0B
IO.D01305	B8	hex_0C
IO.D01306	B8	hex_0D
IO.D01307	B8	

PLD Bank 5

U18E	U18E	U18E	U18E	
adCA_D0	D1	IO.DIFFIO_TX42p	J6	adI_D16
adCA_D1	D2	IO.DIFFIO_TX43p	J7	adI_D17
adCA_D2	E3	IO.DIFFIO_TX43n	J8	adI_D18
adCA_D3	E4	IO.DIFFIO_TX44n	K8	adI_D19
adCA_D4	F1	IO.DIFFIO_TX44p	K9	adI_D20
adCA_D5	F2	IO.DIFFIO_TX44n	L9	adI_D21
adCA_D6	F3	IO.DIFFIO_TX45p	L10	adI_D22
adCA_D7	F4	IO.DIFFIO_TX45n	M10	adI_D23
adCA_D8	F1	IO.DIFFIO_TX48p	M11	adI_D24
adCA_D9	F2	IO.DIFFIO_TX48n	N7	adI_D25
adCA_D10	G3	IO.DIFFIO_TX47p	K6	adI_D26
adCA_D11	G4	IO.DIFFIO_TX47n	L7	adI_D27
adCE_D0	G1	IO.DIFFIO_TX48p	L5	adI_D28
adCE_D1	G2	IO.DIFFIO_TX48n	L6	adI_D29
adCE_D2	H1	IO.DIFFIO_TX49p	M11	adI_D30
adCE_D3	H2	IO.DIFFIO_TX49n	M11	adI_D31
adCE_D4	H1	IO.DIFFIO_TX50p	M8	adI_D32
adCE_D5	H2	IO.DIFFIO_TX50n	M9	adI_D33
adCE_D6	J1	IO.DIFFIO_TX51p	M6	
adCE_D7	J2	IO.DIFFIO_TX51n	M7	
adCE_D8	K3	IO.DIFFIO_TX52p	N7	
adCE_D9	K4	IO.DIFFIO_TX52n	N8	
adCE_D10	K1	IO.DIFFIO_TX53p	N9	
adCE_D11	K2	IO.DIFFIO_TX53n	N9	
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adI_D2	N4	IO.DIFFIO_TX55p	P6	
adI_D3	N5	IO.DIFFIO_TX55n	P7	
adI_D4	M3	IO.DIFFIO_TX56p	P4	
adI_D5	M4	IO.DIFFIO_TX56n	P5	
adI_D6	M2	IO.DIFFIO_TX57p	P11	
adI_D7	L2	IO.DIFFIO_TX57n	P11	
adI_D8	N2	IO.DIFFIO_TX58p	R6	
adI_D9	N3	IO.DIFFIO_TX58n	R7	
adI_D10	M1	IO.DIFFIO_TX59p	R4	
adI_D11	M2	IO.DIFFIO_TX59n	R5	
adI_D12	R2	IO.DIFFIO_TX58p	R10	
adI_D13	R3	IO.DIFFIO_TX58n	R11	
adI_D14	P1	IO.DIFFIO_TX61p	T5	
adI_D15	P2	IO.DIFFIO_TX61n	T6	
T1	T1	IO.DIFFIO_TX62p	T11	fm_TACH
T2	T2	IO.DIFFIO_TX62n	T11	fm_EN_n
T3	T3	VREFBSN0.VREFBSN0	P3	VCC3_3
T4	T4	CLK11n.INPUT	J6	
D3	D3	CLK11p.INPUT	F5	
D4	D4	FPLL10CLKn.INPUT		
		FPLL10CLKp.INPUT		

EP2S180F1020C3



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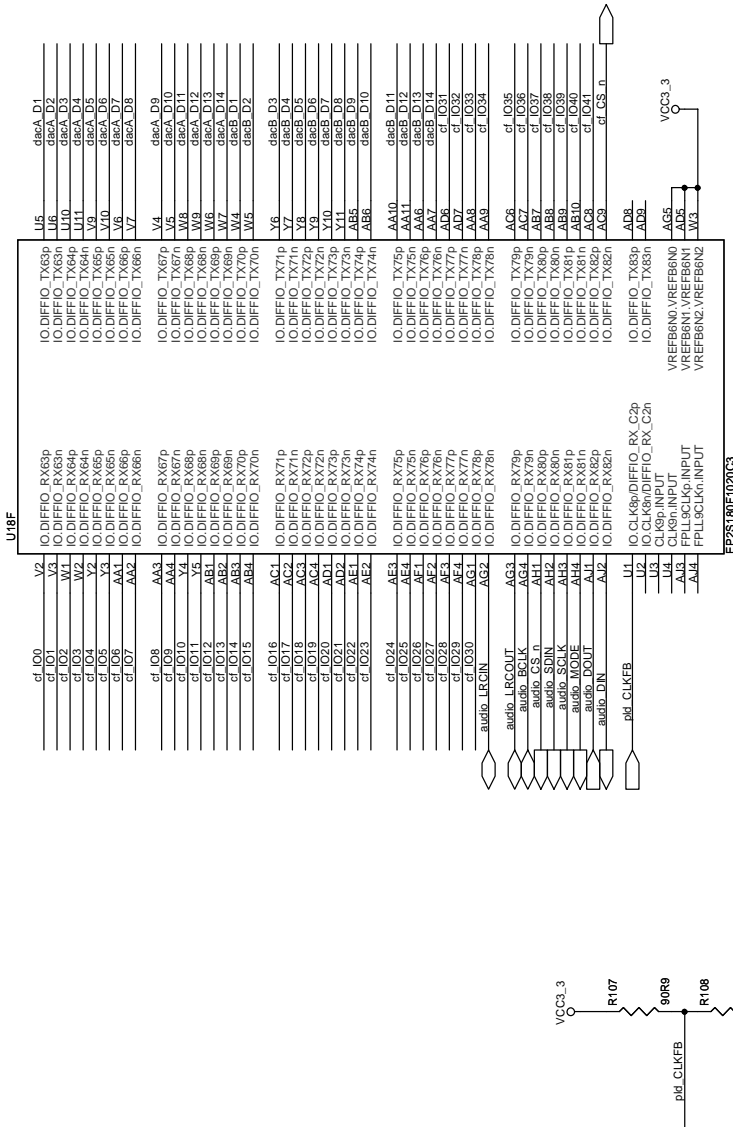
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B Pub-0217-01

Date: Thursday, August 18, 2005

Rev 01

Sheet 21 of 40



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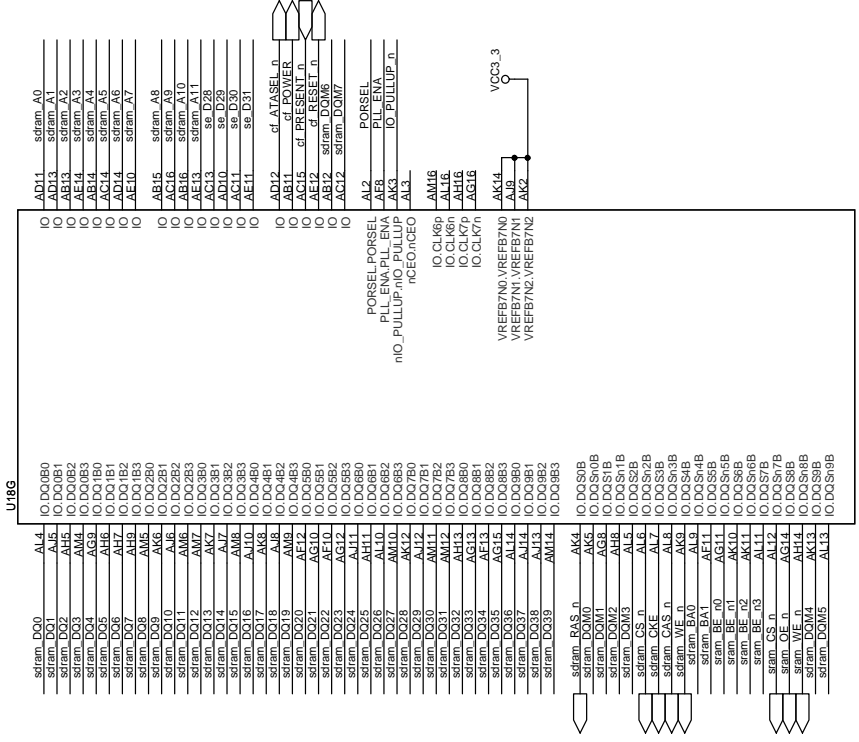
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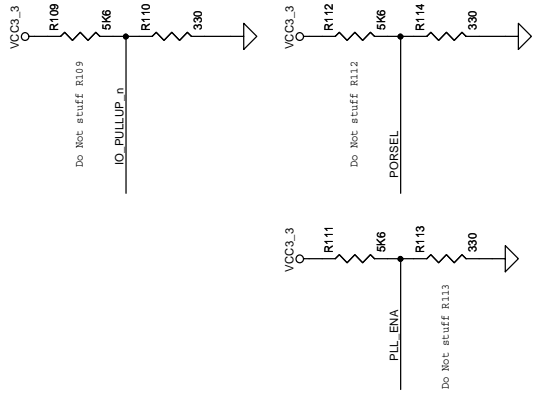
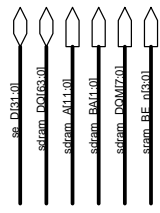
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B	P06-10217-01	01

Date: Thursday, August 18, 2005 Sheet 22 of 40

PID Bank 7



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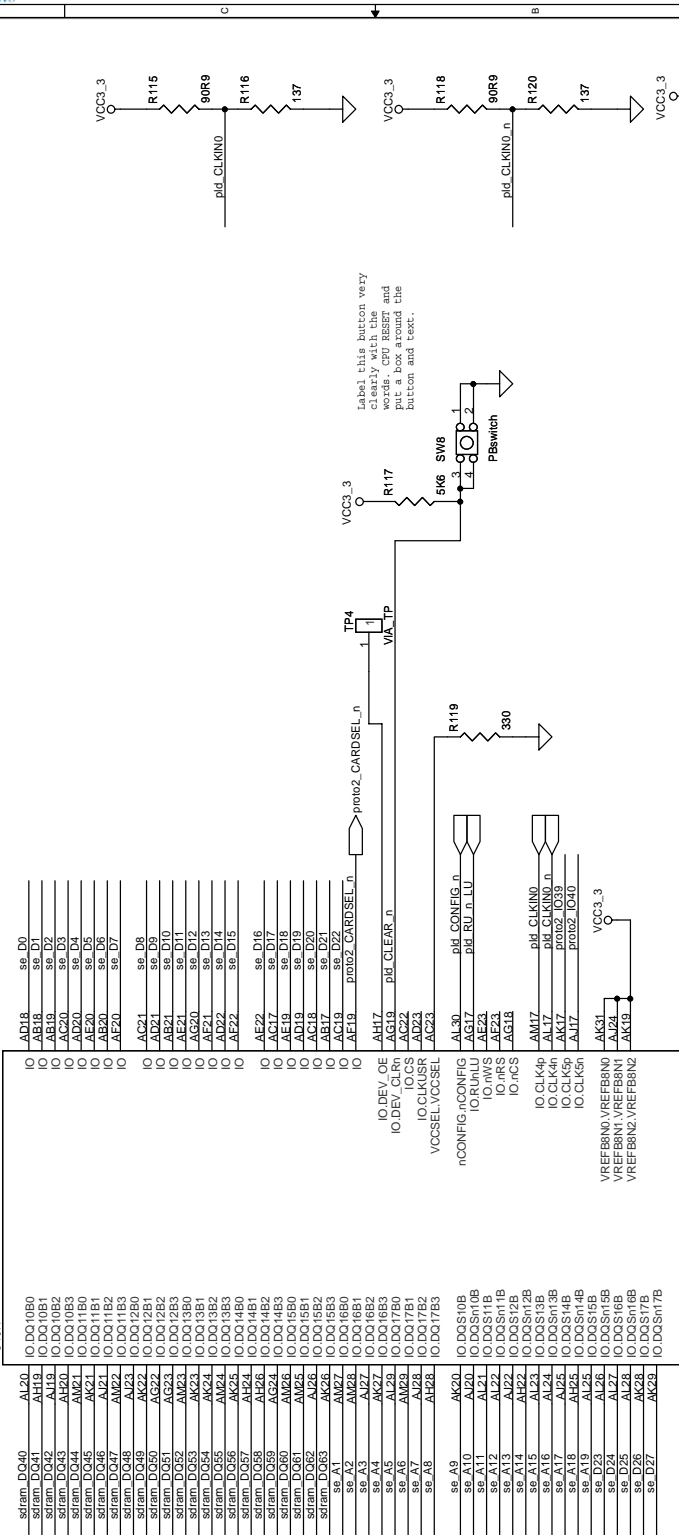
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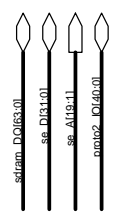
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B	Pdb-0217-01	01
Date:	Thursday, August 18, 2005	Sheet 23 of 40

PLD Bank 8

U18H



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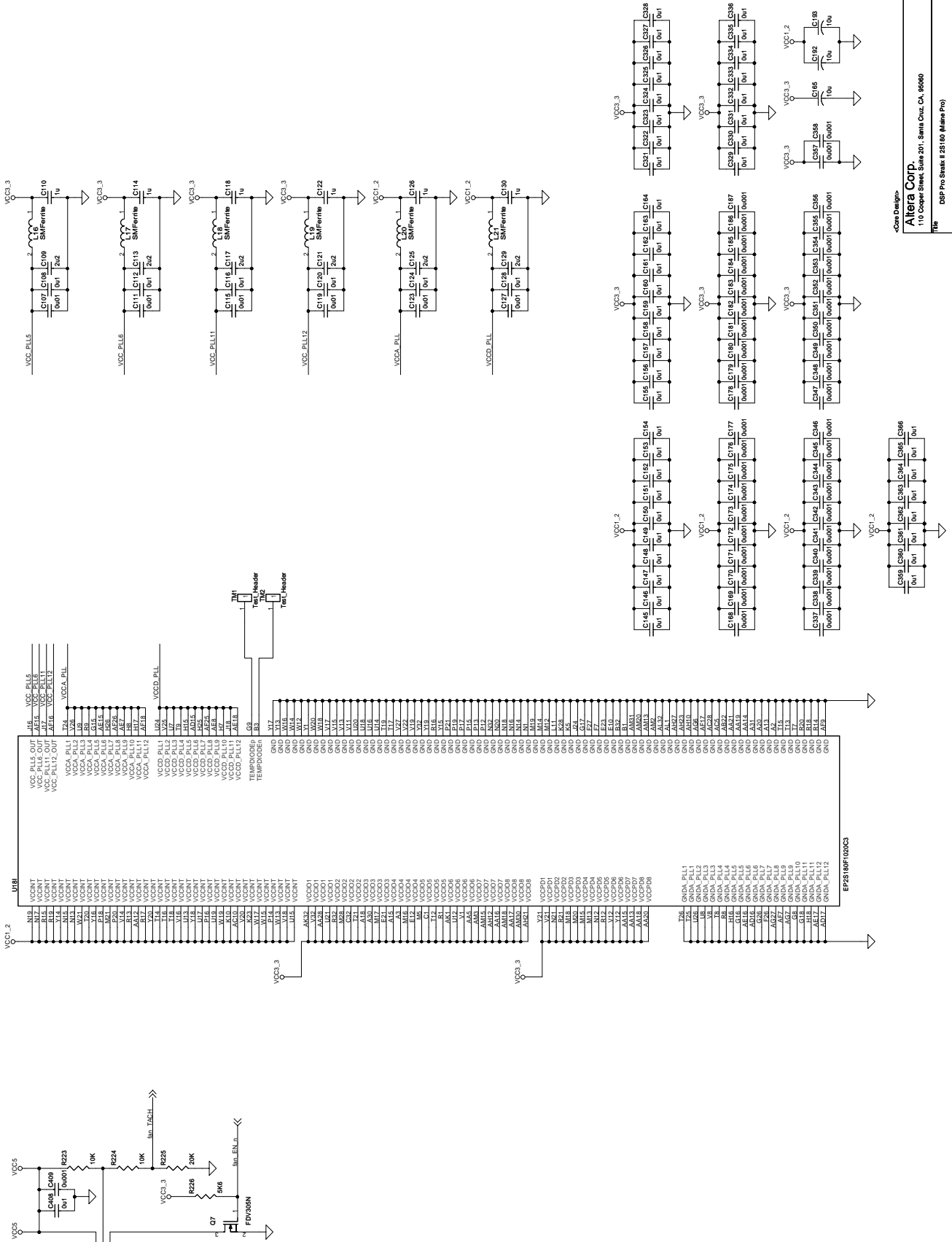
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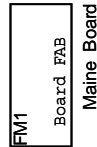
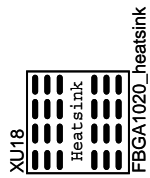
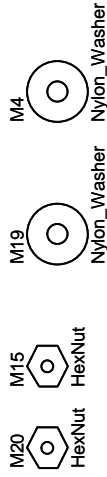
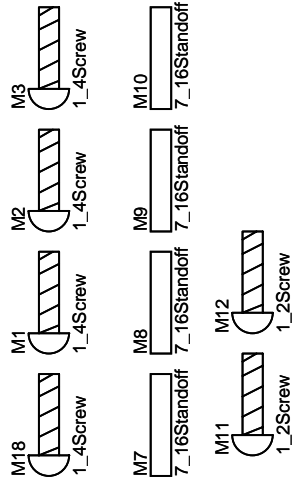
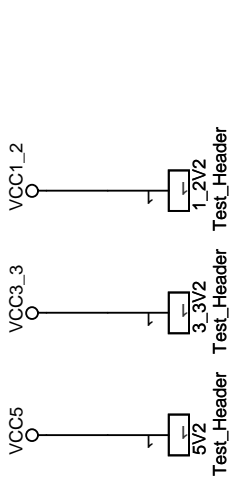
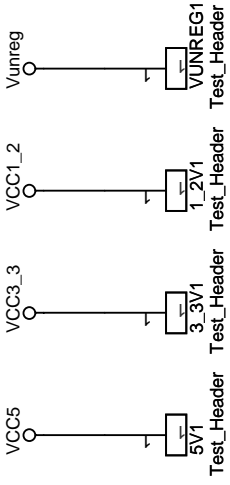
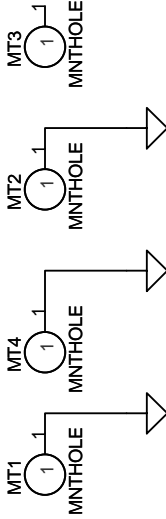
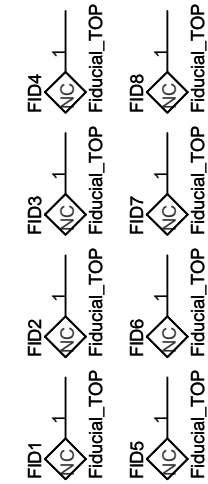
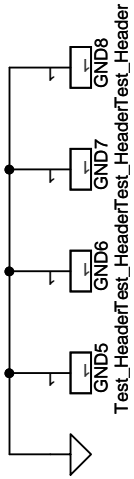
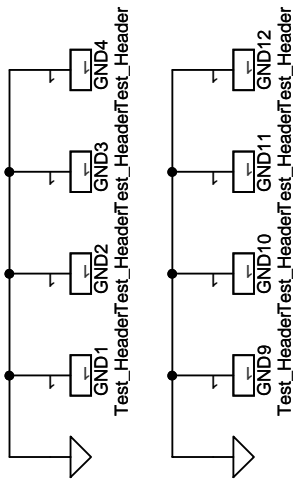
Date: Thursday, August 18, 2005 Sheet 24 of 40

PLD Power



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 File: DSP Pro Schem # 2S180 (Maine Pro)
 Date: 08/17/01
 Rev: 01
 Sheet: 28 of 40

Reset and Test headers



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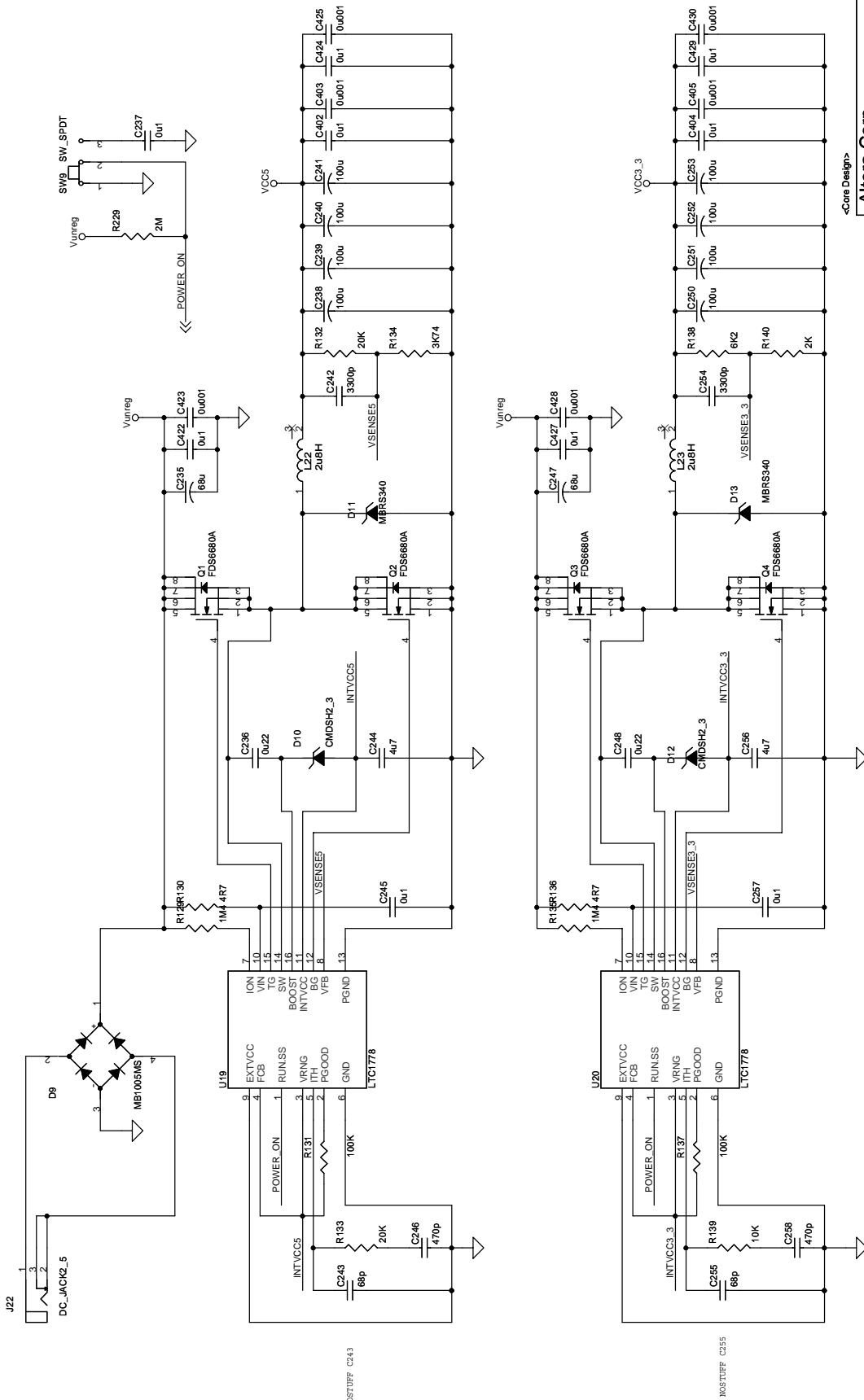
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Size A Document Number P06-10217-01

Rev 01

Date: Thursday, August 18, 2005 Sheet 28 of 40

Power 5V and 3.3V



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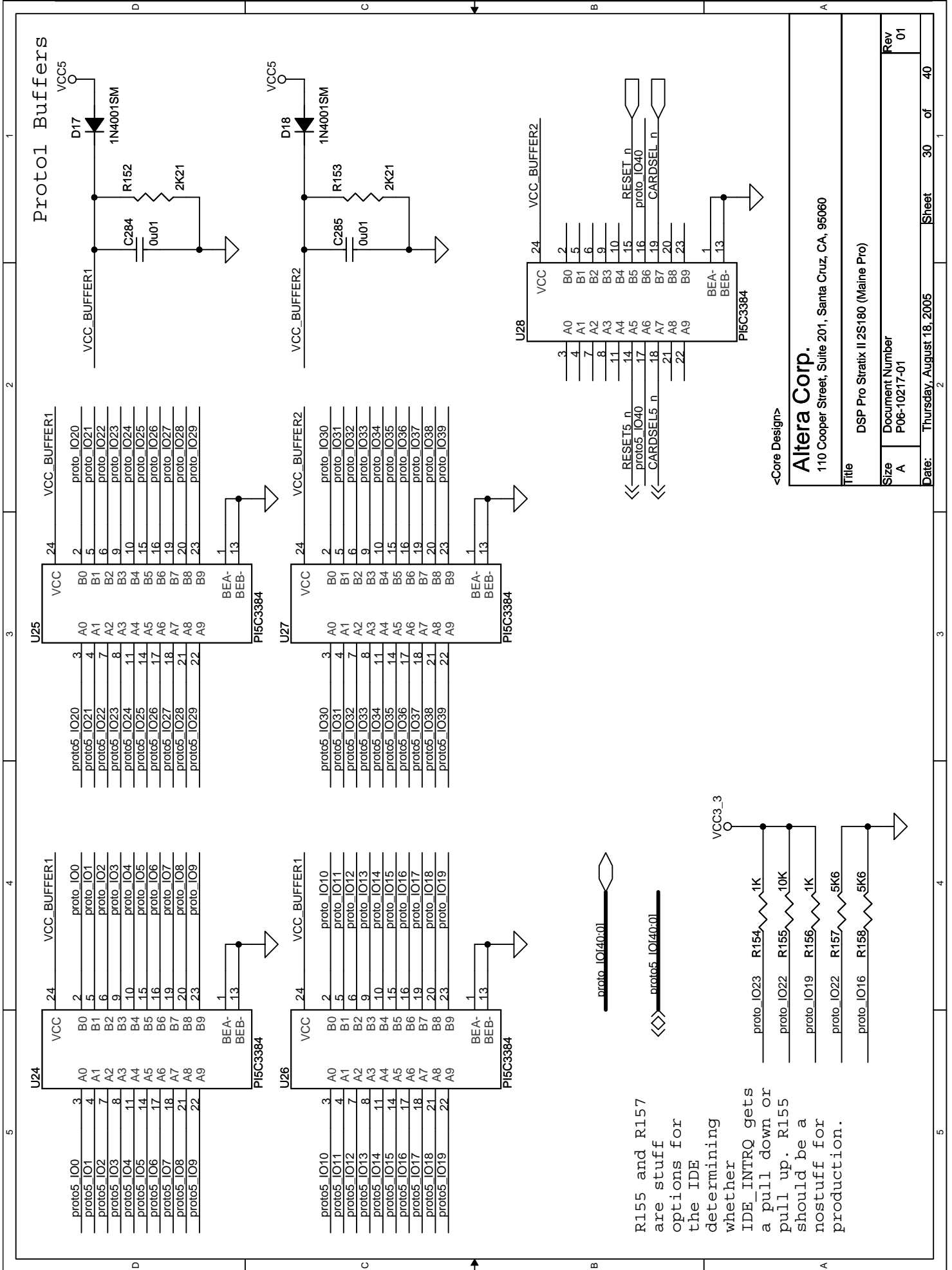
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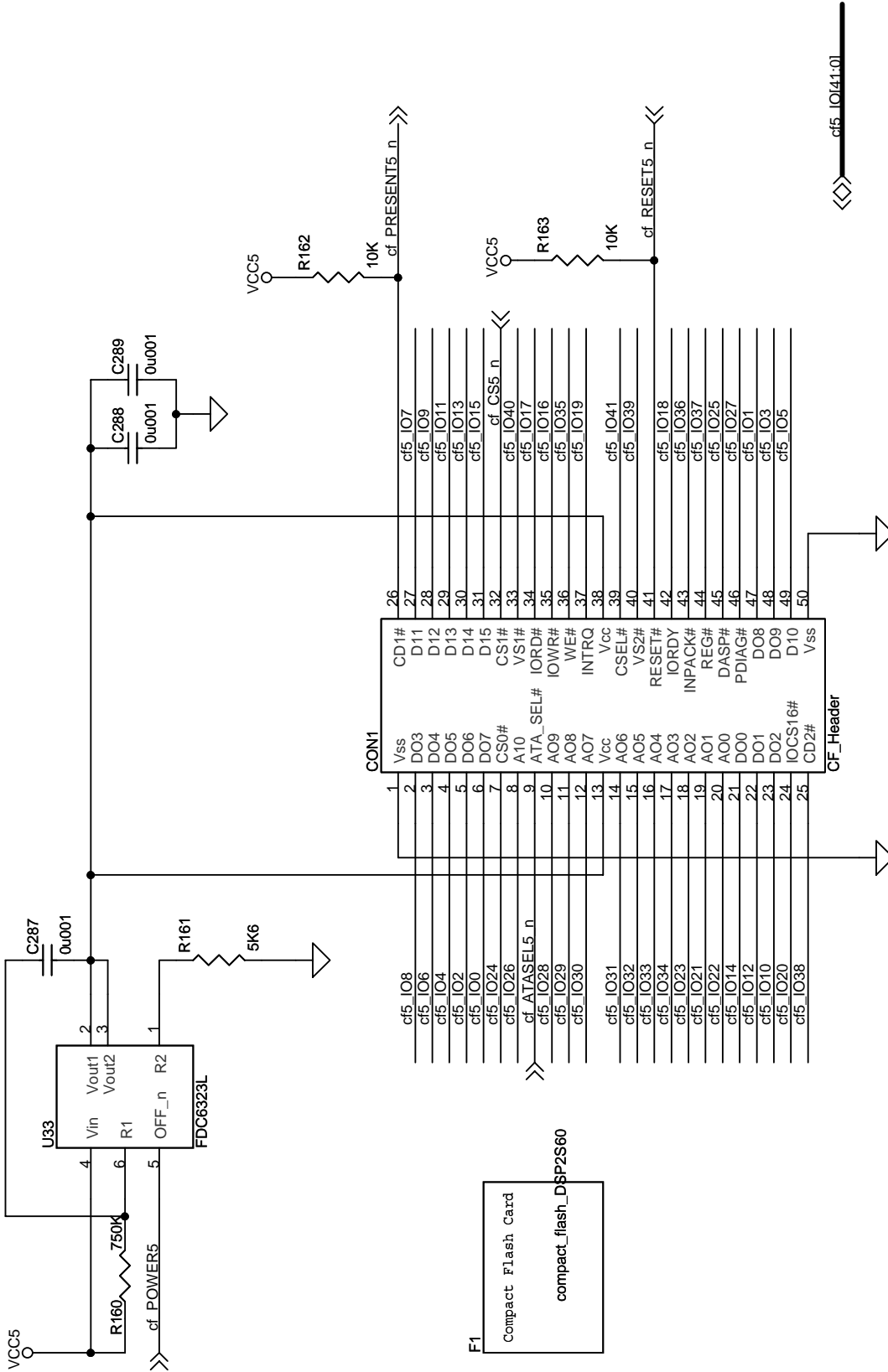
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Date: Thursday, August 18, 2005 Sheet 29 of 40

Rev 01

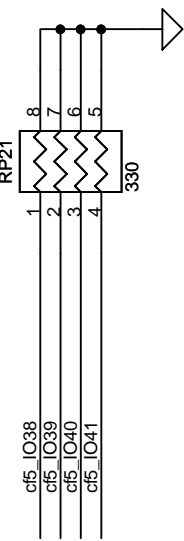


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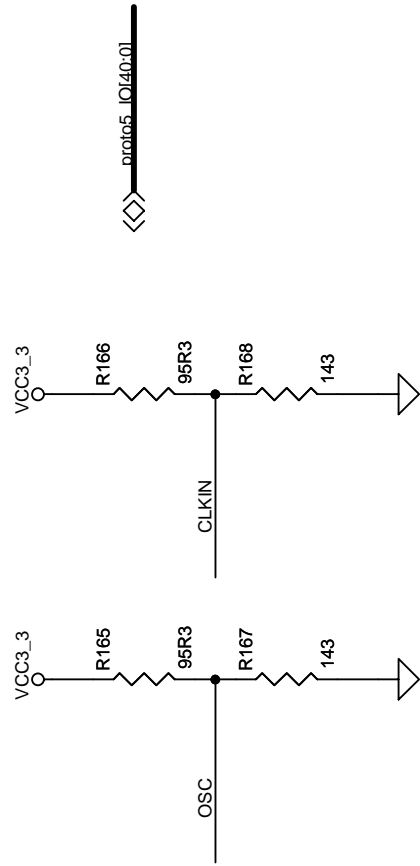
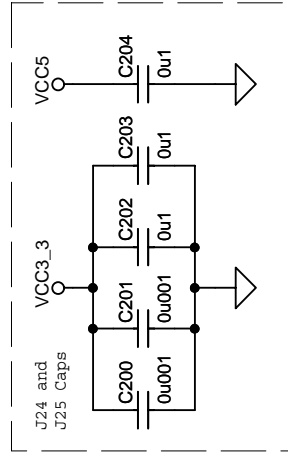
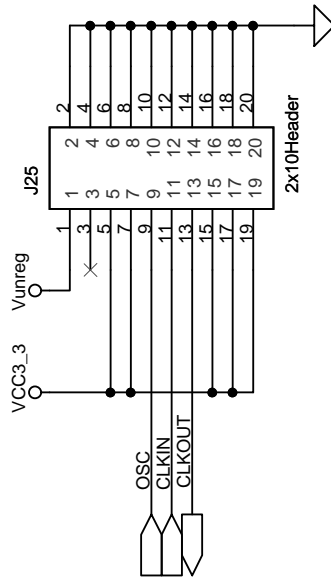
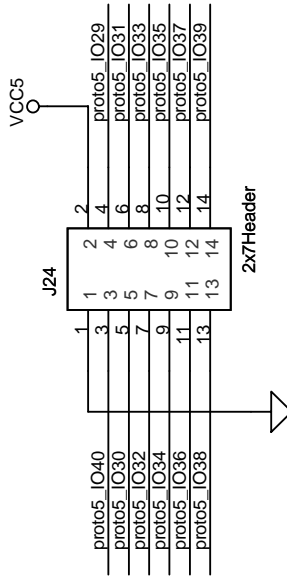
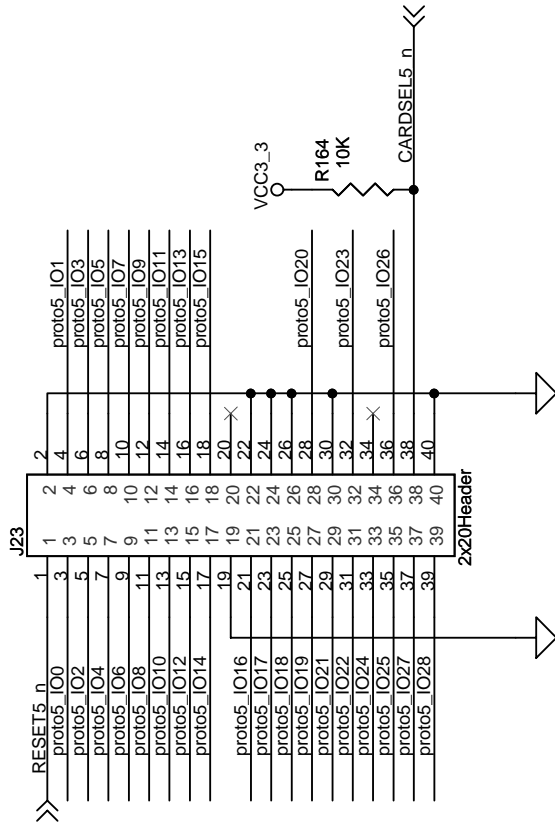


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Title		DSP Pro Stratix II 2S180 (Maine Pro)
Size	Document Number	P06-10217-01
Rev		01
Date:	Thursday, August 18, 2005	Sheet 32 of 40



Protocard 1



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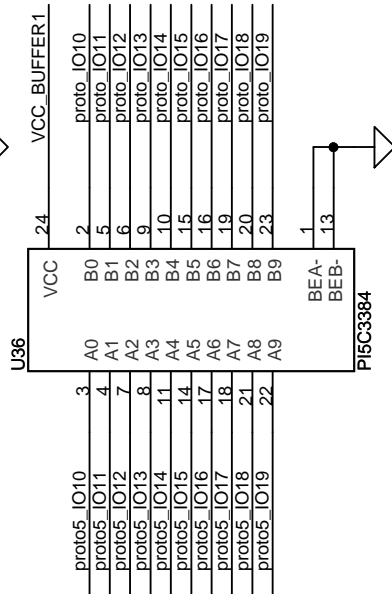
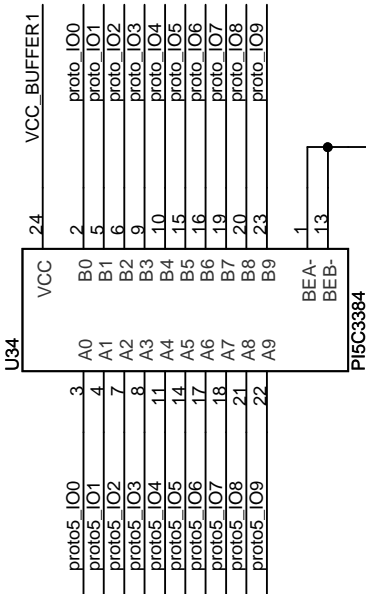
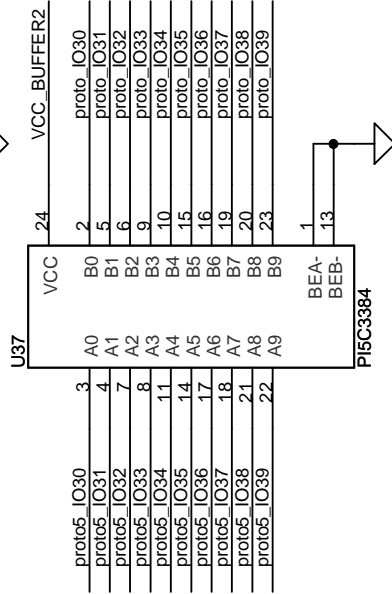
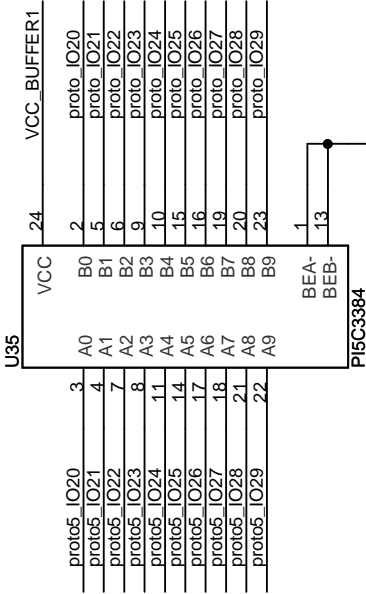
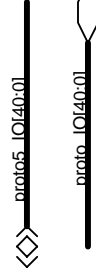
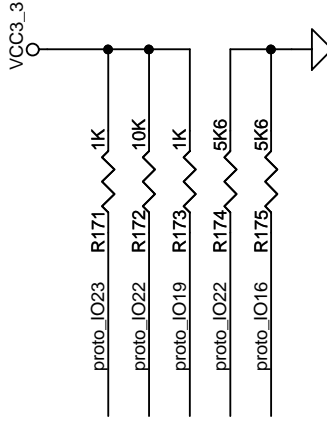
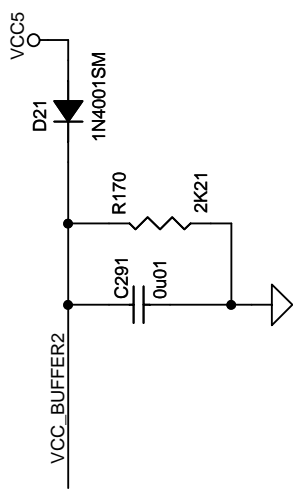
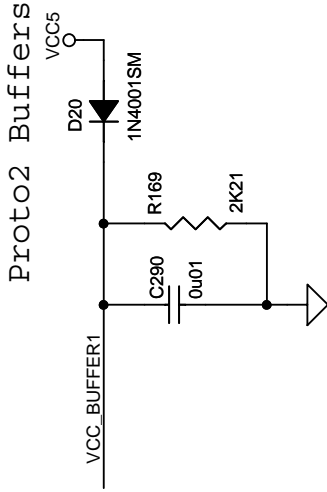
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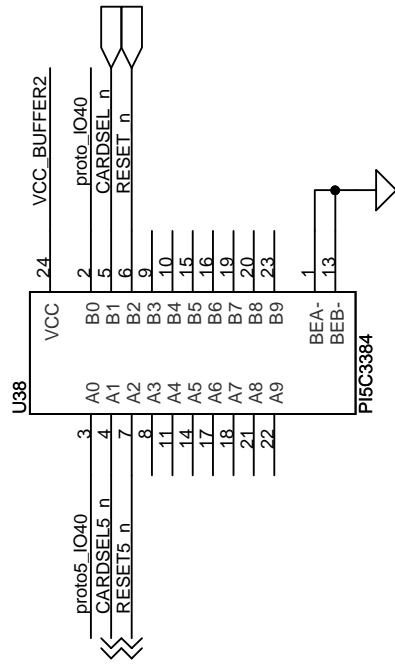
Rev 01

Date: Thursday, August 18, 2005 Sheet 33 of 40

Proto2 Buffers



R172 and R174 are stuff options for the IDE determining whether IDE_INTRQ gets a pull up. R172 or pull up. R172 should be a nostuff for production.



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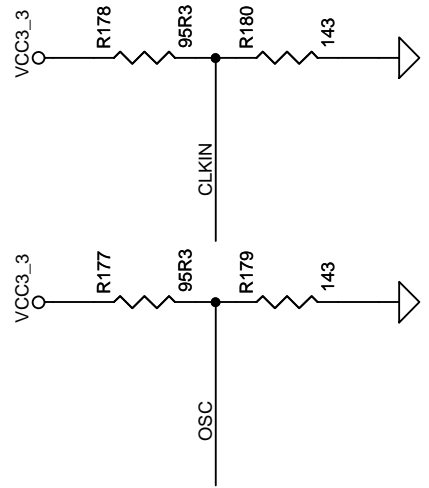
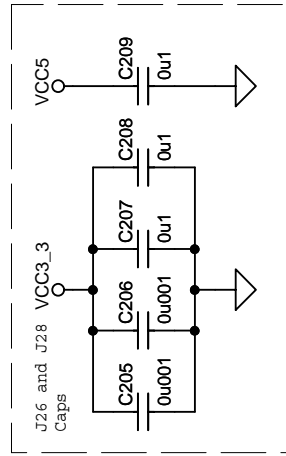
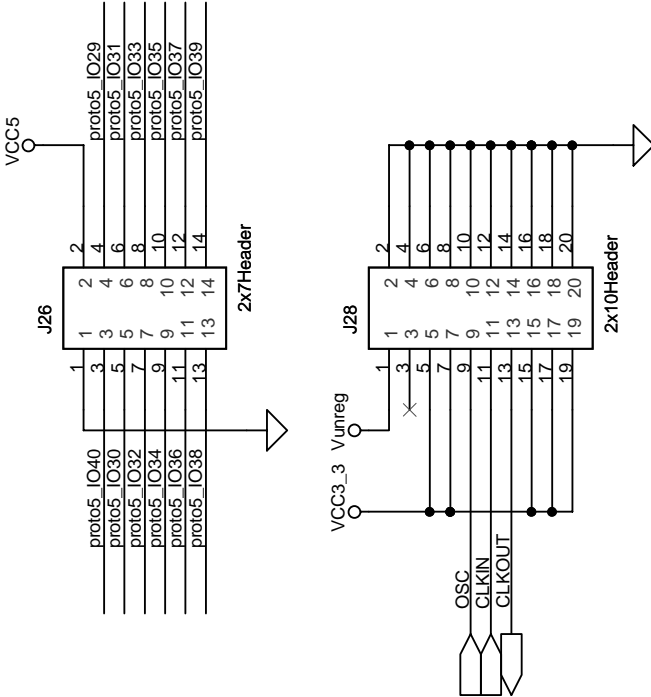
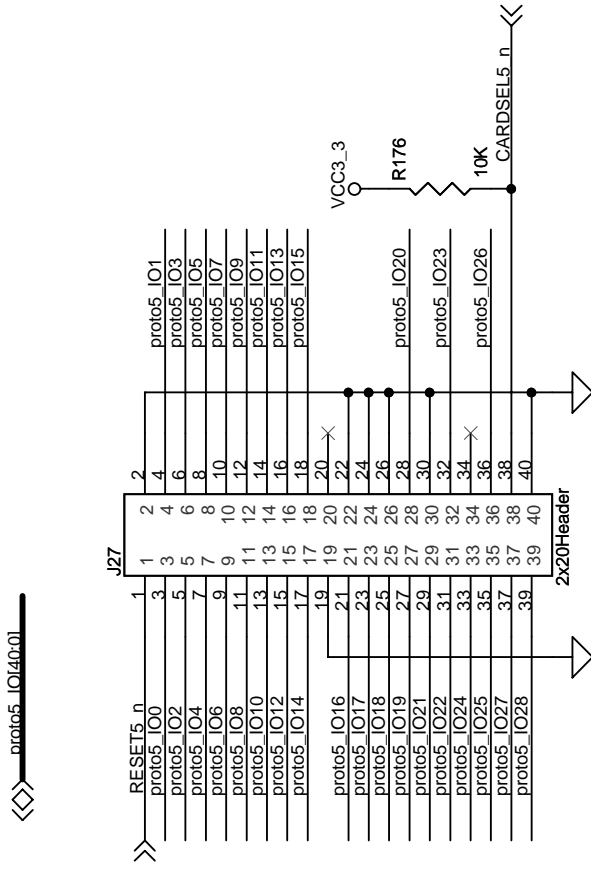
Title DSP Pro Stratix II 2S180 (Maine Pro)

Size A Document Number P06-10217-01

Rev 01

Date: Thursday, August 18, 2005 Sheet 34 of 40

Proto2 Headers



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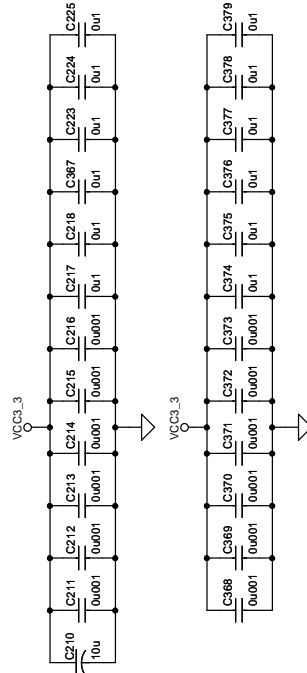
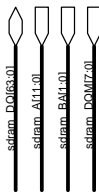
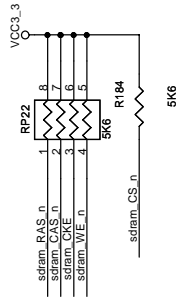
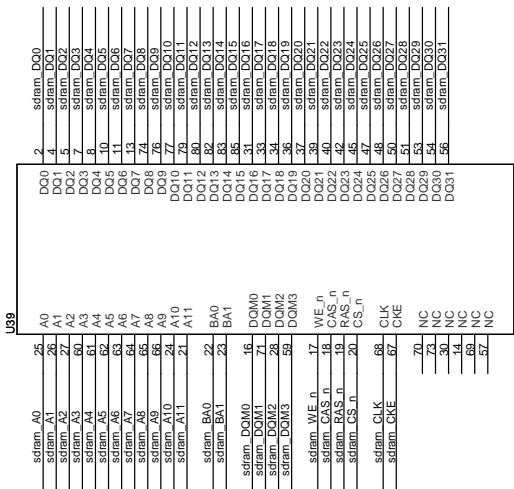
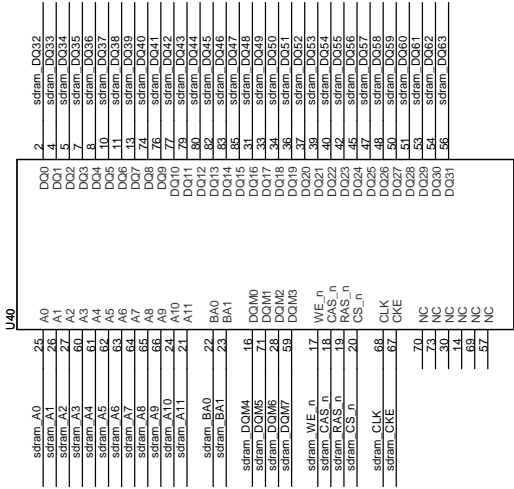
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Size A Document Number P06-10217-01

Date: Thursday, August 18, 2005 Sheet 35 of 40

SDRAM

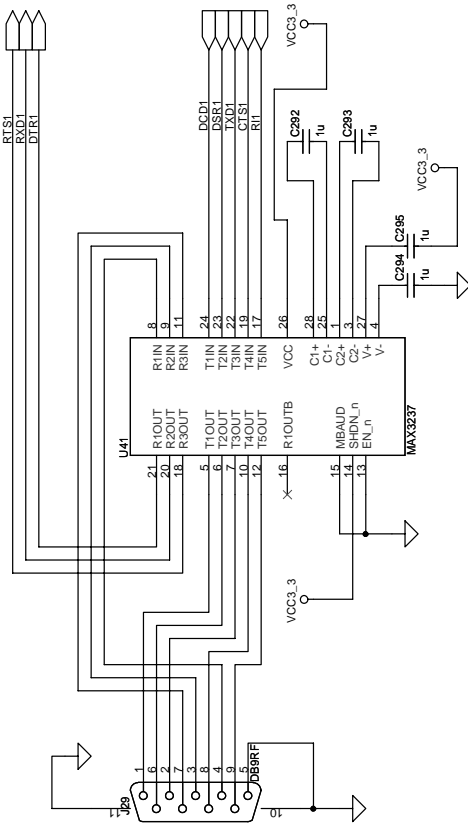
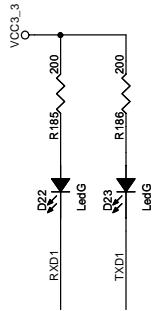


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Size	1	35	of 40
Docu	1		
Pub	10217-01		
Date:	Thursday, August 18, 2005	Sheet	35 of 40
Rev			01

Serial Ports



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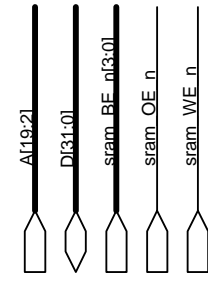
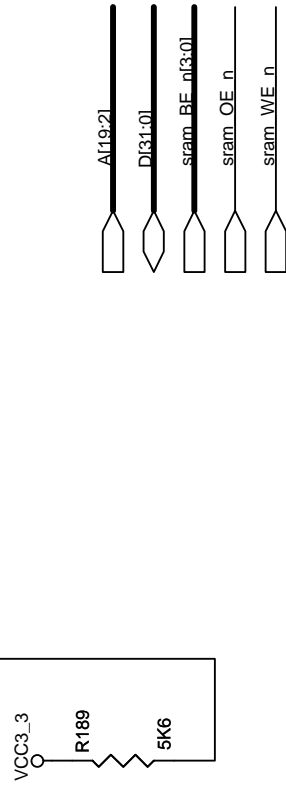
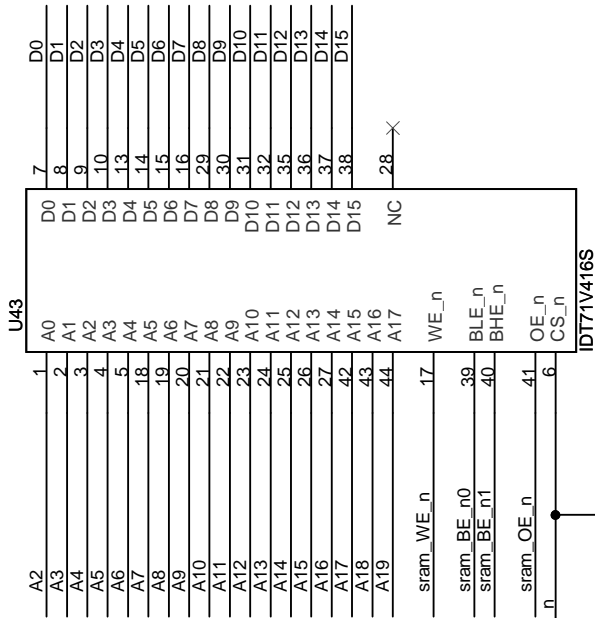
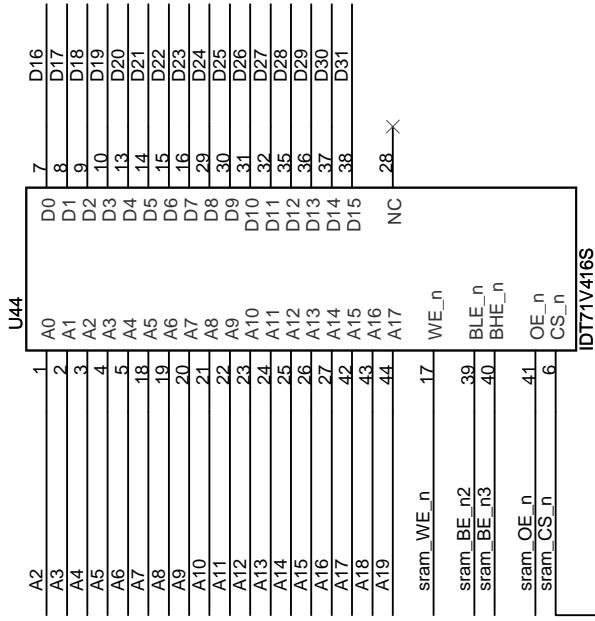
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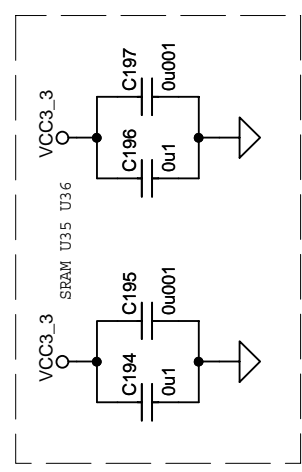
Sheet 37 of 40

Rev 01

SRAM



One bank of 256K x 32 SRAM (two 256K x 16 parts in parallel) = 1Mbyte of SRAM
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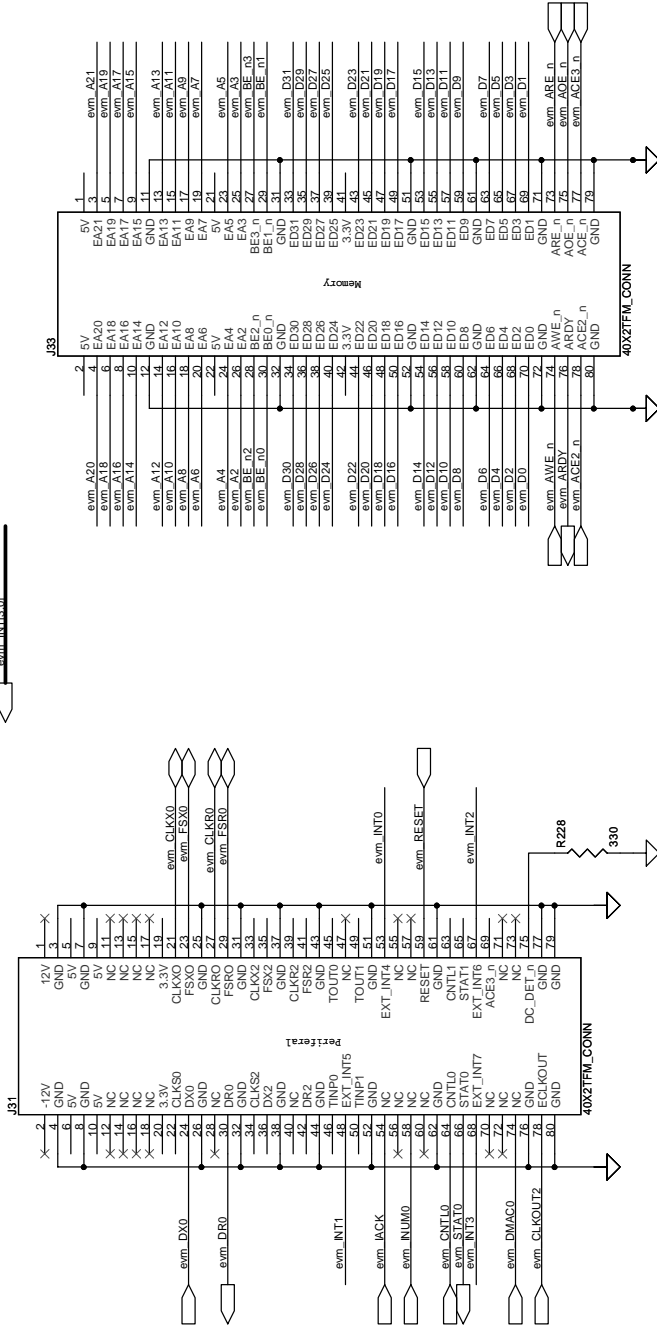


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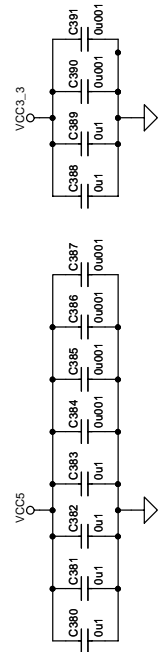
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Size	Document Number	P06-10217-01
Rev		01
Date:	Thursday, August 18, 2005	Sheet 38 of 40

TI EVM Connector

3.00" apart



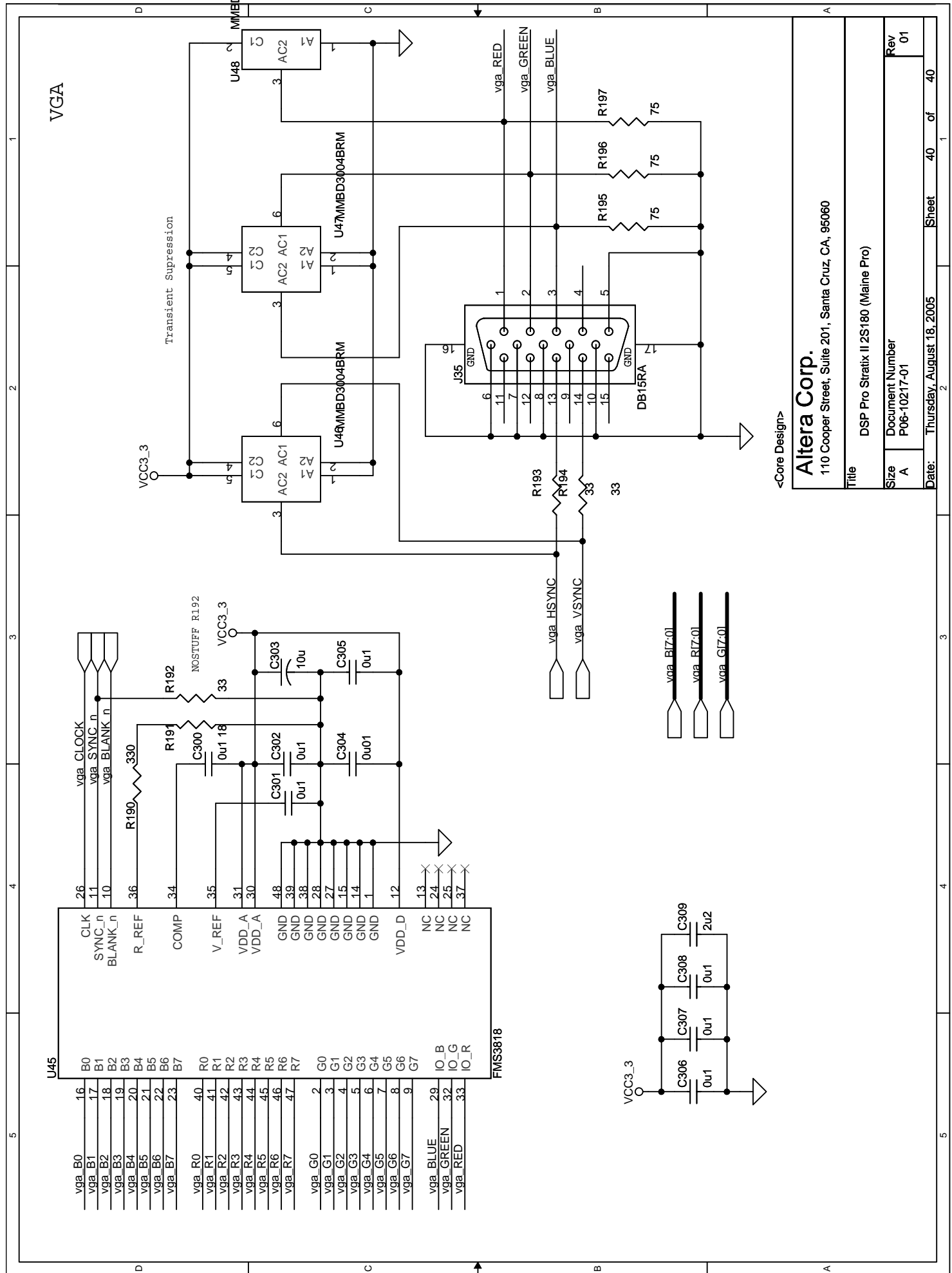
These connectors reference the TI 6416 board



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Size	Document Number
B	Pds-0217-01
Date:	Thursday, August 18, 2005
Sheet	39 of 40

Rev 01



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Title DSP Pro Stratix II 2S180 (Maine Pro)

Size A Document Number P06-10217-01

Date: Thursday, August 18, 2005 Sheet 40 of 40

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vga_B1	17	SYNC_n	11
vga_B2	18	vga_SYNC_n	10
vga_B3	19	BLANK_n	36
vga_B4	20	R_REF	34
vga_B5	21	COMP	35
vga_B6	22	V_REF	31
vga_B7	23	VDD_A	30
vga_R0	40	VDD_A	30
vga_R1	41	GND	48
vga_R2	42	GND	38
vga_R3	43	GND	28
vga_R4	44	GND	27
vga_R5	45	GND	15
vga_R6	46	GND	14
vga_R7	47	GND	1
vga_G0	2	VDD_D	12
vga_G1	3	NC	13
vga_G2	4	NC	24
vga_G3	5	NC	25
vga_G4	6	NC	37
vga_G5	7	IO_B	29
vga_G6	8	IO_GREEN	32
vga_G7	9	IO_RED	33

FMS3818